Improved Power Quality of Single Power Converter for SMPS

Dhara R. Ramani
IEEE Member

***Abstract*- This paper introduces a modified single-stage power factor correction (S2PFC) converter topology for high voltage, power and frequency (HVPF) applications which improves the power quality at utility AC side and at the load end. The modified proposed converter possess the ability of controlling the voltage and frequency independently and also simultaneously. The voltage can be controlled by PWM technique and also by dead time control which performs the boost operation. On the other side, frequency control can be obtained by using variable switching frequency. This paper presents the operation of the proposed converter topology, PWM switching scheme and MATLAB simulation results of the converter topology at a specific load are presented.**

***Index Terms*- High frequency (HF), modulation index (m), power factor correction (PFC), Duty ratio (K), High voltage, power and frequency (HVPF).**

I. INTRODUCTION

For industrial and domestic use, some applications require high frequency (HF) supply like getter firing for removing contamination from evacuated tubes, in semiconductor industry at purification zone, in the cutting and melting of metals and etc. With the recent advances in power electronics and magnetic materials, several converter topologies were proposed in literature, [1]-[11] for wide range of industrial and domestic applications which utilize HF supply voltage.

The power supply with a frequency range of 20-120 kHz (Medium range), is required for HF applications. Conventionally, this requirement was full filled by converter topologies with three-stage power conversions were proposed in [1], [2] and the block diagram of convention scheme is shown in Fig.1. The three-stage conversion is combination of diode bridge rectifier, which converts utility AC supply to rippled DC voltage. Second stage is a boost PFC intermediate stage, which improves power quality at the supply side and finally third stage for converting rippled DC into HF AC. As the power conversion is of three-stages efficiency and power density are less in these topologies.

A two-stage boost half bridge (B-H-B) converter with HF output and with two power conversion stages was proposed in [3], which offers high efficiency and power density compared to that of three-stage converter topologies, though the drawback of this topology was it provides low output voltage. For improving the performance of B-H-B-HF converters AC-AC single-stage converters with integrated voltage doubler circuits were proposed in [4], [5]. As these topologies offer controllable output voltage, but regulation of the output is complex.1

High frequency applications requires voltage at very high frequency, switching of semiconductor switches at these frequencies causes more switching losses and more stresses on switches, which reduces the life time of switches.

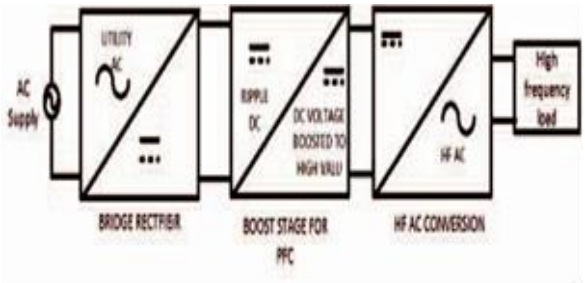


Fig.1. Conventional topology with three stage conversion.

In recent years for reducing the switching losses due to hard switching and for minimizing the electromagnetic interference (EMI) noise, resonant converter topologies were proposed in literature [6], [7]. These were HF Asymmetrical resonant converters with low cost and high power density, but output voltage regulation cannot be achieved without a complex control structure. Full bridge inverter topologies with zero voltage switching (ZVS), which are providing HF output voltage were proposed in

[8]-[11]. As these converters adopts different pulse width modulation (PWM) schemes for control, the switching losses are very much reduced and voltage regulation is possible. Though they have less power density, because soft switching is possible only within a narrow range. section-II. Section-III presents proposed open loop control scheme. Simulation results and operating range of the converter, are given in Section-IV.

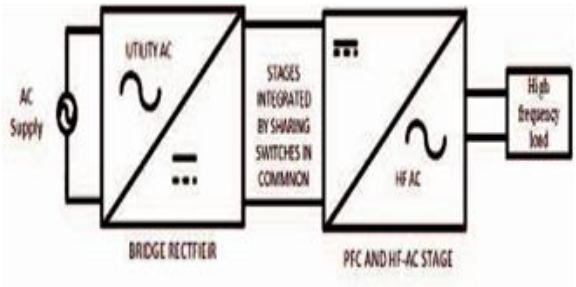


Fig.2. Single-stage integrated topology.

II.MODIFIED CONVERTER TOPOLOGY AND ITS FEATURES

A.Converter topology:

Three-level single-stage DC-DC converter with less number of components was suggested in [15]. Using [15], a modified single-stage AC-AC converter is proposed for HVPF applications, which is shown in the Fig.3. In this modified proposed topology AC supply is rectified by using Diode Bridge. The rippled DC is converted into high frequency voltage by a three-level converter. Three-level stage performs the input PFC by boosting the DC link voltage, which in turn provides high output AC voltage. The boosting operation is performed, when the two middle switches i.e., S2 and S3 are conducting. Upper and lower switches i.e., S1 and S4 are used for integrating the two levels. In this converter topology for attaining the higher output voltages, duty ratios of the middle switches and their dead time can be adjusted. The switching of middle two switches at minimum and maximum dead times provides, minimum and maximum boosting with the effect of modulation index.

The frequency of the output is considered as constant in this paper, whereas, the variable frequency output can be achieved by variable switching frequency. The switching scheme of the converter is such that the carriers of middle switches are shifted by 1800 with each other and the alternative switches should never be turned on at the same instant which makes a short circuit of the DC bus. In order to satisfy this, inverted carriers are used for the alternative switches.

B.Features of the converter:

1. Single-stage operation: The modified proposed converter is integrated single-stage PFC converter which has less number of power conversion stages compared to that of three and two stage converters [1]-[3].
2. High output voltage: By controlling the modulation index and duty ratios of the middle switches wide range of output voltage can be achieved.
3. Improved input power factor: With the boost operation at the dc link, the input current can be aligned in phase with that of input voltage, for boosting operation a boost inductor is used in the dc-link, by making the discontinuous current in the boost inductor input power factor can be maintained.
4. Input current with frequency ripple doubled: Middle two switches which are responsible for boost operation are simultaneously turned on, twice in a switching period, which causes the increased ripple in the input current as two times that of switching frequency.
5. Number of components: When compared to the all other converter topologies, this scheme utilizes less number of components, by eliminating auxiliary diodes and capacitors.

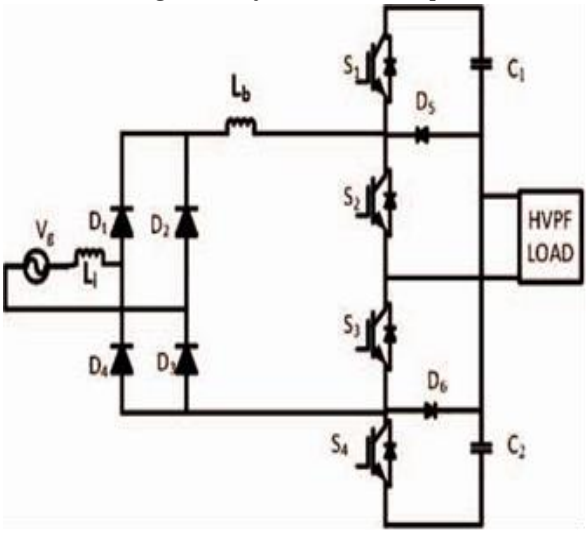


Fig.3. Open loop single-stage PFC converter.

III. PROPOSED OPEN LOOP CONTROL

A. PWM Scheme:

In the open loop control scheme, Pulse width modulatedgating signals for four switches and high frequency output voltage over one switching period are shown in Fig. 4

Carrier signals of middle switches are shifted by 1800. The modulation index 'm' is varied in between 0.55-0.95, the gate pulses of switches S1 and S4 are the inverse of S2 and S3. And turn on delay is inserted for switches S2 and S3, which introduces dead time at S1 turn off and S3 turn off similarly at S4 turn off and S2 turn on. This scheme assures that alternative switches are never turned on at same time which avoids short circuit of DC side. The mathematical relations for generating pulses in terms of switching frequency and duty ratio is as follows.

Where,

T_s = switching period.

K = duty ratio = $T_{on} \div T_s$.

Then Duty ratio of switch S_1 is K_1 " $(1\text{-}K_3)$.

B. Modes of operation

1. Mode-I: In the starting of this mode, S1 and S2 are in on condition. And capacitor C1 is discharged to the load by applying half of the dc bus voltage which is negative.
2. Mode-II: Switch S1 is off at the starting of this mode and S2 is in on condition, while zero voltage is applied across the load.
3. Mode-III: Switch S3 is turned on at the starting of the mode and S2 is still in on position, which makes the boost inductor to store the energy. In this period still output voltage is at zero level.
4. Mode-IV: At starting of this mode S2 is turned off and S4 is turned on. And C2 discharges by applying half of the dc bus voltage to the output, which is positive.
5. Mode-V: Switch S4 is turned off at starting of this mode. The output voltage is maintained at zero level and only S3 is in on condition.
6. Mode-VI: This is similar to mode-III, S3 is kept on and S2 is turned on. Input inductor stores the energy in this mode, by applying zero voltage level to the load.

Diodes D_5 and D_6 are forced to turned on in the boosting mode and whenever only one of the S_2 and S_3 are in conducting. Which applies zero voltage level across the load.

IV. SIMULATION RESULTS AND OPERATION RANGE

A. Simulation Results

This section presents the simulation results for the proposed open loop converter, with a load of 4.8kw across its output terminals. The converter is operated with a frequency of 25 kHz. Simulation results of switching pulses, output voltage, output Capacitor voltages, diodes and dc link currents are shown in Fig.5. It is observed that the operation of the converter whenever S1 and S2 are turned on, negative voltage is applied across the load and when S2 and S3 are turned on, the output voltage is at zero level and boosting of input inductor is done. In this case because of the load inductance diode D5 will get turned on and circulates the load current. Similarly, when S3 and S4 are turned on positive voltage is applied across the load. And, the same sequence will repeat. Fig.6, represents the capacitor voltage, it shows the charging and discharging of capacitor voltage around half of the DC bus voltage. The converter has the feature of PFC the input voltage and current waveforms for the simulated load are shown in Fig.7. Where, the input power factor is maintained at almost unity with a discontinuity in the inductor current waveform, which has ripple with double of frequency of output voltage. These simulations are performed at a modulation index of m=0.8 and turn on delay, which is responsible for dead time is taken as 10% of the duty ratio of middle switches.

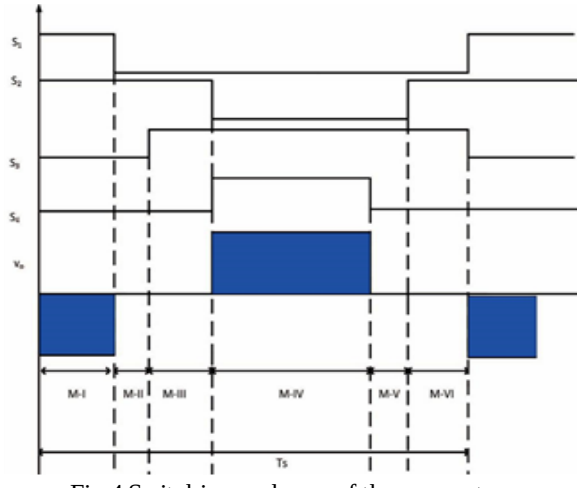


Fig.4.Switching scheme of the converter.

Comparison of the proposed converter topology with three-level, two-level and single-stage is given in Table.I.

TABLE.I TOPOLOGY COMPARISON

Parameter	Existing topologies	Proposed topology
Stages of conversion	Three-stages, [1], [2]. Two stage [3].	Single-stage
Stresses across the switches	More stresses , [1], [2]	Reduced to half.
Number of components Used in HF ac	More auxiliary components, [12]-[14]	Less components
Number of energy storage elements used for resonance	More number of elements, [16]	Very less and reasonable

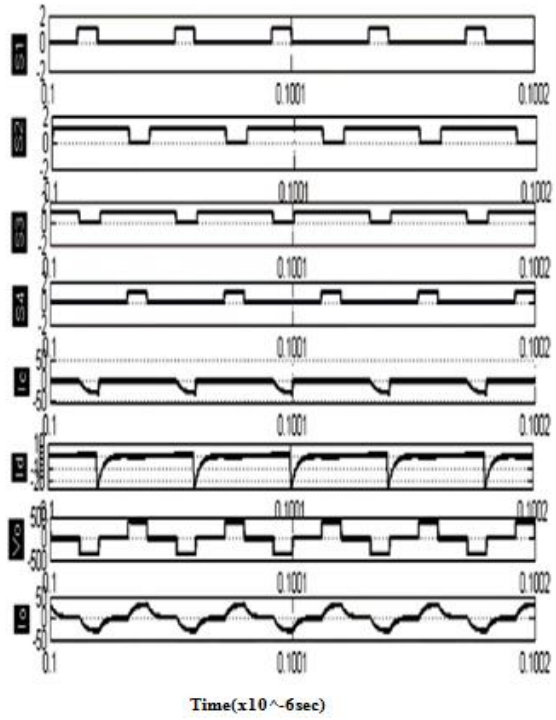


Fig.5. Simulation results of output voltage, capacitor, diode and output currents.

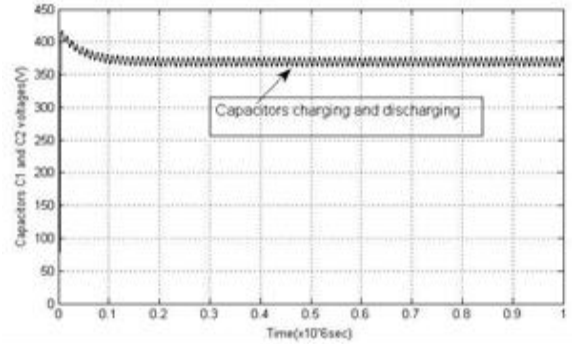


Fig.6.Charging and discharging of capacitors C1, C2.

B. Range of Operation:

The main feature of the proposed open loop converter topology is the adjustable output voltage, which can done by varying the 'm' of the switches and dead time adjustment of S2 and S3. By maintaining, the odd pair and even pair of switches should never be turned on at same time. The two extreme dead time for middle switches S2 and S3 are shown in Fig. 8. And the variation of voltage across the capacitor with different values of 'm' and for different dead times is shown in Fig. 9.

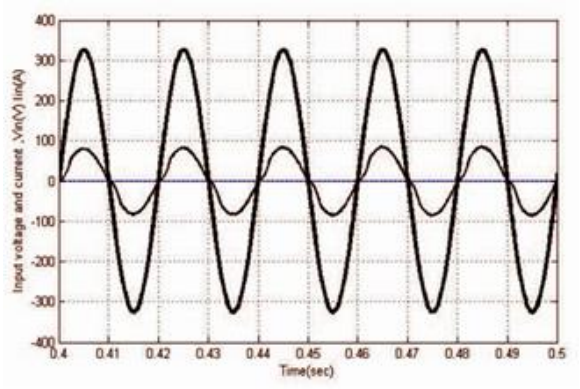
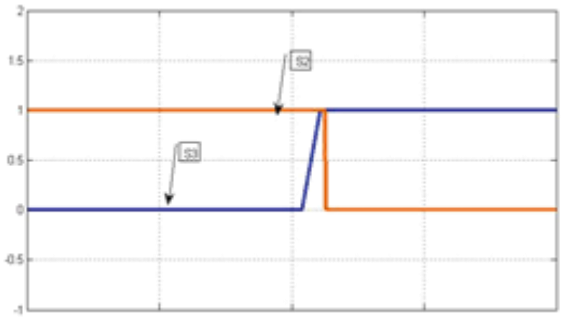
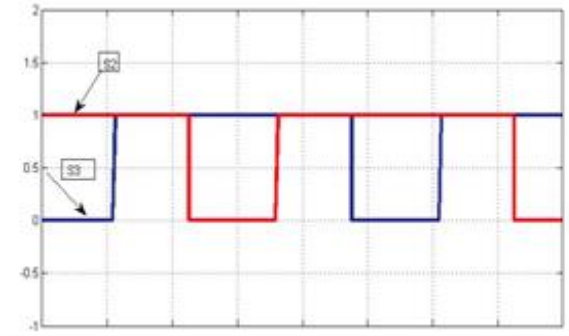


Fig.7.Input voltage and current waveforms with UPF

The maximum and minimum values of the capacitor voltages are observed as 210-1510 volts. For the minimum dead time condition the dc bus voltage is boosted to a very less value.



(a)



(b)

Fig. 8. a) Minimum overlap of S2 and S3. b) Maximum overlap of S2 and S3.

If the dead time and 'm' are adjusted such that switches are overlapped for long time with more turn on period, then the DC bus voltage can be boosted up to several times as that of input voltage.

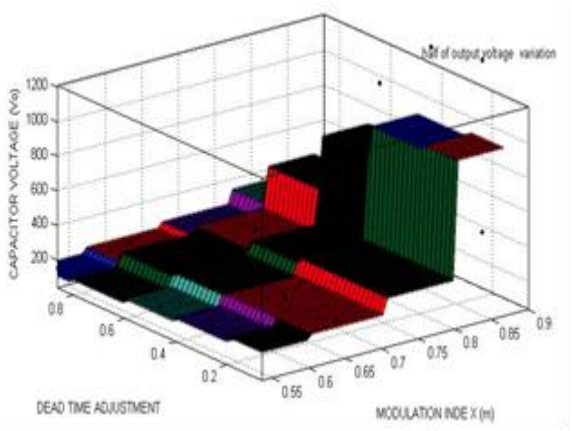


Fig.9 Voltage variation of capacitor with 'm' and dead time.

IV-CONCLUSION

In this paper, open loop AC-AC converter is proposed for high frequency applications. The proposed converter having the single stage conversion which improve the efficiency. Three level variable output voltage is also achieved using boost operation of converter. Thus, the stress across the switches also reduced which increase the life of converter. Simultaneously, the power factor at the source side is also maintained unity. The proposed scheme also utilized the less number of components, hence it is economical. The operations of proposed scheme are validated through MATLAB Simulation results and found satisfactory in different mode of operations.

REFERENCES

[1] Y. Kawaguchi, E. Hiraki, T.Tanka, M. Nakaoka, H Sadakata, A. Fujita and H. Omori, "Feasibility study of a full bidge inverter for induction heating cooking appliances with dicontinuous current mode PFC control," in Proc. IEEE Power Electron. Sepc. Con!, 2008, pp.2948-2953.

[2] H. Shoji, J. Uruno, and M. Isogai, "Induction heating system for all types metal pans employing a method of changing the dc link voltage and the number of turns of the work coli," IEEE Trans. IA, vol. 133, no. 2, pp. 1082-1088 .Nov. 2013.

[3] B. Saha, S. K Kwon, N.A. Ahmed, H. Omori, and M. Nakoaka, "Commercial frequency ac to high frequency ac converter with boost active clamp bridgesingle stage ZVS-PWM inverter," IEEE Trans. Power Electron., vol. 23, no. l, pp.412-419, Jan. 2008

[4] H. Sugimura, H. Muraoka, E. Hiraki, T. Hirota, K. Yasui, H. Omori, H.W. Lee, and M. Nakaoka, " Anovel soft switching PWM power frequency converter with non dc smoothing filter link for consumer high frequency induction heating," IEEE Trans. IA, vol. 125-D, no. 2, pp. 988-999 2005.

[5] N. A. Ahmed, "High frequency soft-switching ac conversion circuit with dual-mode PWM/PDM control strategy for high-power IH applications,' IEEE Trans. Ind. Electron., vol. 23, no. 34, pp. 1440-1448, Apr. 2011.

[6] I. Hirota, H. Omori, and M. Nakaoka, "Practical evalutaions of single ended load-resoant inverter using application- specific IGBT and driver IC for induction –heating appliance," in proc. IEEE Int. Conf. PEDS, Feb. 1995, vol.1, pp,531-537.

[7] O. Lucia, J.M. Burdio, I. Millan, J. Acero, and L.A. Barragan, "Efficiency-oriented design of ZVS half-bridge series resonant inverter with variable frequency duty cycle control", IEEE Trans. Power Electron., vol. 25, no. 7, pp. 1671-1674, Jul. 2010.

[8] H. Sugimura, H. Muraoka, T. Ahmed, S. Chandhaket, E. Hiraki, M. Nakaoka, and H.W. Lee, " Dual mode phase-shifted ZVS-PWM series load resoant high-frequency inverter for induction heating super heated steamer," J. Power Electron., vol. 4, no. 3, pp. 138-151, Jul. 2004.

[9] P. Viriya, N. Yongyuth, and K. Matsuse, "Analysis of two continuous control regions of conventional phase and transition phase shift for induction heating inverter under ZVS and NON-ZVS operation Pichetjamroen," IEEE Trans. Power Electron., vol. 23 no. 6, pp. 2794-2805, Nov. 2008.

[10] J. Jittakort, S. Chudjuareen, A. Sangswnag, S. Naetiladdanon, and koompai, "A dual output

series resonantinverter with improved asymmetrical voltage-cancellation control for induction cooking appliance," in Proc. 37th Annu. IEEE IECON, pp. 2520-2525, Nov. 2011.

[11] H. Sugimura, S.K. Kwon, H. Ogiwara, E. Hiraki, and M. Nakaoka, "A new phase shifted ZVS-PWM controlled full bridge resonant high frequency inverte with auxilary quasi-resonant commutation circuit," in Proc., 4th PCC, pp. 1505-1511 Apr. 2007.