Ananlyis and Design of FIN FET base of ALU

Sushmita Mahan
M.Tech. Scholar, EC Department, faculty of Engineering & Technology, Mandhana Kanpur, Uttar Pradesh, India

***Abstract*- ALU is the core of all microprocessors. It also a combination of logic blocks to perform the logical or arithmetic operations. Now a days ALU is getting more complex and smaller in size to make the development of smaller and most powerful computer systems. This project designs An ALU using MOSFET as a conventional method. In conventional ALU consumes a large amount of power and also consist some limitations during scaling down such as short channel effects, gate dielectric leakage etc. The proposed ALU designed with a FINFET. It has powerful control on short channel effects while scale down the size of the transistor. The design simulation is carried out in TANNER EDA V13.0 version tools. Finally power has been studied and also compared between the ALU designed using MOSFET with proposed FINFET based design of ALU.**

***Index Terms*- FINFET, Leakage Power, Back Biasing, Independent gate circuit.**

I INTRODUCTION

The process of nanometer technology in VLSI is to meet the required performance within the budgeted power. In earlier days, performance of area, accuracy of the design and cost were the primary factors of the VLSI chip designers. Power was the secondary consideration of the circuits. The central processing unit (CPU) is the core of all computers, where the critical building block is ALU. This chapter gives the importance of FINFET in the current VLSI design as well as MOSFET. It also gives the brief introduction of the FINFET and overview of structure.

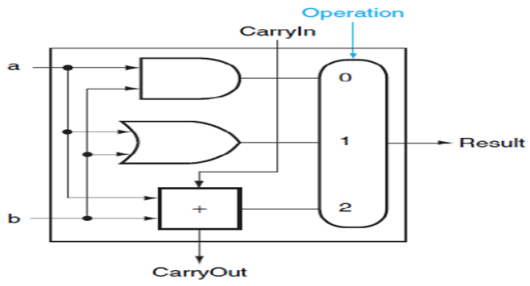


Fig: - Basic structure 1 Bit ALU circuit

1.1 MOTIVATION

"Advancement in the technology VLSI has following the Moor'es law[1.1] where the number of transistor and the density of the component within the chip is doubling in every 18 months" . The transistor size is limited the phenomena of hot carrier and also exponential increment in the electric field which slows down the performance of the device. Scaling is the effective key factor for any new design technology.

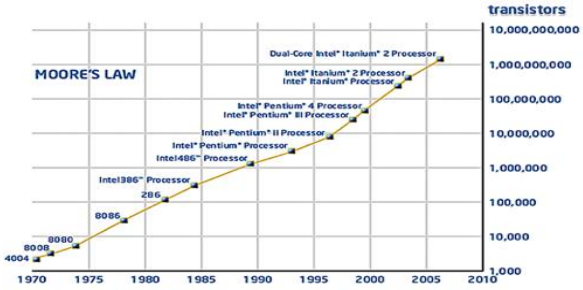


Fig1.1 Moore's law Graph in transistor

The trend in now a days, any electronic devices which are portable, smaller and smarter such as laptops, iphones, mobiles etc. Smarter device is nothing but the devices which are responding fas tly. Also the smaller devices ,it should be in terms of area and cost. To come across the specifications, we should follow from the level of system to the level of circuit.

1.2 BASIC ALU STRUCTURE The basic design of ALU consists of a control unit made up with a multiplexer and the operation unit consist of different kind of operations like and or subtraction addition. A simple design of ALU is shown in Figure 1.1

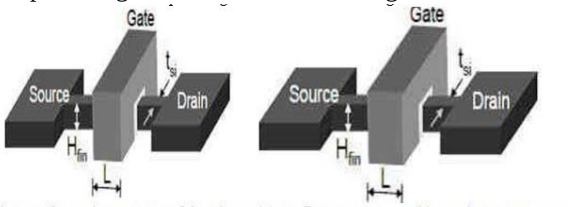


Fig1:- Schematic structure of the FinFet (a) 3T finFet MOSFET (b) 4T FinFet MOSFET

Figure 1.1: 1-bit ALU 1.3 BASIC CMOS STRUCTURE MOSFET are generally categorized into two types, n-type MOS (NMOS) and p- type MOS (PMOS) device .The NMOS device fabrication is carried out on a substrate of p-type also called the bulk or body of the device . It consist of Highly doped two n-regions which forms the source and drain terminals .A piece of polysilicon has not heavily doped which operating as a gate ,and a silicon dioxide (SiO2) with thin layer which seperates the gate and p-type substrate.

The basic diagram for MOSFET as shown in Figure 1.2.Consider a PMOS structure, where the device fabrication is carried on a n-type substrate and consist of not lightly doped two p-regions. The thin SiO2 seperates the gate terminal from the n-type substrate .In MOSFET, the conducting channel is formed between the source and drain region. The complementary manner operation of

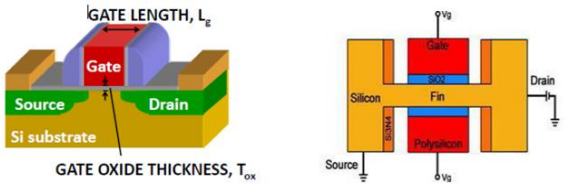
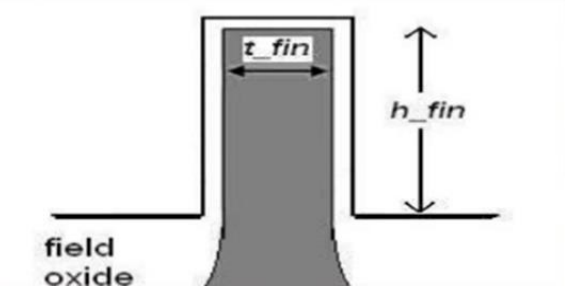


Fig1.3:- Structure of Finfet

The structure of FINFET as shown in Figure 1.3. FINFET transistor technology is a new concept to the VLSI designers. The first FINFET was fabricated a two-gate on a SOI structure as called a single gate transistor. FINFET term was explaining the non planar, two-gate transistor which fabricated on a SOI se most relevant substrate that depends on the basic single gate transistor model. The most relevant characteristics of FINFET that the channel formed between source and drain due to the electron flow conduction is covered with a thin silicon "fin", which implement the body of the transistor. Effective length of the channel is equivalent to the thickness of the silicon fin. In order to raise the channel in FINFET, it used a "fin".



Effective Channel width $w=(t_{fin} + (2* H_{fin}))$ and Effective channel length $=(L_{gate} +(2*L_{ext}))$ shows the effective channel length and width of the FINFET. The gate has a very good control over the carriers presented in the device, if the channel shape is very thin. This shape gives the limitation to flow of current at low level when the device is switched ON. If the back gate of the FINFET is biased with a voltage like non-zero, it gives a result of reduction in the leakage current, with an increment of delay[10].

II.DESIGN IMPLEMENTATION

These days the exponential increment of portable devices required a less power consumption, lesser area and increased speed of operation. As the package density of a chip will increases when the transistors number increases in single silicon chip. The leakage power is increasing where the technology related with CMOS process is reduced. The main aim of device scaling is that reduces the space which is used, increasing the speed of operation and applies a best control to the channel with the configuration of gate. The important factor in any circuit design is the decreased consumption of power. The suitable way of reducing the power in a circuit is to decrease the supply voltage. The leakage current in a gate because of thin tox and the sub threshold leakage current because of small value of vth are the different design factors related with the increasing leakage current. Here the sub threshold leakage current is nothing but the current flows from the drain region to the source region, when the transistors are in off condition. The sub threshold leakage current will also occurs where the transistor threshold voltage is greater than the gate to source region voltage. In a circuit, the gate leakage current is nothing but the flow of current to the substrate from the gate through the insulator layer of oxide[15]. The following sections discuss about the ALU design with existing CMOS structure and proposed FINFET structure.

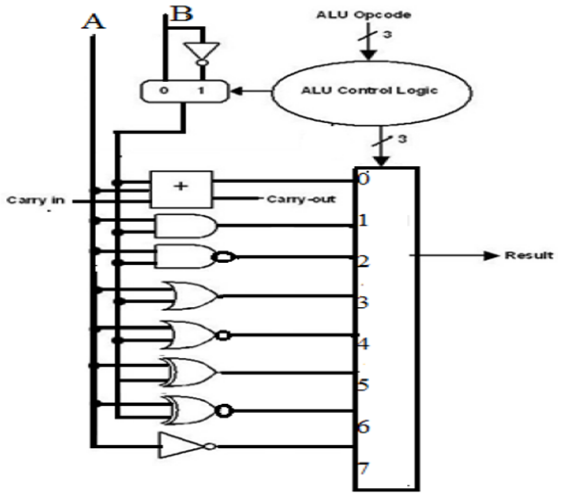
III.ARITHMETIC AND LOGIC UNIT

ALU is the important building block of any digital system design, which gives the arithmetic and logical operation functions. Various bit width of ALU is recently required for in the field of very large scale

integrated circuit design. The enhanced computer and digital processing applications causes to the more demand for low power and high speed operations. In order to get the better performance in signal processing and image processing, the throughput of arithmetic operations should be high. Multiplication, division, addition, subtraction are the major arithmetic operations.

VI. CONVENTIONAL MOSFET ARITHMETIC AND LOGIC UNIT

In conventional method, the 1-bit arithmetic and logic unit is designed using MOSFET with 180nm technology. Here the ALU performs one arithmetic and seven logical operations including addition, AND, NAND, OR, NOR, EXOR, EXNOR and INVERTER. The circuit also consists of an 8:1 multiplexer. The block diagram for a 1-bit ALU as shown in Figure2.The diagram of ALU was designed in the transistor level with MOSFET. The 1-bit ALU diagram generally designed with the help of different circuit modules such as full adder, multiplexer etc.



VI. 1.1 FULL ADDER The full adder circuit is a combinational circuit. This circuit provides the sum output of the three input bits. Generally a full adder circuit includes three input bits and two output bits. The inputs bits are nothing but, it included a one bit for A, one bit for B and one bit for the carry input. The circuits give the two output likes sum and carry out. So the sum gives the results after adding the bits A, B, carry input. Consider a device or circuit consists of more bit of ALU, there it will use carry out as the input of next ALU.

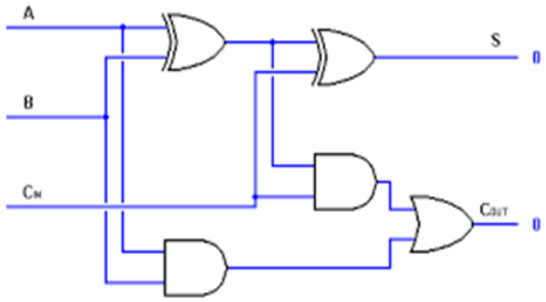


Fig full adder diagram

1.2 MULTIPLEXER Here the ALU control logic is an 8:1 multiplexer. The multiplexer was implemented in the transistor level using MOSFET. It will select the required input for the arithmetic logic unit. Here the 8:1 multiplexer was designed by using 2:1 multiplexer module. The 2:1 multiplexer was implemented with inverter, AND and OR gates in the transistor level. The 2:1 multiplexer diagram is shown in below

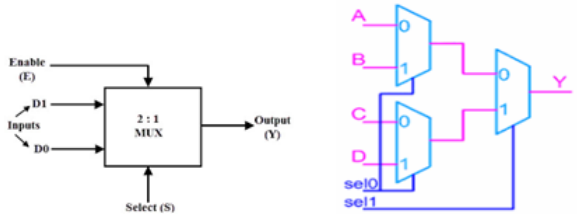


Fig:- (a) 2:1 Multiplexer (b) Circuit Diagram of 2:1 Multiplexer

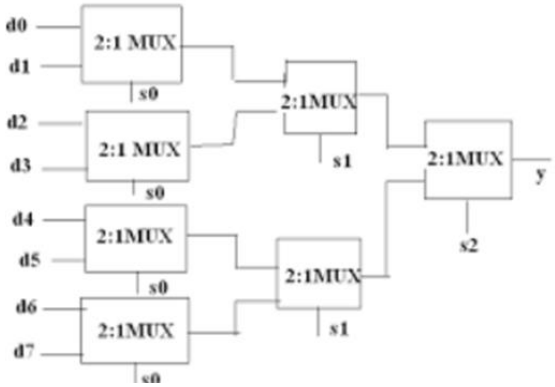


Fig:- 8X1 multiplexer using 2X1 multiplexer circuit.

S2	S1	S0	FUNCTION
0	0	0	ARITHMETIC
0	0	1	AND
0	1	0	NAND
0	1	1	OR
1	0	0	NOR
1	0	1	EXOR

1	1	0	EXNOR
1	1	1	INVERTER

Table2.1(a):- Operation of ALU

When the all select lines s2, s1, s0 bits are equal to zero, then the ALU will perform the arithmetic operation. If the s0 bit is equal to one and other select lines are zero, the ALU will perform the AND operation. According to the Table 2.1(a) the ALU perform the other operation also. In CMOS technology, mainly three factors are causes to the power dissipation, such as static power, dynamic power and short circuit power. The static power will occurs when the circuit is inactive. It is also a "product of the power supply voltage and static or dc current. The static current flow occurs due to the parasitic diodes". The dynamic power is the major factor involved in the power consumption. Dynamic power occurs due to the "charging and discharging of the gate capacitance during switching". So the total capacitance of a gate circuit is the effective part in power consumption. In order to minimize the transistor capacitance, the designer should concentrate on the transistor sizing.

ADVANTAGES AND DISADVANTAGES OF MOSFET ADVANTAGES:

- High noise immunity.
- Does not provide thermal noise
- Allow the logic function with high density in to a chip

DISADVANTAGES:

- Problem with short channel effects during CMOS technology scaling below 32nm
- Difficult to control the leakage current.
- More power dissipation
- Channel is controlled with only one gate
- MOSFET is a planar device, so the current flow is parallel to the wafer. Here the channel is kept on the wafer.

PROPOSED FINFET ARITHMETIC AND LOGICAL UNIT

Due to the scaling limitations in CMOS technology introduced a device with new concept like multi-gate device. Small scaling technology became too difficult in the MOS device. So the designers went to use a FINFET device in their circuit designs. In this project, the existing MOSFET based ALU is replaced with FINFET. The ALU having architecture blocks same as in existing method like arithmetic and logical unit. But the transistor level circuits are different. The FINFET have different modes of operation. In that one of the mode of operation is followed by the ALU designs.

DIFFERENT MODES OF OPERATION

- Short Gate(SG) mode
- Low Power (LP) mode
- Independent –Gate (IG) mode
- Hybrid IG/LP –mode

Short Gate (SG) mode:

In shot gate mode of operation both gate of the FINFET are shorted to get the improved performance like better control to the channel length. The Figure 2.5(a) shows the short gate mode inverter design and Figure 2.5(b) shows the short gate mode NAND gate.

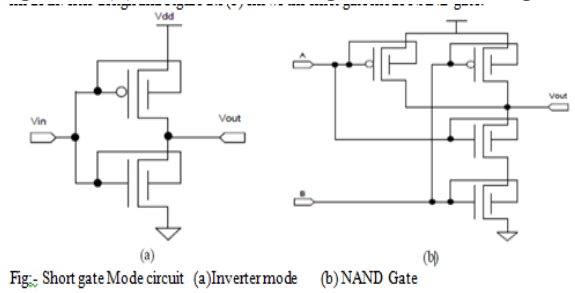


Fig:- Short gate Mode circuit (a)Invertermode (b) NAND Gate

Low power (LP) mode: In this mode a low voltage is applied to back gate of the n-type and a high voltage is applied to back gate of the p-type FINFET transistor. There is a reduction of leakage power dissipation with an increased delay due to the variation of threshold voltage. Figure 2.6 (a) shows the low power mode inverter where the back gate of the p-type transistor is biased with a high voltage like 1V and the back gate of the n-type transistor is biased with a -0.2V .Figure 2.7 (b) shows the Low Power mode NAND gate.

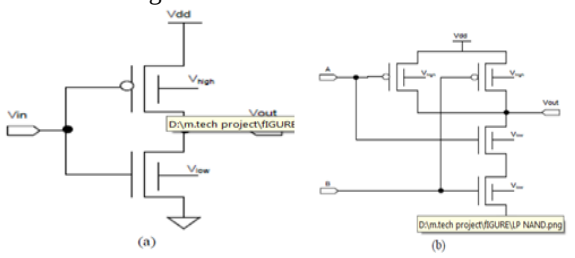


Fig :- Low Power Mode Circuit (a) INVERTER (b) NAND Gate Circuit

Independent –Gate (IG) mode: The two gates of the device is driven by the independent signals. So the number of transistor in the circuit may be reduced. Figure 2.7 (a) shows the independent mode inverter. Figure 2.7 (b) shows the independent gate mode NAND gate. Here only one p-type transistor is used and it is connected with two input signal, one is connected to the front gate and another is connected to the back gate. The n-type transistors are kept in the short gate mode.

Hybrid IG/LP mode: The operation mode is done with Independent mode and Low power mode .As a result, decreased leakage power, less area and increased delay.

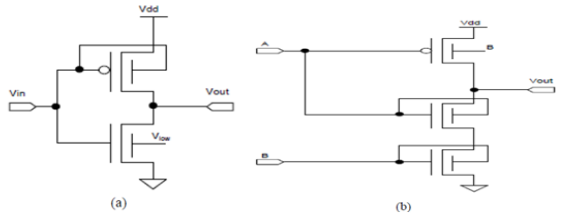


Fig:- Independent Gate Circuits (a) INVERTER (b) NAND Gate Circuit

III. RESULTS

In this project work an ALU is designed using Tanner EDA tool. The ALU is implemented with MOSFET in conventional method. The proposed ALU is designed using FINFET. Power analysis is carried out through the ALU design. Here the ALU implemented with FINFET involves low power compared with MOSFET. Here FINFET is operating with a 0.4V.

A. Complete ALU with MOSFET

Schematic Diagram:

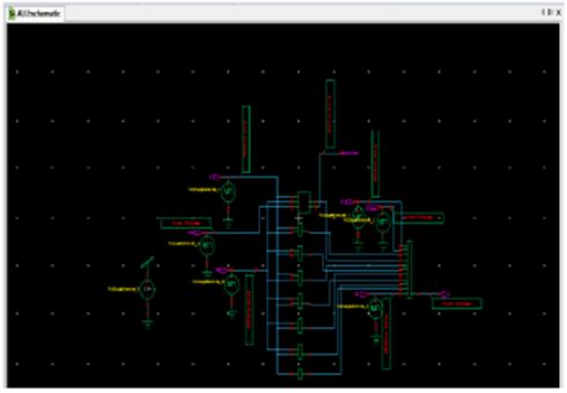


Figure 3.1: Complete Schematic diagram of MOSFET ALU

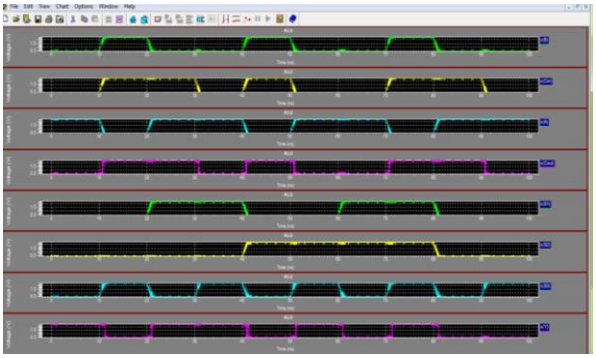


Figure 3.2: Waveform of complete MOSFET ALU

B. Complete ALU with FINFET

The above Figure 3.1 represents the complete ALU schematic diagram. After design the schematic diagram, check for the errors in the design. Then save the schematic design if the errors are corrected properly. Simulate the schematic design using simulator editor and calculate the power from the T-SPICE window.

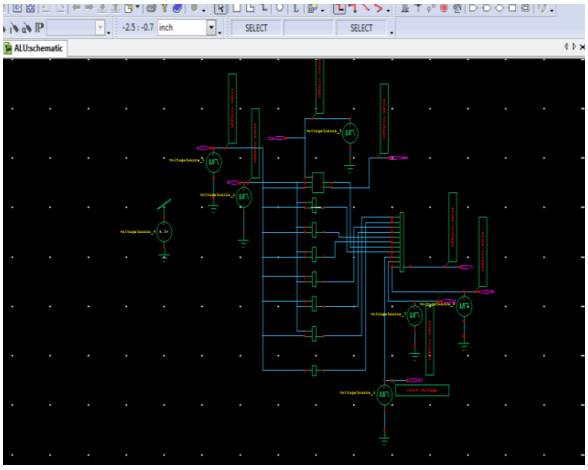


Figure 3.3: Complete ALU diagram with FINFET

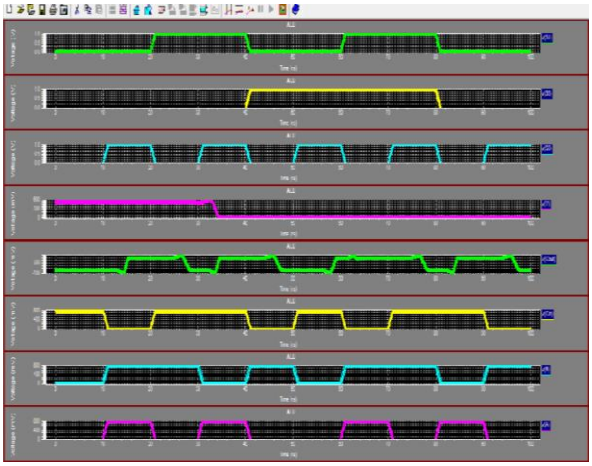


Figure 3.4 : Waveform represents the FINFET ALU

IV.CONCLUSION AND FUTURE WORK

This project designed and implemented an ALU by using FINFET as well as MOSFET. The ALU include the arithmetic and logical operations. It is shown that results obtained for proposed FINFET ALU consumes less power compared with the conventional MOSFET ALU. The ALU designed in 180nm technology and FINFET ALU designed in the SG mode. During scaling process the FINFET design is better to use in the VLSI technology field. The simulation will be carried out using TANNER EDA tools.

REFERENCES

[1] Aqilah binti Abdul Tahrim, Huei Chaeng Chin, Cheng Siong Lim, andMichael Loong Peng Tan,“ Design and Performance Analysis of 1-Bit FinFET Full Adder Cells for Sub threshold Region at 16 nm Process Technology”. Hindawi Publishing Corporation Journal of Nanomaterials Volume 2015.

[2] Anthony Chand. “Cost affective ALU designs that save energy with increased performance”.Department of Electrical and Computer Engineering.University of Central Florida.

[3] Ruchi dantre, Sudha yadav, “Design And Analysis Of Finfet Based High Performance 1-Bit Half Adder-Half Subtractor Cell”.Proceedings of 27th IRF International Conference, 14th June 2015, Chennai, India.

[4] Jency Rubia J, Gopal B.G, Prabhu V ,4-Bit Full Adder using FinFET. “Analysis, Design and Implementation of 4-Bit Full Adder using FinFET”. Journal of Convergence Information Technology (JCIT) Volume 10, Number 2, March 2015

[5] Michael C. Wang, “Independent-Gate FinFET Circuit Design Methodology”. IAENG International Journal of Computer Science, 37:1, IJCS_37_1_06

[6] Ajay N. Bhoj, Niraj K. Jha,“Design of Logic Gates and Flip-Flops in High-Performance FinFET Technology”. IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume:21 , Issue: 11), January 2013

[7] Raj Lakshmi Shukla , Rajesh Mehra“Design Analysis and Simulation of 1 bit Arithmetic Logic Unit on different foundaries”. International Journal of Science and Engineering, Volume 2, Number 1 – 2013,PP:44-53

[8] Akshay Dhenge, Abhilash Kapse, Sandeep Kakde , “Design and Implementation of Area Optimized ALU using GDI Technique”. International Journal Of Innovative Research In Electrical, Electronics, Instrumentation And Control Engineering,Vol. 2, Issue 3, March 2014

[9] Prateek Mishra, Anish Muttreja, and Niraj K. Jha,“FinFET Circuit Design”, Springer Science+Business Media, LLC 2011

[10] Sameer Dwivedi , Dr. Neelam Rup Prakash N, “A Study on Recent Advancements in VLSI Technology using FinFETs”, International Journal of Innovative Research in Science, Engineering and Technology, Vol. 4, Issue 12, December 2015

[11] Girish H, Shashi Kumar D. R “A Survey on the Performance Analysis of FinFET SRAM Cells for Different Technologies, International Journal of Engineering and Advanced Technology (IJEAT)ISSN: 2249 – 8958, Volume-4 Issue-6, August 2015.

[12] Dayadi Lakshmaiah, M.V.Subramanyam , K.Sathya Prasad” Design of High speed Low-Power 1-Bit CMOS ALU” International Journal of Technology and Engineering Science, Volume 2[9], pp: 2284-2287, September 2014.