A Three Phase Interleaved High- Frequency Inverter with Single-Reference Eight-Pulse-Modulation Technique (SREPM) For Fuel Cell Vehicle Applications

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***Abstract*- This paper presents a three phase four leg inverter with neutral connected to load. The inverter hybrid modulation technique consisting of singe-reference eight-pulse-modulation (SREPM) for front-end dc/dc converter and 33% modulation for three-phase inverter. In proposed SREPM to control front-end dc/dc converter, high frequency (HF) pulsating dc voltage waveform is produced, which is equivalent to six-pulse output at 6× line frequency (rectified 6-pulse output of balanced three- phase ac waveforms) and the two more pulses to neutral connection leg. It reduces the control complexity owing to single-reference three-phase modulation as compared to conventional three-reference three-phase SPWM And also the harmonic content in currents. In addition, it relives the need of dc-link capacitor reducing the cost and volume.. It needs only33% (one third) modulation of the inverter devices to generate balanced three-phase voltage waveforms resulting in significant saving in (at least 66%) switching losses of inverter semiconductor devices. At any instant of line cycle, only two switches are required to switch at HF and remaining switches retain their unique state of either ON or OFF. Drop in switching loss accounts to be around 86.6% in comparison with a standard voltage source inverter (VSI) employing standard three- phase sine pulse width modulation. This paper explains operation and analysis of the HF two-stage inverter modulated by the proposed novel modulation scheme. Analysis has been verified by simulation results.**

Index Terms- Electric vehicles, fuel cell vehicles, high frequency, six-pulse modulation, three-phase four leg inverter.

I. INTRODUCTION

Though fossil fuel resources are limited and depleting at an alarming rate, the global demand for oil has increased significantly in recent years. Energy consumed and demanded by transportation sector have risen exponentially due to increasing number of vehicles [1]. Transportation accounts for above20% of the total energy-related emissions [2]. Today most of the world's vehicles are dependent on conventional energy sources. In this regard, alternative solutions for sustainable and green mobility‖ are being researched and implemented by researchers, industries as well as policy makers.

In conventional vehicles, only 10–15% of the fuel energy is converted to traction due to the poor performance of internal combustion engine (ICE). The hybrid electric vehicle (HEV) can boost this efficiency to about 30–40% by increasing fuel economy. HEVs reduce CO2 emission but cannot eliminate completely like electric vehicles (EVs). Major challenge in EVsis energy storage, since energy density of available storing options is small as compared to fossil fuels decreasing the drive range. Another challenge is quick charging of energy storage device [3].

Fuel Cell Vehicles (FCVs) are next generation transportation systems with zero emission to keep the environment clean. FCVs have the potential to significantly reduce dependence on foreign oil. FCVs run on hydrogen rather than gasoline and emit harmful tailpipe emissions that cause the climate change. FCV are efficient and quieter like EVs. FCV is an EV, but the most obvious difference is the fuel cell stack that converts hydrogen gas stored on board with oxygen from the air into electricity instead of direct use of battery to drive the electric motor that propels the vehicle. FCVs are free from driving range and charging time limitations. However, cost, safety, and on board hydrogen storage are the major challenges. FCVs have been tested on road in countries like U.S. (in Chicago), Canada (Vancouver, BC), and Germany, not only cars but local public transportation.

Automotive industries like Honda, Toyota, GM, Ford, and Kia Ria are designing their FCVs [2]. Fuel cell buses are being trialed by several manufacturers in different locations. The fuel cell car market is now in the ramp up phase to commercialization, anticipated by automakers. The primary barriers for this market are cost and infrastructure deployment. The major components of a typical FCV are illustrated in Fig. 1 [1]–[8].

An auxiliary energy storage device is required for start up and for storing the energy captured by regenerative braking EVs/FCVs because present fuel cell technology lacks bidirectional power flow capability [9]. Based on the characteristics and dynamics of fuel cell, optimal energy storage like battery or ultra capacitor is selected [10], [11].

A 12-V battery is used to supply power to auxiliary loads in a vehicle. The same battery can be used with a bidirectional dc/dc converter [12] to complete the aforementioned tasks as shown in Fig. 2. Since the fuel cell stack voltage varies by 100% with change in the fuel flow rate, there is a need for converter to regulate the dc bus voltage (say at 100 V) and power flow [13]–[17].

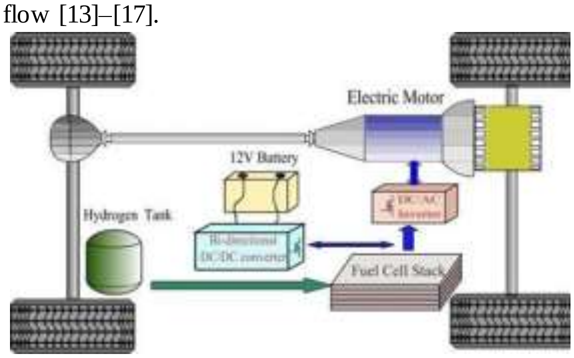

Fig.1. Architecture of a fuel cell car

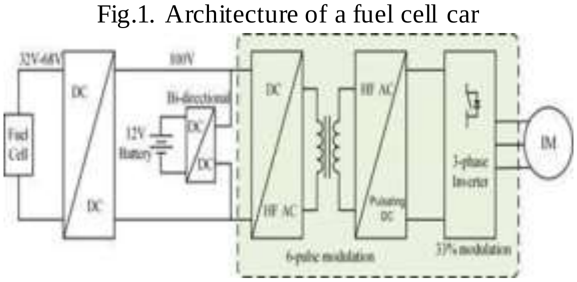

Fig.2. Functional diagram of a fuel cell propulsion system

An HF two-stage inverter is employed to convert 100 V into three-phase ac voltage to drive the ac motor to propel the vehicle and is main focus of this paper.

The single-stage inverter is the simplest topology with least component count and high efficiency. But low voltage fuel cell stack needs a multistage inverter to boost its low voltage to generate three-phase voltage signals [18]. HF modulation is adopted to achieve compact, low cost, and light weight system. Therefore, two stage HF inverter consisting of front-end dc/dc converter followed by a standard three-phase pulse-width modulated (PWM) inverter as shown in Fig. 2 is an alternative solution. This paper proposes a hybrid modulation technique that comprises two different modulations for the two stages. Single Reference Six Pulse Modulation (SREPM) is proposed to control front-end full-bridge dc/dc converter to produce HF pulsating dc voltage having six-pulse information on an average. A single reference signal is used for SREPM implementation. Second modulation is 33% (or one third) modulation adopted for a three- phase inverter that produces balanced three-phase voltage. In 33% modulation, only one leg is modulated at a time. It reduces the average switching frequency and limits the switching losses to 33% of the conventional value. Interleaving does not affect the modulation implementation, or in other words the proposed SREPM is applicable to single full-bridge unit too. Interleaving is shown to improve power transfer capacity. Though a similar hybrid modulation technique for inverter control has been proposed earlier [19], [20], the front-end dc/dc converter essentially has minimum three full bridges employing standard three-phase SPWM with three references. It results in complex control and has major issue of circulating current among the bridges conducted by semiconductor devices. If one bridge fails, the modulation fails, i.e., the pulsating dc voltage does not contain six-pulse information anymore, and hence, the inverter is not able to produce balanced three-phase output. The proposed modulation has unique single reference signal. Even if a bridge fails, the other will maintain six-pulse information in pulsating dc-link voltage and inverter is still able to produce balanced three-phase voltage. It is, therefore, robust and offers higher reliability.

The overall system has the following merits:

1. Elimination of dc-link electrolytic capacitor: reduces volume of system and improves reliability;
2. Reduced average switching frequency of inverter: at any instant of time, only one leg of

inverter is modulated at HF keeping other two legs at same switching state. This reduces the switching losses and improves efficiency. Switching losses are further reduced because the devices are not commutated when current is at its peak.

3. Single reference front-end modulation: A single reference signal is used to implement six pulse modulation to produce pulsating dc voltage at the dc link.

The proposed inverter has better reliability compared to existing topologies owing to single- reference modulation. In [19] and [20], three full- bridges at front-end are used and standard three-phase SPWM is employed that uses three single-phase sine references. Three single-phase HF transformers are connected to compute maximum line-to-line and generate pulsating dc voltage with six-pulse information. Modulations of three full-bridges are mutually dependent on each other to produce pulsating six-pulse waveform at the dc link of the inverter.

In this case, accurate functioning of each front-end full bridge is necessary to maintain six-pulse waveform/information at the dc link and later to obtain balanced three-phase inverter output voltage. From the reliability point of view, failure of a full-bridge results in failure of the system. This is a major weakness of the three-reference modulation demonstrated in [19] and [20].

This paper proposes a single-reference modulation to do the same task, i.e., producing pulsating six-pulse waveform and eight waveforms at the dc link and producing balanced three-phase sine output. Interleaving (two bridges at front-end) is done to increase the power transferring capacity. However, the proposed modulation scheme works with single bridge too owing to single reference approach. Devices at symmetrical location in two bridges are operated by identical gating signals. The novelty and merit of this innovation is unique single reference that is developed to contain information of six-pulse waveform. Since, identical single reference is given to both the front-end bridges, in case of failure of one of the bridges; the other bridge still produces the same six-pulse pulsating waveform at the dc link and then the balanced three- phase inverter output voltage. Therefore, single- reference modulation with interleaved front-end offers

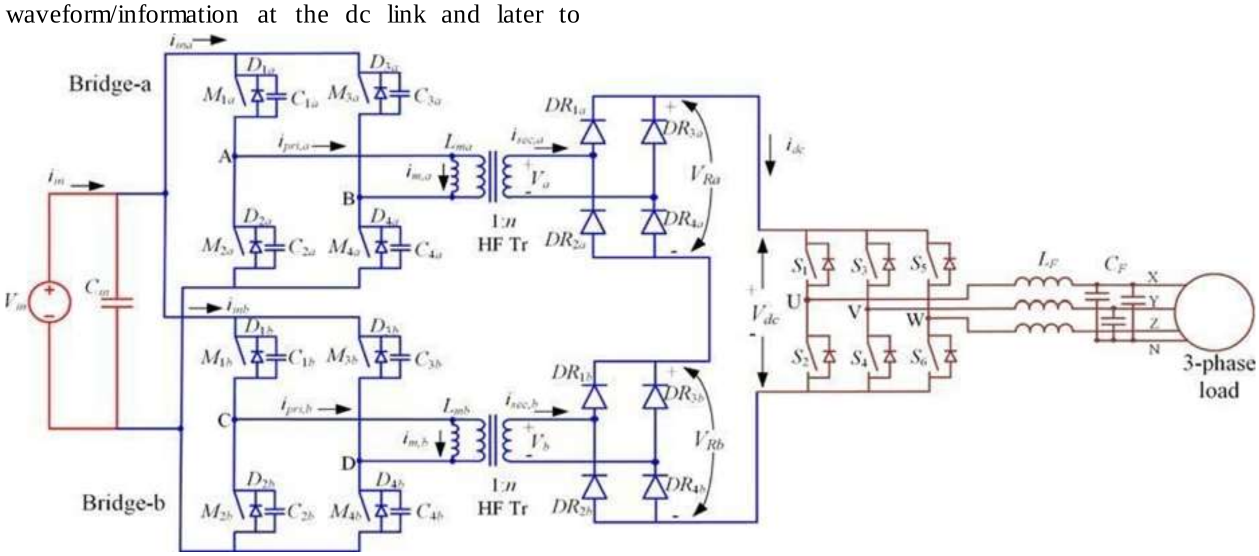

Fig.3. Schematic of the conventional fuel cell inverter system with 3 legs

In addition, the circulating current between the bridges is eliminated. Conventional modulation [19], [20] suffers from circulating current between the bridges (i.e., through semiconductor devices) causing additional losses.

II.OPERATION AND ANALYSIS OF THE CONVERTER

In this Section, steady-state operation and analysis of the modulation technique have been explained. Two full-bridge converters are interleaved at front-end in parallel input series output to increase the power handling capacity as shown in Fig. 3. Both full-bridges are modulated using identical six-pulse modulation producing HF pulsating dc voltage Vdc, which is fed to a standard three-phase inverter.

Modulation of the two stages is planned, developed, and implemented, so as to reduce the switching losses of inverter while making dc link capacitor less. The three- phase inverter is modulated to shape this HF pulsating dc-link voltage to obtain balanced three-phase sine inverter output voltages of required frequency and amplitude after filtering.

The following assumptions are made for easy understanding of the analysis of the converter:

1. All semiconductor devices and components are ideal and lossless.
2. Leakage inductances of the transformers have been neglected.
3. Dc/dc converter cells are switched at higher frequency compared to the inverter.

Therefore, current drawn by the inverter, Idc remains approximately constant over one HF switching cycle of the dc/dc converter. Magnetizing inductances of the HF transformers are denoted as Lma and Lmb in Fig. 4.Higher reliability as compared to that proposed in [19] And [20].

A. Modulation

The switch pairsM1a−M2a andM3a−M4a are operated with complementary signals. The gating signal of M1a and M3a is as shown in Fig. 4.

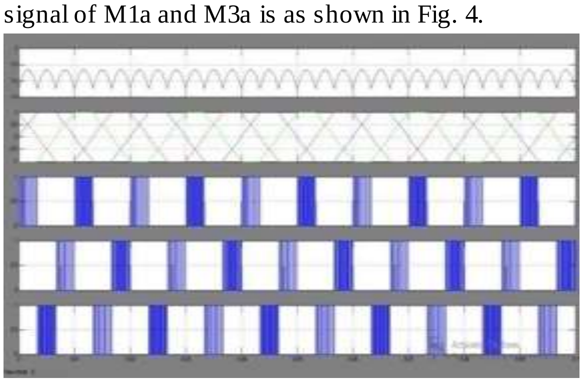

Fig.4. Modulating waveforms for the proposed converter–inverter topology

TABLE-I.MODULATION SIGNALS FOR SWITCHING OF THE INVERTER

	T_1	T_2	T_3	T_4	T_5	T_6
$S_1 \cdot \bar{S}_2$	V_{ab}/V_{cb}	1	1	V_{ac}/V_{bc}	0	0
$S_3 \cdot \bar{S}_4$	0	0	V_{bc}/V_{ac}	1	1	V_{ba}/V_{ca}
$S_5 \cdot \bar{S}_6$	1	V_{cb}/V_{ab}	0	0	V_{ca}/V_{ba}	1

Phase shifted by DTs, where D is defined as the duty ratio of the switch. By varying D, voltage at the rectifier output can be varied linearly. In the proposed modulation, D is generated by comparing reference signal with carrier signal. Reference signal Vref is a six-pulse waveform that is obtained from the rectified output of three-phase line-line voltage as shown in Fig. 4. As the name suggests, the reference voltage is having frequency of 6× ac line frequency. These six equal pulses (segments) are flagged as T1 to T6 and T7 and T8 for compensation leg.

During each of these pulses, only one leg of the inverter is modulated at HF whereas remaining two legs are steady at their switching state. The modulating sequences of the inverter switches S1−S6 are given in Table I, which are compared with carrier waveform to get gating pulses for the devices. During time interval T1, S4 and S5 are ON, and S3 and S6 are OFF. S1 and S2 are modulated at HF by using Vab/Vcb as modulating signal. It can be clearly observed from Fig. 4 that only two (1 leg) of six devices (3 legs) are switched at HF resulting in reduction of number of switching instants in a line cycle

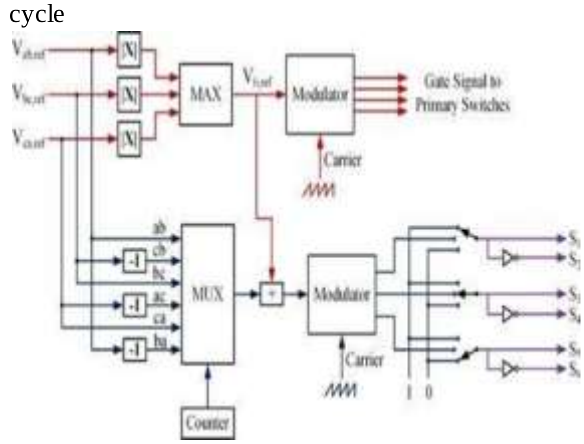

Fig.5. Schematic of complete modulation implementation.

Similar procedure is followed for remaining five segments. In a complete line cycle, each semiconductor device is switched at F only for one third of the line cycle. It is also important to note that the devices do not commutate when current through them is at its maximum value. This further reduces the switching losses lower than 33%. The modulation given in Table-I produce a low harmonic distortion of the output waveforms as compared to previous method given in [19] that gives an unsymmetrical wave shape.

In the proposed method, exact modulating signals are calculated by considering variation in average dc-link voltage in six-pulse fashion. This modulation technique is very easy to implement by using three-phase line–line voltages as references shown in Fig. 5. Six- pulse modulating signal is obtained from maximum of absolute value of three-phase references, i.e., rectification of balanced three-phase sine ac signals. This reference along with the carrier waveform decides gating signals for switches M1a−M4a . Interleaving at front- end is easy to scale the power transfer capacity due to the proposed modulation. Switches are modulated in similar fashion with same value of D.

The modulation given in Table-I is implemented for inverter by selecting modulating signal in the given sequence. Fig. 5 that only two (1 leg) of six devices (3 legs) are switched at HF resulting in reduction of number of switching instants in a line cycle. Similar procedure is followed for remaining five segments. In a complete line cycle, each semiconductor device is switched at HF only for one third of the line cycle. It is also important to note that the devices do not commutate when current through them is at its maximum value. This further reduces the switching losses lower than 33%. The modulation given in Table I produce a low harmonic distortion of the output waveforms as compared to previous method given in [19] that gives an unsymmetrical wave shape.

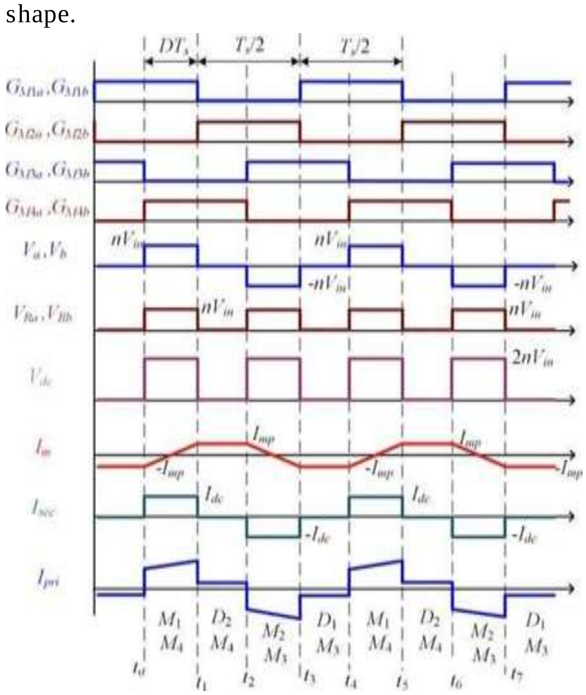

Fig.6. Waveforms showing gating signals, voltage, and current at essential

parts of the full-bridge converter voltage at dc link over a switching cycle is obtained as

$V_{Ra} = V_{Rb} = 2D \cdot n \cdot V_{in}$ (1)

$V_{dc} = V_{Ra} + V_{Rb} = 4D \cdot n \cdot V_{in}$ (2)

Where D is the duty ratio of the converter.

In the proposed method, exact modulating signals are calculated by considering variation in average dc-link voltage in six-pulse fashion. This modulation technique is very easy to implement by using three-phase line–line voltages as references shown in Fig. 6. Six- pulse modulating signal is obtained from maximum of absolute value of three-phase references, i.e., rectification of balanced three-phase sine ac signals. This reference along with the carrier waveform decides gating signals for switches M1a−M4a. Interleaving at front-end is easy to scale the power transfer capacity due to the proposed modulation. Switches are modulated in similar fashion with same value of D. The modulation given in Table I is implemented for inverter by selecting modulating signal in the given sequence.

In the conventional modulation scheme, the duty ratio D is generated from Vref which is a six-pulse waveform. The duty ratio varies between its maximum Dmax and minimum values Dmin for required three- phase output voltages as the Vref varies at 300 Hz. The maximum value of voltage obtained at Vdc corresponds to the peak of line to line inverter output voltage is obtained at Dmax and is obtained as

$V_{XY,peak} = 4D_{max} \cdot n \cdot V_{in}$ (3)

where VXY,peak is the peak of line-line output voltage. Magnitude of output voltage can be varied by varying the reference voltage Vref, which changes the range of operating duty ratio Dmin and Dmax.

C. Switching Losses

As discussed and explained previously, it is clear that devices of the three-phase inverter switch at HF only for 1/3rd of the line cycle. The switch is kept in the on-state for 1/3rd of the cycle conducting the peak current of the output line current when the output power factor is unity and in the OFF state for rest 1/3rd of the line cycle. Similarly, line current is at its negative peak during off-state of the top switch and on-state of the bottom switch. Devices are switching at HF when the line current crosses zero. The total switching loss in the inverter devices Psw, SPM can be analytically calculated as

$$P_{sw,SPM} = 6 \cdot \frac{1}{T_S} \cdot 2 \int_{-\frac{T_S}{12}}^{\frac{T_S}{12}} \frac{1}{6} V_{DC} \cdot i_X \cdot (t_{ON} + t_{OFF}) \cdot f_{SI} dt \tag{4}$$

$$P_{sw,SPM} = \frac{2}{\pi} \cdot V_{DC} \cdot I_X \cdot (t_{ON} + t_{OFF}) \cdot f_{SI} \cdot \left(1 - \frac{\sqrt{3}}{2}\right) \tag{5}$$

where TS is the time period of the three-phase output voltage, VDC is the dc-link voltage during switching which is equal to 4n∗ Vin, iX is the output line current given by IX ∗ sin(wt), tON and tOFF are the on-time and the off-time of the switch and fSI is the inverter switching frequency. Switching losses for standard sine PWM, Psw ,SPWM, are calculated in a similar fashion where all the six devices are switched at HF

$$P_{sw,SPWM} = 6 \cdot \frac{1}{T_S} \int_0^{T_S} \frac{1}{6} V_{DC} \cdot i_X \cdot (t_{ON} + t_{OFF}) \cdot f_{SI} dt \tag{6}$$

$$P_{sw,SPWM} = \frac{2}{\pi} \cdot V_{DC} \cdot I_X \cdot (t_{ON} + t_{OFF}) \cdot f_{SI}. \tag{7}$$

Reduction in switching losses is obtained from (5) and (7)

$$\frac{P_{sw,SPM}}{P_{sw,SPWM}} = \left(1 - \frac{\sqrt{3}}{2}\right) = 0.134 \tag{8}$$

The switching loss in the inverter devices reduces by around7.5 times for the proposed modulation method as compared to the standard sine pulse width modulation (SPWM).

III. DESIGN OF THE INVERTER

In this Section, design procedure is illustrated by a design example for the following specifications: Input voltage Vin = 100 V, output phase voltage VO = 110 V at fO = 50 Hz, rated power Po = 400 W, switching frequency of dc/dc converter fSC = 100 kHz, and of inverter fSI = 40 kHz.

1. Average input current is Iin = Po /(ηVin). Assuming an efficiency η of nearly 95%, Iin = 4.21 A. Each full-bridge is sharing half of the load, Iina = Iinb = Iin /2 = 2.1 A.
2. Maximum value of average voltage at dc link should be above peak value of line–line output voltage Vdc = √ 3 • √ 2 • Vo = 270 V. (9)
3. The turns ratio of the transformers are designed by considering the operating duty ratio of the full- bridge converter as 0.4–0.425. From (2), value of turns ratio n is calculated as
$$n = \frac{V_{dc}}{4 \cdot D \cdot V_{in}}. \tag{10}$$
The turn's ratio of 1.6 is selected allowing safe margin in case of decrease in input voltage below100V. Transformer primary needs to carry current of Iin /2 = 2.1 A.
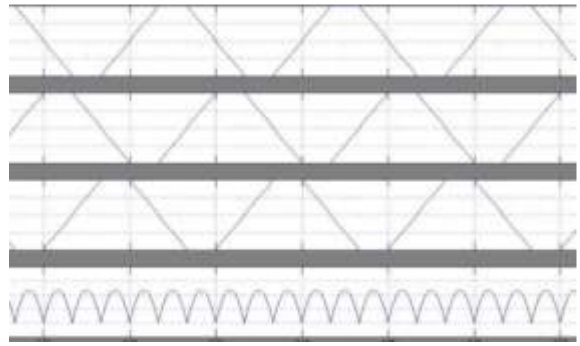
Fig.7.Simulation waveforms showing modulating signals
4. Rating of the full-bridge converter: Switches M1a−M4a and M1b−M4b are rated to conduct current of Iina = Iinb = 2.1 A and rated to withstand voltage of Vin = 100 V.
5. Rectifier diodes have to be able to block a voltage of nVin and current of Idc given by
$$I_{dc} = \frac{P_O}{V_{dc\ min}} \tag{11}$$
Where Idc ~= 1.71 A. Voltage rating of rectifier diodes,
VDR = nVin = 200 V.
6. Inverter circuit: Voltage across inverter switches is selected based on the maximum voltage across dc link, which is equal to 2n × Vin . The RMS current rating of the switches is the same as the output current IO. For the given specification, voltage rating is equal to 400V and current rating is 1.71 A.
7. Filter design: Filter inductance is calculated such that the voltage drop across the inductor is less than 2% of the nominal voltage during the full-load condition
$$L_F = \frac{V_O \cdot 0.02}{2\pi \cdot f_O \cdot I_O} \tag{12}$$
where IO is the output current. For the given specifications, LF is obtained as 10 mH. Filter capacitance is calculated from the cut-off frequency of the low-pass filter.

For this application, one tenth of the inverter switching frequency fSI is selected as the cut-off frequency. Filter capacitor is calculated as

$$C_F = \frac{1}{4\pi^2 \cdot f_C^2 \cdot L_F} \qquad (13)$$

Where fC is the cut-off frequency of the filter. For fC = 4 kHz, the capacitor CF is obtained as 0.16 μF.

IV. PROPOSED THREE PHASE FOUR WIRE NETWORK

In the proposed network topology we are adding another inverter of two switches S7 and S8 (leg 4) to compensate loads with the neutral connected point at inverter as shown in Fig 8.and the control pluses to the switches S7 & S8 as shown in Fig 9.

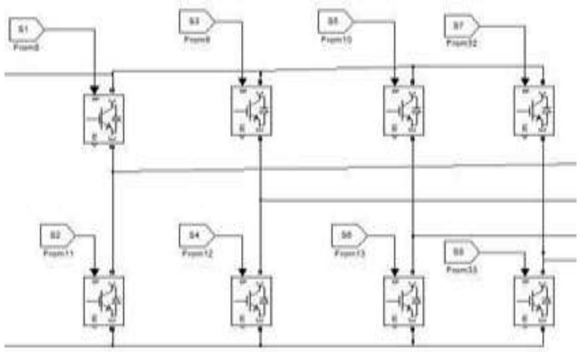

Fig.8.three phase network based inverter

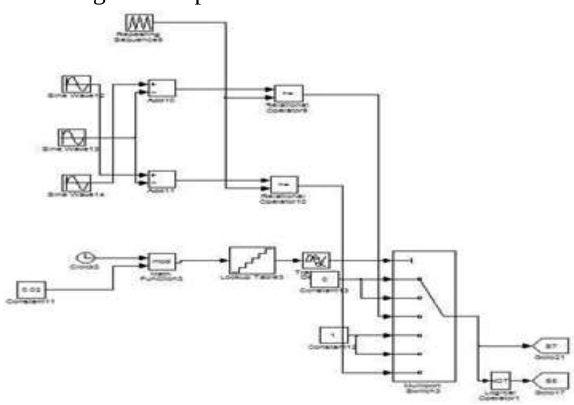

Fig.9.control network for leg 4

V .SIMULATION RESULTS CONVENTIONAL THREE PHASE INVERTER

The conventional modulation scheme has been simulated using MATLAB. Simulation results are illustrated in Figs. 7, Fig 10& Fig 11 matching closely with the theoretical predicted waveforms and results.

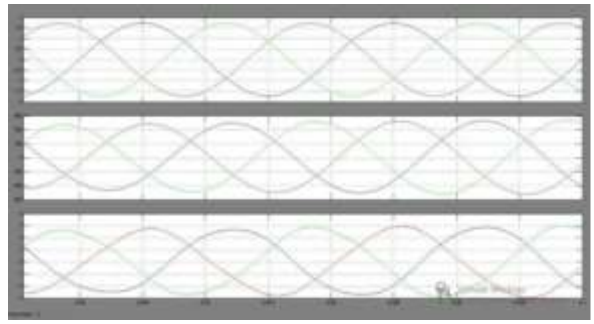

Fig. 10. Simulation results showing references (Vab, Vbc, and Vca), output phase voltages (Vxn , Vyn , and Vzn) and output line current (Ix , Iy , and Iz) waveforms at rated load under the normal operating condition

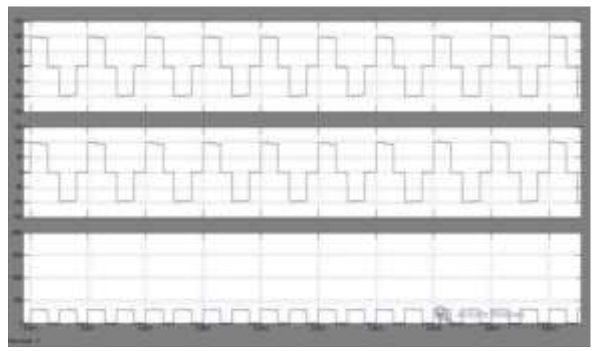

Fig.11. Simulation output showing voltages VAB, VCD, and Vdc at rated load under the normal operating condition.

The modulation for the inverter devices is derived by comparing modA, modB, and modC waveforms shown in Fig. 7 with the carrier signal of 40 kHz. Switches are commutated at HF for only one third of the line cycle resulting in significant saving in switching losses. It is also observed that only one of the legs is switching at HF, remaining two device legs being connected to either Vdc (off) or 0 (on).

In order to generate pulsating dc voltage at Vdc, semiconductor devices are modulated with the varying duty ratio generated from the six-pulse signal, Vref shown in Fig. 7.

The duty ratio of front end converter varies nearly 15% over frequency of 6× line frequency.

Fig. 10 shows three-phase reference voltages used to implement the proposed modulation scheme.

Fig. 10 also presents the balanced three-phase output voltages of 110 V rms that are obtained across the load and the load currents. The LC filter has eliminated HF components resulting in low harmonic contents (distortion) of the inverter output waveforms. SwitchesM1a−M4a andM1b−M4b are controlled using gating pulses that are generated by comparing Vref with the carrier signal. Whenever diagonal switches are conducting, the input voltage appears across the transformers. During remaining time of the HF switching cycle, voltage across the transformers is clamped to zero. Two identical bipolar voltages are obtained at the secondary of the transformers. These two voltages are rectified to obtain unipolar voltage waveforms. The series connected rectifier output voltage is shown in Fig. 11 as explained in the analysis.

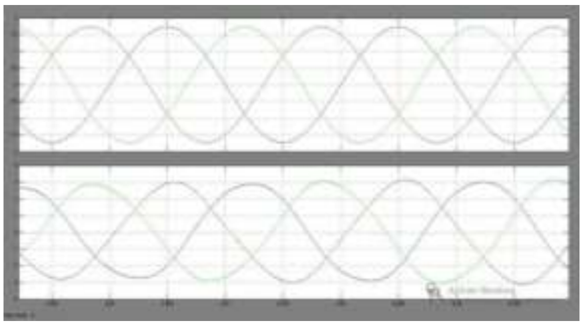

Fig.12. Simulation results showing references (Vab, Vbc, and Vca), output phase voltages (Vxn , Vy n, and Vzn) and output line current (Ix , Iy , and Iz) waveforms if―bridge—b‖ fails at front-end supplying output power 25% of rated load.

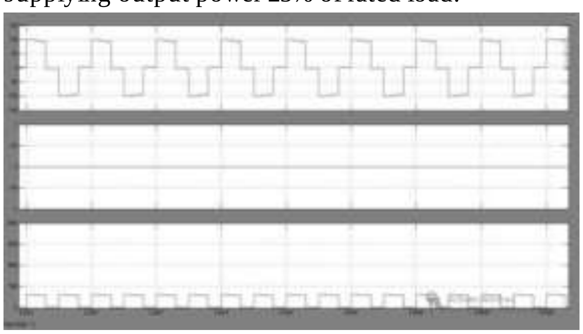

Fig.13. Simulation output showing voltages VAB, VCD, and Vdc if ―bridge—b‖ fails at front-end supplying output power 12.5% of rated.

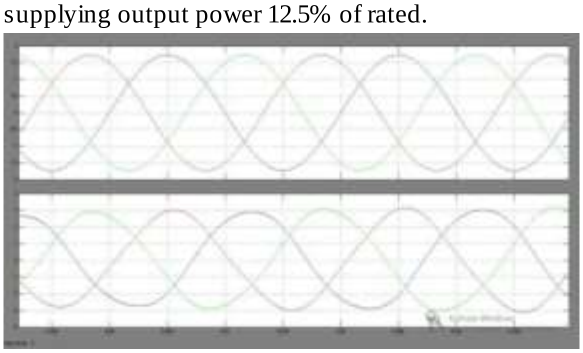

Fig. 14. Simulation results showing references (Vab, Vbc and Vca), output phase voltages (Vxn , Vyn , and Vzn) and output line current (Ix , Iy , and Iz) waveforms if ―bridge—b‖ fails at front-end supplying output power 12.5% of rated load.

Figs. 12 and 13 show the results for power transfer at reduced power if ―bridge—b‖ fails. Fig. 13 clearly demonstrates that the ―bridge—b‖ is not contributing to the power transfer, i.e., VCD = 0 and, therefore, only ―bridge—a‖ is supporting the drive or load, i.e., Vdc = nVAB . Owing to failure of a bridge, the output voltage at dc link Vdc is reduced to half. Therefore, the inverter output or motor input voltage is reduced to half as shown in Fig. 13 and supporting the drive with 25% of the power as shown in Fig. 12 with balanced three-phase output voltages and currents with low distortion. Fig. 14 shows reduced power transfer at lower load, i.e., 12.5%. The balanced three-phase output is obtained even at such a reduced load with distortion.

Single-reference modulation still works with excellence as discussed and explained. It is well known fact that the series inductance or transformer leakage inductance limits the power transfer capacity from input to output or source to load. Theoretically, there is no limit on power transfer if series inductance between source and load is zero provided components design and selection (ratings) is done to withstand it. If the HF transformers could be designed with a very low leakage inductance (negligible or significantly less of the order of nH or <1 μH), then even a single cell would be able to support rated load or nearly rated load.

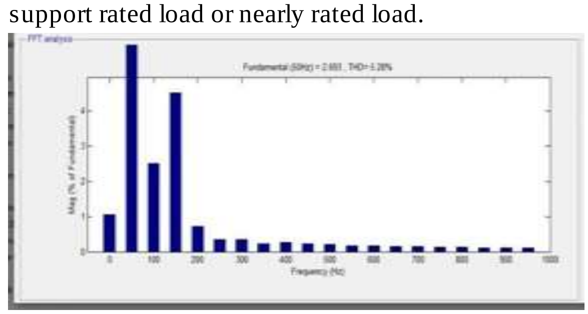

Fig.15.THD at normal load condition

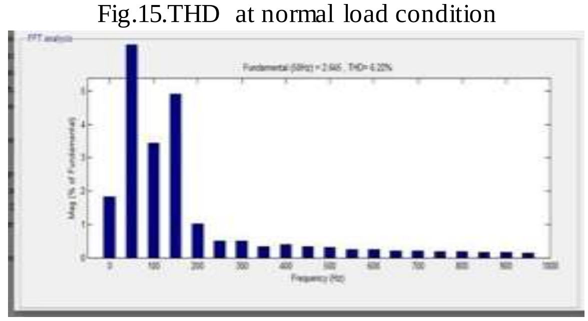

Fig .16.THD Tat 12.5% over load condition

Fig.15 and 16 illuminates the THD levels in the resultant output which is having harmonic content in resultant output currents and voltages. The THD under normal load condition as 5.28 and at the condition of 12.5% over load the THD as 6.22 as shown in Table 2.

PROPOSED THREE PHASE FOUR LEG INVERTER NETWORK

Under normal load condition

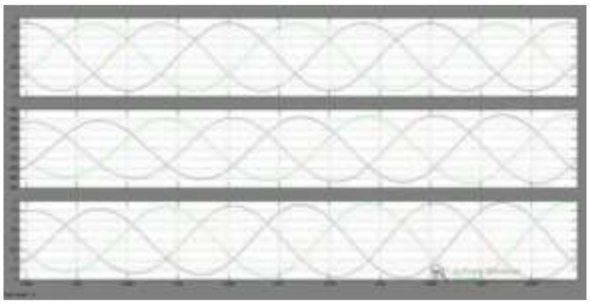

Fig.17. Simulation results showing references (Vab, Vbc, and Vca), output phase voltages (Vxn , Vyn , and Vzn) and output line current (Ix , Iy , and Iz) waveforms at rated load under the normal operating condition

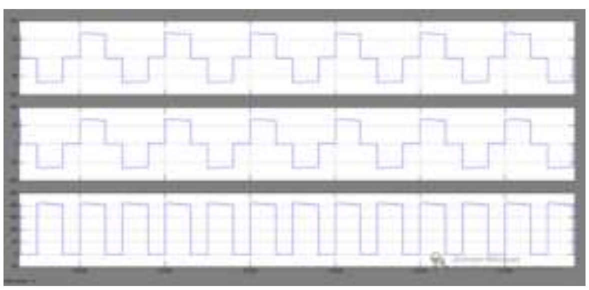

Fig. 18. Simulation output showing voltages VAB , VCD, and Vdc at rated load under the normal operating condition

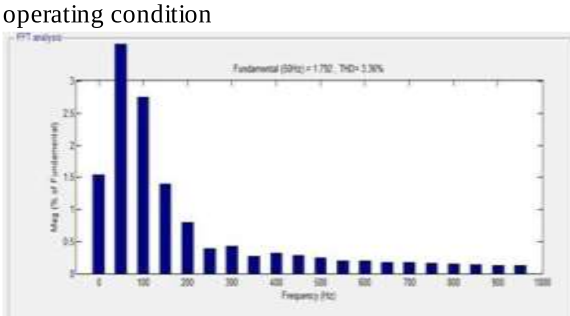

Fig.19.THD at normal load condition

Fig. 20. Simulation results showing references (Vab, Vbc, and Vca), output phase voltages (Vxn , Vy n, and Vzn) and output line current (Ix , Iy , and Iz) waveforms if ―bridge—b‖ fails at front-end supplying output power 25% of rated load.

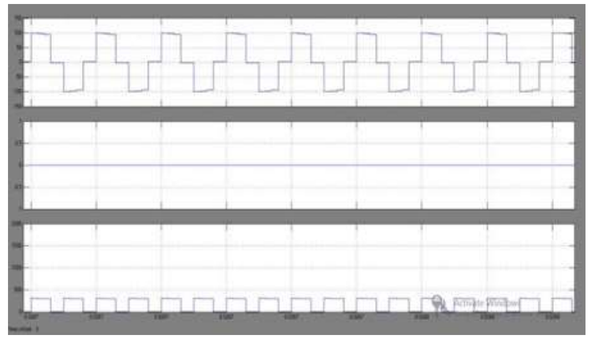

Fig.21. Simulation output showing voltages VAB , VCD, and Vdc if ―bridge—b‖ fails at front-end supplying output power 12.5% of rated

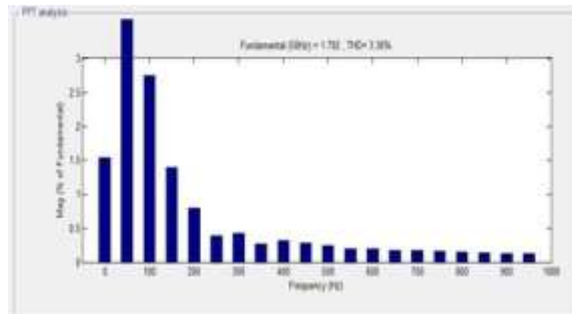

Fig .22.THD at 12.5% over load condition

The THD under normal load condition as 3.36 and at the condition of 12.5% over load the THD as 3.36 as shown in Table 2. Thus even under load variation we have balanced inverter voltages to the loads.

TABLE II THD

inverter scheme	NORMAL LOAD	RATED LOAD
Three leg	5.28	6.22
Four leg	3.36	3.36

VI. SUMMARY AND CONCLUSION

FCVs are becoming lucrative solution toward sustainable low carbon clean mobility owing to zero emission. Volume, cost, efficiency, reliability, and robustness of power electronics are the important attributes of the power electronics system to be addressed. This paper proposes a novel modulation technique named SREPM to control front-end full-bridge converter to generate HF unipolar pulsating voltage waveform at dc link having six-pulse information if averaged at HF cycle over line frequency. Six-pulse is meant for six-pulse waveform that results after rectification of three-phase balanced ac waveforms at 6× of line frequency.

It permits the next three-phase inverter devices to switch at HF during 33.33% (1/3rd) of the line cycle and remains to stay at steady switching state of ON for 33.33% and OFF for rest 33.33% of line cycle. It results in low average switching frequency or 66.66% reduction in switching transition losses and improved efficiency. Compared to three-phase inverter, reduction in switching loss up to 86.6% is accomplished It is suitable for high-power applications like FCVs and EVs, three-phase uninterruptible power supply (UPS), islanded or standalone micro grid, and solid-state transformer.

The proposed modulation technique eliminates the need for dc-link capacitor and feeds directly HF pulsating dc voltage to a three-phase four leg based inverter. This pulsating waveform is utilized to generate three-phase output voltage at reduced average switching frequency (one third of the inverter switching frequency) or 33% commutations of inverter devices in a line cycle. The steady-state operation and analysis of the two stage HF inverter controlled by the proposed modulation scheme have been discussed. Simulation results are presented to verify the proposed analysis.

Under normal operating steady-state conditions, the system does not have effect on fuel cell output current (in case of fuel cell source). Usually, a large ultra capacitor is placed across the fuel cell tack to handle transients to suppress slow fuel cell dynamic response. And the THD of load is reduced from 6.22 to at rated load of 12.5% over load condition hence the four wire network with neutral load balance shown the change in THD of output of inverter at load side.

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