Enhancement of Power Quality Using Hybrid Active Neutral Point Clamped Flying Capacitor Multilevel Inverter

Sujeet Yadav[1], Vivek Kumar Yadav[2]
[1] *M Tech Scholar, Department of Electrical Engineering, SRK University, Bhopal,*
[2] *Assistant Professor, Department of Electrical Engineering, SRK University, Bhopal*

***Abstract*- Multilevel inverters have been widely accepted for high-power high-voltage applications in this paper presents the hybrid cascaded active neutral-point-clamped (ANPC)-based multilevel converter. This paper proposes a new seven –level hybrid topology combining features of neutral point clamped and flying capacitor inverters. This paper presents the seven level inverter with harmonics reduction. Multilevel converters are the attractive solution for medium and high-power applications. For medium voltage inverters, cascaded H-bridge (CHB), neutral point clamped (NPC) and flying capacitor (FC) are the primary topologies. Among them, ANPC and FC provide a common dc link which is a strict requirement for many applications. The proposed topology provides a tradeoff between different component counts to achieve a good loss distribution, avoid direct series connection of semiconductor devices, keep the balanced operation of dc-link capacitors while keeping the number of costly components such as capacitors and switches low. The required modulation strategy is developed and the operation of the proposed topology is studied in this paper. For medium voltage applications verify the performance of the converter by using the simulation results. Experimental results from a low-power laboratory prototype are presented that verify the operation of the hybrid converter under SHE-PWM.**

Index Terms- cascaded H-bridge (CHB), Neutral point clamped (NPC), Flying capacitor (FC)

INTRODUCTION

A multilevel inverter is a power electronics converter is recently applicable for high voltage and high power application such as flexible AC transmission system (FACTS) and AC motor drives [3]. Also, power electronics technologies have provided an important improvement in the renewable energy application. In recent year the multilevel inverter has gained due to some advantages in lower switching loss, high voltage capability and lower harmonics [1]-[3]. In several topologies for multilevel inverter have been proposed; the diode-clamped [4], [5], flying capacitor [6], and cascade H Bridge [7] structures. In high power, applications that require high voltages and high currents the maximum ratings of power semiconductors become a real handicap. The series connection of power switches is the solution for dealing with larger voltages. Nevertheless, achieving static and dynamic voltage sharing among those switches becomes a problem, which led to the development of the new family of multilevel converters. On the other hand, paralleling of subsystems is the solution for dealing with larger currents. If more than three phases are used to deliver power to the load then the per-phase current rating is lower and low-current devices can be used. As a consequence, multiphase multilevel converters are good candidates to be used in high-power drive applications. Nevertheless, this advantage comes at the price of a greater complexity in the inverter and in an increased control difficulty. The number of devices that must be controlled goes up from the only six switches of the two-level three-phase converters to the tens of switches of multiphase multilevel converters. At present, there are no commercial digital signal processors (DSPs) having enough appropriate built-in pulse- Using Hybrid Active Neutral Point Clamped

Flying Capacitor Multilevel Inverter provide significant advantages over the typical two-level converters such as improved output waveforms with less harmonic distortion, less electromagnetic interference, reduced stress across the semiconductor

switching devices, and fault-tolerant operation [1]. However, the increase in the number of levels comes at the cost of increased complexity of the topology and increased component count, including switches, capacitors, and isolated dc sources. An increase in the number of levels further complicates the implementation, requiring voltage balancing of capacitor and neutral point voltages [2], [3]. The three-level neutral-point-clamped (NPC)-based converters are the most widely used in industrial applications [4]. The three-level active NPC (3L-ANPC) can deal with the uneven distribution of semiconductor losses inherent to the NPC converter [5]. Some of the popular multilevel configurations are the neutral point clamped (NPC), series-connected H-bridge, flying capacitor, etc. Although they can be configured for more than two levels, as the number of levels increase, the power circuit and control complexity due to a large number of devices increases. An optimum topology for multilevel inverters for more than three levels has not been achieved until now, and research is going on to improve the drive efficiency at reduced circuit complexity and control. In NPC multilevel inverters [1]–[7], the load current drawn from the neutral point will cause an unequal voltage sharing between the series-connected capacitors. This will introduce unwanted harmonics in the inverter output voltage and also results in an unequal voltage stress on the switching devices. To avoid this problem, special voltage balancing techniques must be implemented [2], [5]–[7], or isolated voltage sources have to supply each series-connected capacitors. Although a scheme is proposed in [8] that allow the NPC three-level inverter to operate with unbalanced capacitor voltages, it increases the control-circuit complexity due to the 3-D space-vector arrangement. In cascaded H-bridge (CHB) multilevel inverter structure [9]–[10], the H-bridge cells are supplied from individual dc source and are series connected to generate multilevel voltage profile. As the number of levels increases, the CHB requires a huge number of isolated voltage sources. In a flying-capacitor topology [2], more number of levels in the phase voltage is generated by adding or subtracting the capacitor voltages. It requires additional control and increased switching for maintaining the capacitor voltages constant. The power circuit and control complexity increases when the number of levels increases in the output voltage. The generalized multilevel inverter topology is presented in [13]. This topology is a combination of NPC and flying-capacitor inverter topologies. However, it requires additional capacitor banks and many active switches to generate a multilevel output voltage. A hybrid asymmetric multilevel inverter topology is proposed [14], by connecting a flying capacitor in series with the NPC inverter. In order to eliminate the need for individual dc sources for every converter stage and extend the number of levels of the conventional multilevel inverters, hybrid cascaded converter topologies with H-bridge cells have been proposed. A topology based on the cascaded interconnection of a two-level inverter with individual H-bridge cells for each phase was presented in. An asymmetrical converter based on the cascaded connection of the three-level NPC converter and H-bridge cell for medium drive applications using model predictive control was also proposed in [3]. A carrier-based pulse width modulation (PWM) control was implemented in [14] and [15] to control the voltage across the flying capacitors (FCs) in a cascaded connection of the three-level NPC converter and H-bridge cells. This converter only requires a single dc source for all the three phases. The cascaded connection of the three level NPC converter and H-bridge cell was proposed for current waveform conditioning in [16] and [17]. However, this scheme is not valid for the entire operating range of the drive (with respect to the power factor and modulation index). A dc-voltage-ratio control strategy for single-phase two-cell CHB converter with a single dc source is presented in [15]. However, this scheme is based on the elimination of switching states which tend to make the floating capacitor voltage unbalanced. Therefore, this scheme cannot be operated for the full modulation range using any arbitrary dc-voltage ratios (i.e., the ratio between the dc source voltage and floating-capacitor voltage).Moreover, if this scheme is extended to a three-phase system, then it requires three isolated voltage sources. Other arrangements of hybrid multilevel converters include the 3L-ANPC converter with an H-bridge cell [18] (Fig. 1), the four-level ANPC converter with a stacked multi cell converter [19], the 3L-ANPC converter with a two-level cell [18]–[19] which is known as five-level ANPC converter, and power electronic building block with five-level ANPC

converter [18]. For a given switching frequency, selective harmonic elimination PWM (SHE-PWM) offers the potential for improved waveform quality compared to other existing modulation techniques (Sinusoidal and space vector PWM). This potential becomes advantageous for applications where low switching frequency is required. The 3L-ANPC converter under SHE-PWM has been studied in [15], while the extension of the method to the five-level FC-based ANPC converter was presented in [16]. Hybrid multilevel converters are derived from various combinations of similar or different converter topologies. The objective of this paper is to discuss the operation of a multilevel converter based on the cascaded interconnection of a 3L-ANPC converter and individual H-bridges for each phase. The configuration of the circuit is shown in Fig. 1. In this

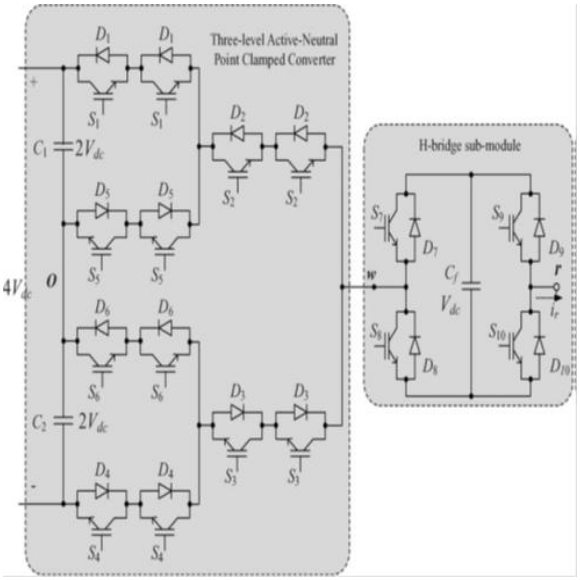

Fig. 1. Circuit configuration of the hybrid Seven-level ANPC-based multilevel converter

Paper, the hybrid seven-level cascaded ANPC-based multi-level converter operational principles are utilized in order to regulate the voltage across the H-bridge floating capacitor under SHEPWM. The effects and limitations in the voltage regulation of the floating capacitor for various loads and modulation indices under SHE-PWM are also analyzed. Moreover, the extension of the modulation index range, where the charging and discharging periods of FC are varied to enhance the voltage regulation of FC, is considered.

LITERATURE SURVEY

Sridhar R. Pulikanti et. al. [1] "Hybrid Seven-Level Cascaded Active Neutral-Point-Clamped-Based Multilevel Converter under SHE-PWM" in this proposed the hybrid seven-level cascaded ANPC-based multilevel converter under SHE-PWM has been analyzed in this paper. The topology is based on the cascaded connection of a 3L-ANPC converter and individual H-bridge sub modules for each phase of the converter. This configuration offers control of the switching losses across the ANPC switches and provides regulation of the voltages across the floating capacitors. The presented utilization of the converter extends the operation range of converters with similar dc-link voltage, while the SHE-PWM provides elimination of low-order harmonic and maintaining the low switching frequency of the power switches. A variable hysteresis band based on the analysis of the floating capacitor voltage ripple is considered to minimize additional switching in the converter. The performance of the topology, together with the voltage regulation strategy under SHE-PWM technique, is validated through simulation results and verified in a low-power laboratory prototype for a number of operating points and loading conditions.

Roozbeh Naderi et. al. [2] "A New Hybrid Active Neutral Point Clamped Flying Capacitor Multilevel Inverter" in this proposed A new hybrid 5-level inverter topology and modulation technique is proposed. Compared to 5-level ANPC as the most similar topology, this new topology requires two less switches at the cost of an additional capacitor and six diodes. However, since the capacitors still see the switching frequency and their size remain the same, it is expected to reduce the inverter's total cost. Also, unlike 5-level ANPC, all switches must withstand the same voltage which eliminates the need for series connection of switches and associated simultaneous turn on and off problem. Good loss distribution among switches can increase the inverters rated power or provide higher switching frequency and smaller capacitor size.

Javier Chivite-Zabalza et. al. [3] "Voltage Balancing control in 3-Level Neutral-Point Clamped Inverters Using Triangular Carrier PWM Modulation for FACTS Applications" in this projected has presented a novel technique to balance the voltage of the two split dc capacitors of a 3-L neutral-point clamped inverter, suitable for reactive power compensation, when triangular carrier PWM modulation is

employed. It consists in injecting a squared waveform at six times the supply frequency. Subsequently, it has been compared with two already known strategies based on the injection of a negative-sequence second harmonic and a sinusoidal sixth harmonic waveform. The contribution of current to the inverter midpoint of these techniques has been analyzed as a performance measure. Subsequently a small signal averaged model, suitable for control design purposes has been presented and a control strategy has been proposed. Finally, these techniques have been evaluated both in simulation and in a 690-V ac, 120 kVA experimental setup when supplying both a balanced and an unbalanced inductive load. The results conclude that, although the three techniques are valid, second harmonic injection has a major effect in balancing the inverter midpoint and the even harmonics that it introduces are negligible and only present during transients. However, out of the two sixth harmonic injection methods that do not produce even harmonics at the inverter output, the proposed squared waveform technique is preferred, as it has a slightly greater compensation effect on the dc midpoint and is easier to implement, particularly, in systems employing a low modulation index.

Anshuman Shukla et. al." Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multilevel Inverter" in this proposed A flying-capacitor-based chopper has been proposed for dc capacitor voltage equalization in a DCMLI. It requires additional power semiconductor devices and capacitors but of reduced voltage rating compared with the conventional chopper.

Two configurations of this topology, named as three-level and four-level choppers, are analyzed for generalization purposes. These are different in capacitor and semiconductor device count and correspondingly reduce the device voltage stresses by half and one-third, respectively. The working principles and control schemes for these circuits have been presented. It has been shown that, by preferentially selecting the available redundant chopper switch states, the dc-link capacitor voltages can be efficiently equalized in addition to having tightly regulated flying-capacitor voltages around their references. The various operating modes of the chopper are described along with their preferential selection logic to achieve the desired performances. Simulation and experimental results obtained have verified the viability and effectiveness of the voltage-balancing circuit and control, even in transient states. This proposed topology is expected to be more reliable, loss efficient, and able to enhance the ride-through capability of the inverter system, and these features need to be investigated further.

K. Siva Kumar et. al. "A Hybrid Multilevel Inverter Topology for an Open-End Winding Induction-Motor Drive Using Two-Level Inverters in Series With a Capacitor-Fed H-Bridge Cell" in this proposed the concept of open-end winding structure has been extended by adding a capacitor-fed H-bridge cell in series with the motor phase winding. This results in a five-level inverter topology. It does not require any clamping diodes as in a conventional five-level NPC inverter. It requires only one capacitor bank for each phase, whereas the five level flying-capacitor topology requires six additional capacitor banks with a voltage rating of Vdc/4 for each phase. Therefore, the proposed topology reduces the power circuit complexity compared with NPC or flying-capacitor topologies. In case of any switch failure in the H-bridge cell, the proposed inverter topology can be operated as a three-level inverter for full modulation range (by appropriately clamping the H-bridge cell). Inherent H-bridge capacitor voltage balancing eliminates the need for additional dc-power supplies and hence, increases the reliability of the power circuit and also reduces the power circuit complexity. In case of any failure in inverter 1 and inverter 2, this topology can be operated as a three level inverter in lower modulation index. The proposed five level inverter topology has been experimentally verified for the full modulation range, on a 5-hp IM drive, for steady-state as well as transient conditions using V/f control.

METHOD

The proposed topology includes a dc-link that is common among three phases. The dc-link provides three voltages levels +3E, 0,-3E for the phase legs. Since phases have similar configuration, only one phase of the proposed topology has been shown in fig.1.All the additives shown in the discern have equal working voltage E which has one sixth of the dc-link voltage Vdc. The flying capacitors CA1, CA2, CA3, CA4 are controlled to stay charged Vdc.

The flying capacitorsCA1, CA2, CA3, CA4 controlled to stay charged at the target voltage E. The cascaded ANPC-based multilevel converter is an arrangement of a 3L-ANPC converter stage and an H-bridge stage which are connected in series as shown in Fig. 2.

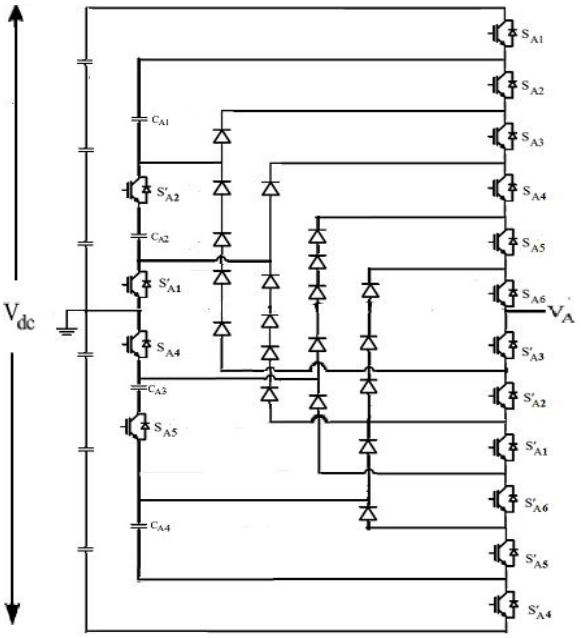

Fig. 2. A phase leg of the proposed 7-level hybrid topology

The dc link consists of capacitors C1 and C2 providing the midpoint required for the 3L-ANPC converter. Considering a dc-link voltage of 4Vdc, each dc-link capacitor voltage is maintained to an average of 2Vdc, and the voltage of the H-bridge sub module capacitor (Cf) is maintained at a voltage equal to Vdc. The active switches (S5 and S6) of the ANPC converter clamped to the neutral point ensure the equal voltage sharing between the main switches (S1–S4) and also create additional zero-voltage level switching states. These redundant switching states can be utilized in order to distribute the semiconductor losses of the 3L-ANPC converter.

The modulation methods used in multilevel converters can be classified according to switching frequency. Methods that work with high switching frequencies have many commutations for the power semiconductors in one cycle of the fundamental output voltage. The popular methods for high switching frequency methods are classic carrier-based sinusoidal PWM (SPWM), and space vector PWM. The popular methods for low switching frequency methods are space vector modulation (SVM) method and selective harmonic elimination method. A very popular method with high switching frequency in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to increase the effective switching frequency. Therefore, the harmonics in the load voltage can be reduced.

A multilevel SHE-PWM strategy is considered, assuming both quarter- and half-wave symmetries. The formulation of the SHE-PWM problem and acquisition of solutions for seven-level waveforms has been analyzed in . The equations describing the seven-level SHE-PWM are given in (1) for the fundamental frequency component and in (2) for the higher order harmonics

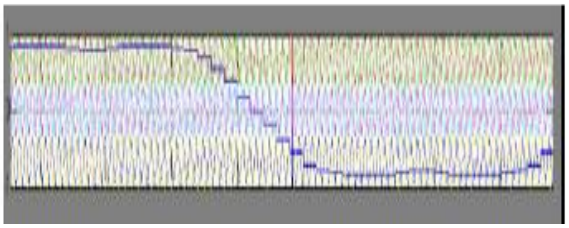

Fig. 3. Carrier-based modulation using modified PSC with sampled CSVPWM reference for three phase application.

$$\sum_{i=1}^{N_1}(-1)^{i+1}\cos(\alpha_i)+\sum_{i=N_1+1}^{N_1+N_2}(-1)^{i}\cos(\alpha_i)+\sum_{i=N_1+N_2+1}^{N}(-1)^{i+1}\cos(\alpha_i)=M \quad \text{.....(1)}$$

$$\sum_{i=1}^{N_1}(-1)^{i+1}\cos(n\alpha_i)+\sum_{i=N_1+1}^{N_1+N_2}(-1)^{i}\cos(n\alpha_i)+\sum_{i=N_1+N_2+1}^{N}(-1)^{i+1}\cos(n\alpha_i)=0 \quad \text{.....(2)}$$

Where N1 is the number of switching's between the zero and the first level, N2 is the number of switching's between the first and the second levels, N3 is the number of switching's between the second and the third levels in the quarter period of the waveform, M is the modulation index, and αi is the ith switching within the quarter period of the waveform. The additional restrictions imposed are

$0 \leq M \leq 3$ (3)

$0 < \alpha_1 < \alpha_2 < \alpha_3 < \cdots\cdots\cdots < \alpha_N < \pi/2$ (4)

and the amplitude of the fundamental component is

$$\hat{V}_1 = \frac{4.M}{\pi} \times V_{dc} \quad (5)$$

COMPARISON WITH OTHER TOPOLOGIES

The 7-level NPC has low switch count but the major problems are unbalanced operation of dc link capacitors, poor loss distribution among switches, and excessive number of diodes. 7-Level FC provides low switch count and excellent loss distribution but requires high number of flying capacitors that can adversely affect the initial cost, maintenance and replacement surcharges, and reliability of the inverter. The proposed topology presented in this paper provides a trade-off between different components counts to achieve good loss distribution avoid direct series connection of semiconductor devices, keep the balanced operation of dc-link capacitors while keeping the number of costly components such as capacitors and switches as small as possible.

CONCLUSION

In the Present Work, performance of cascaded Seven level inverter using hybrid pulse width modulation technique has been analyzed. The topology used in this technique reduces the number of power switches and switching losses. In the Cascaded H-bridge multilevel inverter is popular in the multilevel inverter family. Out of various PWM techniques level gives a good harmonic performance. The modified PWM technique has also been developed to reduce switching losses. Also, the proposed method can reduce the number of required power switches compared to the cascaded multilevel inverter. From the FFT analysis we get minimum THD of 256.93% and the fundamental frequency 7.567Hz shows performance of the cascaded hybrid five level inverter. The simulation results show that this hybrid five level inverter topology can be applied for high power applications. Thus the proposed method will reduce the cost, and also used only 6 switches, harmonic reduction and the heat losses. The hybrid seven-level cascaded ANPC-based multilevel converter under SHE-PWM has been analyzed in this paper. The topology is based on the cascaded connection of a 3L-ANPC converter and individual H-bridge sub modules for each phase of the converter.

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