Performance Analysis of Three Phase Cascaded Multilevel Inverter

Darshana Khedkar[1], Dr. P.V. Thakre[2]
[1]*PG Student Scholar, Dept. of EEE, SSBT'S College of Engineering & Technology, Jalgaon, M.H, India*
[2]*Professor, Dept. of EEE, SSBT'S College of Engineering & Technology, Jalgaon, M.H, India*

***Abstract*- In this paper, a modular cascaded H-bridge multilevel inverter for single-phase and three-phase renewable applications has been described. HCMMLI (Hybrid Cascaded Modular Multilevel Inverter) is one of the useful power electronic interface strategy for PV system The primary operation of single phase module and the cascaded hybrid inverter has been explained in this paper. The operation of symmetrical mode has been analyzed. The Nearest Level Control method of multilevel inverter topology is discussed. With this topology, less number of switches could be used which reduces switching losses and harmonic distortion. The size and cost of the system is reduced with the reduced power switches. In this paper, the main focus is on utilization of above discussed topology for several H Bridge configuration with equal and unequal magnitude of DC source. This configuration are considered to be symmetrical and asymmetrical. Here, in order to find an optimum arrangement with high quality output voltage, the comparison of symmetrical, binary asymmetrical and trinary asymmetrical topologies are analyzed.**

Index terms- Nearest Level Control (NLC), Total harmonic distortion (THD)

I. INTRODUCTION

High performance of ac drive systems require high quality inverter output with low harmonic contents. Conventional two level inverters require high switching frequency to obtain a quality output voltage waveform. In high power and high voltage applications, these two level inverters, have some limitations in operating at high frequency. Harmonic reduction by raising switching frequency of two level inverter is difficult. From this aspect Multilevel (begins with three level) approach is promising alternative. [1]

Multilevel inverter plays a major role for development of power in renewable energy source. In renewable energy source the photovoltaic system efficiency is around 40%, to increase the efficiency and output voltage of the system the Switch Mode DC Power Supplies (SMPS) and Multilevel Inverter are utilized. In Inverter there are two types single inverter and Multilevel inverter. Comparison of SI with MLI, it produces a 'n' number of output voltage, less Electromagnetic Interference (EMI) and less Total Harmonic Distortion (THD). In MLI there are three types Neutral Point Clamped (NPC) MLI, Flying Capacitor (FC) MLI and Cascaded H Bridge (CHB) MLI. In MLI the cascaded Inverter is utilized in research attention than FLCMLI and NPCMLI due to their circuit simplicity and modularity. [7]

In CHBMLI topology consists of sub multilevel converter unit (SMCU) and full bridge cascaded Inverter. If the DC source are equal provided to the Inverter is said to be Symmetrical. If the DC source are unequal provided to the inverter are said to be Asymmetrical. In Symmetrical configuration, the output voltage levels are less when compared to the Asymmetrical. In Asymmetrical configuration the output voltage levels are increased and result in reduced harmonic content and improved resolution in output voltage waveform.[1] The main conception of multilevel inverter (MLI) is to achieve higher power by using number of power switches with several low voltage dc sources. It can produce output voltage waveform in steps which is closer to sine wave and reduces total harmonic distortion. Important points regarding topological structure of multilevel inverter are:

- It should have less switching devices as far as possible.
- It should be capable of enduring very high input voltage such as HVDC transmission for high power applications.

- Each switching device have lower switching frequency to multilevel approach.

Recently multilevel inverters have been used in applications like distributed generation, adjustable speed drives, flexible ac transmission system,, HVDC, electrical vehicles etc. due to noticeable advantages like high quality output voltage using low switching frequency, low harmonic contents, low electromagnetic interference, less voltage stress on power switches, more efficiency and low dv/dt stress on load.[7] The proposed Hybrid Cascaded Modular (HCM) MLI is constructed from modified H-bridge module and T-type three leg inverter structure (TTL). Three sources are needed to produce the aforementioned levels in the output in each module. To design each module, this is not effective approach of MLI to have more sources. Two capacitors and one DC source are employed to reduce one source. A charge balance control method is employed for the voltage balance between two capacitors and to have this control method, the switching states must have a redundancy where the switch count may increase. The proposed HCM MLI has ability to operate in both symmetrical and asymmetrical modes. [9]

II. SYMMETRICAL CASCADED H-BRIDGE INVERTER

The proposed multilevel inverter which has fundamental square comprises of two DC voltage sources. A similar voltage is connected in two voltage source then it is said to be in symmetric mode. Be that as it may, If the voltage source given is observed that as it may, to be diverse that is it is working in awry method of operation. The six semiconductor switches which are associated with the anti-parallel diode forms the square. By inductive attributes of load, 8 diodes which are utilized for conduction of in reverse current is additionally present.[6]

As part of this circuit, the semiconductor switches utilized is IGBT. The circuit shown in fig1. comprises of different squares used for the different levels of operation. The two positive, two negative and zero voltage levels have been obtained by turning the switches on and off in the correct sequence. The redundancy in switching state can provide average power control according to the proper switching of devices, can be calculated using equation. [3],[9].

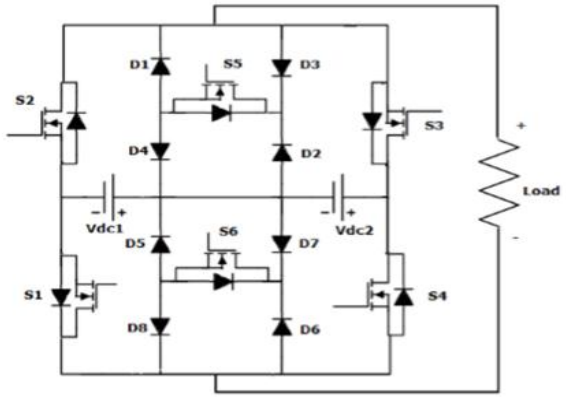

Fig 1: Symmetrical Cascaded H Bridge MLI using R-Load

III. ASYMMETRICAL CASCADED H-BRIDGE INVERTER

To produce more number of output levels, asymmetrical multilevel inverter is used without increasing the number of cells. According to geometric progression with a factor of 2 or 3, the magnitude of dc voltages sources can be chosen. The generalized multilevel inverter is constructed from the connection of the basic block in series and connection of blocks which leads to the increase in number of levels. [6] It has the capability to produce 13 levels in the output voltage side because of the two basic blocks are connected in series and is going to operate in asymmetric mode of operation. In this proposed method, the various DC voltage sources are given and the values are determined using the equation to reach the required output voltage levels in the circuit. [9]

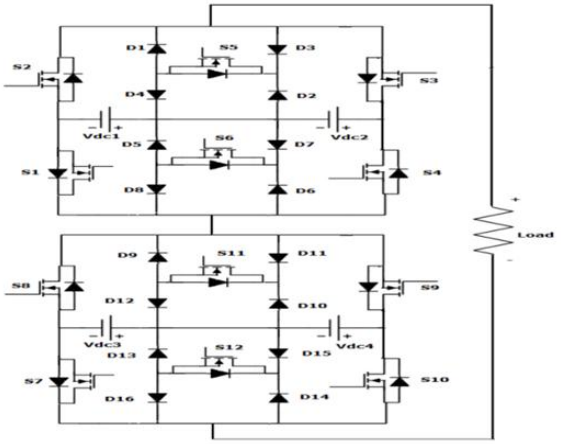

Fig 2: Asymmetrical Cascaded H Bridge MLI using R-Load

Table-1: Asymmetrical CHB-MLI

Binary Asymmetric CHB-MLI	Trinary Asymmetric CHB-MLI
Voltage sources are in the ratio 1:2	Voltage sources are in the ratio 1:3
Value of dc voltage source $V_k = 3^{(k-1)}Vdc$ $k = 1, 2, \ldots\ldots m.$	Value of dc voltage source $V_k = 3^{(k-1)}Vdc$ $k = 1, 2, \ldots\ldots m.$
No. of output voltage levels $n = 2^{(m+1)} - 1$	No. of output voltage levels $n = 3^m$
Maximum voltage generated. $Vm = (2^m - 1)Vdc$	Maximum voltage generated. $Vm = \frac{(3^m - 1)}{2}Vdc$

IV.COMPARISON BETWEEN SYMMERICAL AND ASYMMERICAL CASCADED H BRIDGE MULTILEVEL INVERTER

It is observed that as compared to symmetrical and binary asymmetrical structure, trinary asymmetrical multilevel inverter can produce more voltage levels and higher maximum output voltage with the same number of bridges. Table 2 shows comparison when m number of cells are connected in series which based on the number of levels (n), number of switches (Ns), dc sources (Nd) maximum output voltages (VM) and number of variety in voltage magnitudes (Nv), total voltage blocked by switches (Vb). [9]

From table 2, comparison of binary asymmetrical and trinary asymmetrical and symmetrical cascaded hybrid multilevel inverter, we obtained the results with standard formulae.

Table-2: Comparison of Symmetrical and Asymmetrical CHB-MLI

Binary Asymmetric CHB-MLI	Trinary Asymmetric CHB-MLI
Voltage sources are in the ratio 1:2	Voltage sources are in the ratio 1:3
Value of dc voltage source $V_k = 3^{(k-1)}Vdc$ $k = 1, 2, \ldots\ldots m.$	Value of dc voltage source $V_k = 3^{(k-1)}Vdc$ $k = 1, 2, \ldots\ldots m.$
No. of output voltage levels $n = 2^{(m+1)} - 1$	No. of output voltage levels $n = 3^m$
Maximum voltage generated. $Vm = (2^m - 1)Vdc$	Maximum voltage generated. $Vm = \frac{(3^m - 1)}{2}Vdc$

The switching tables are used for the generation of switches in multilevel inverter circuit. PWM technique is the pulses used for activation of turn on and turn off process of the switches used in inverter. The two main advantages of PWM are the control amplitude and fundamental frequency output voltage with decreasing the filter requirements to reduce the harmonics. In order to create a sinusoidal output voltage in a single phase inverter, the switches must be controlled in a definite sequence and for this a reference sinusoidal waveform is required. The reference waveform is known as the modulation or control signal. The problem of the switching sequences is that they produce a lot of harmonics. The problem can be overcame if PWM techniques can be used instead of switching sequences to produce sine waves with better quality so that it resembles the ideal sine wave more closely. There are several PWM techniques that can be applied for operating multilevel inverters. These techniques are basically of two types: level shifted pulse width modulation (LS-PWM), and phase shifted pulse width modulation (PS-PWM). There are different schemes to implement the carriers: in-phase disposition (IPD), phase opposite disposition (POD), alternate phase opposite disposition (APOD), and phase shifted carrier (PSC). Different types ofthesecarrierschemesareshowinFig.8. In this paper, level shifted in-phase disposition (LS-IPD) PWM is used. In general, for n-level inverter (n-1) phase shifted carrier signals are required. The phase shift between carriers are governed by the following equation $\varphi = 180^\circ$ m (9) where m is the number of h-bridge used in a multi-level inverter. For 5-level inverter driver by phase shifted carrier, 4 phase shifted carrier waves are required and the phase shift between two consecutive carriers is 90 degrees. To overcome the problem PWM techniques.[1]

V. NEAREST LEVEL CONTROL MODULATION

The Nearest level control (NLC) or Round method is low switching frequency control technique leads to reduction in switching losses. The proposed topology of cascaded H-bridge adopts the NLC method. This method uses the nearest voltage level which is used by converting to the desired output voltage reference. With the comparison of the reference waveform with the existing output voltage with level count L,

sampled waveform is processed. Since, the power signal and the load requirement is sine wave, the reference signal is sinusoidal. The sinewave signal is quantized with reference to required levels then the reference signal is quantized or rounded to amplitude division of N. Then the rounded signal is transferred to the pulse generator to generate the pulses. All this operational approach is illustrated in Fig. 3. [4]

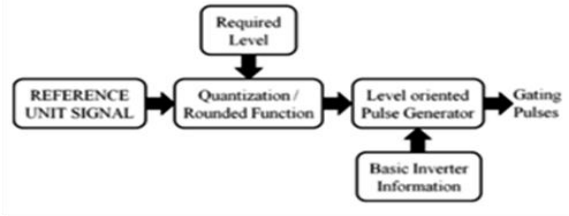

Fig. 3. Logical approach of NLC Modulation

VI. SIMULATION RESULTS

In this paper, MATLAB/SIMULINK is used the nine level inverter circuit and results of output voltage and THD are shown in figure.

Table 3. SIMULATION PARAMETERS

No.	Parameter	Value
1	MHB Module	1
2	Capacitor in one module	2200 µF
3	Switching Freq.	3khz
4	Modulation Index	1
5	Load (R – L) per	126Ω, 120mH

A) Nine level Inverter MHB Model

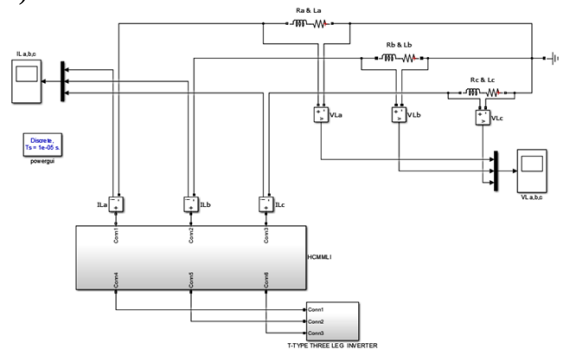

Fig. 4. Nine level Inverter Simulink Model

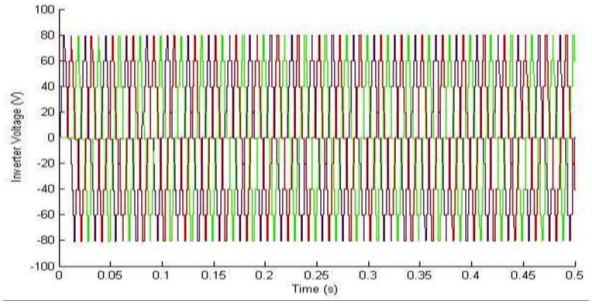

Fig.5. Simulink Output waveform of nine level Inverter

In this paper, the simulation result of MHB module is shown in figure 5.

In figure 4, four level switching scheme with 1 modulation index level shifted PWM is shown.

In figure 4, 100 V voltage with R – L load level are generated as per switching table 3.

B) Single Phase Nine Level MHB Inverter

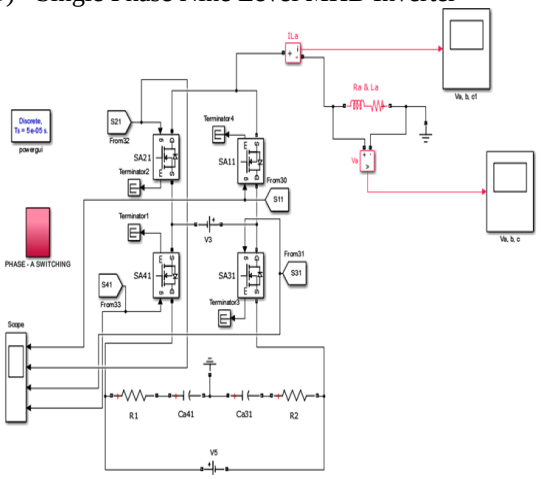

Fig.6. Simulink Model of Single Phase Nine Level MHB Inverter

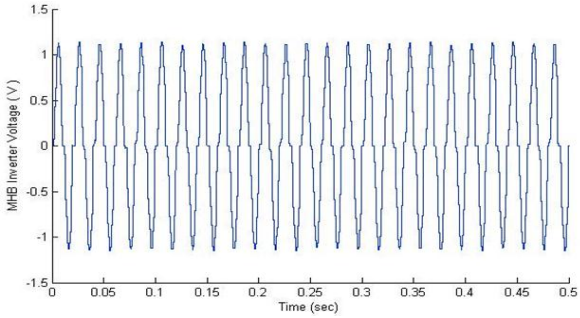

Fig.7. Output voltage waveform of Single Phase Nine-level MHB Inverter

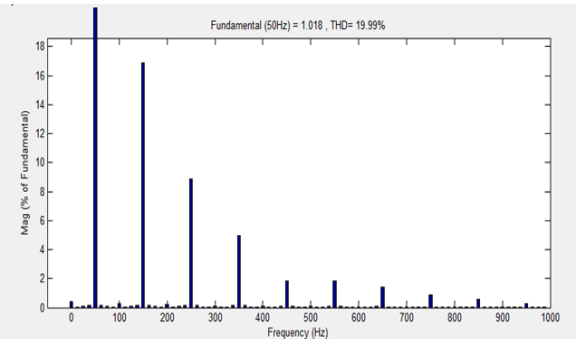

Fig.8. THD value of Single Phase Nine Level MHB Inverter

C) Single Phase Nine Level TTL Inverter

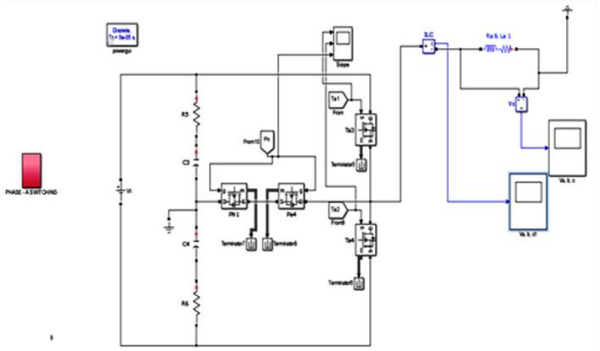

Fig.9. Simulink Model of Single Phase Nine Level TTL Inverter

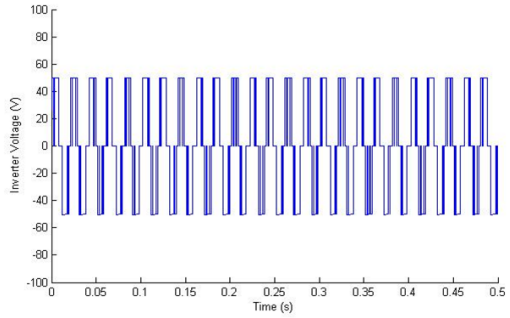

Fig.10 (a). Output voltage waveform of Single Phase Nine-level TTL Inverter

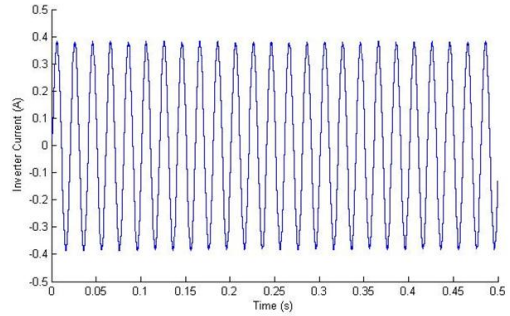

Fig.10 (b). Output current waveform of Single Phase Nine-level TTL Inverter

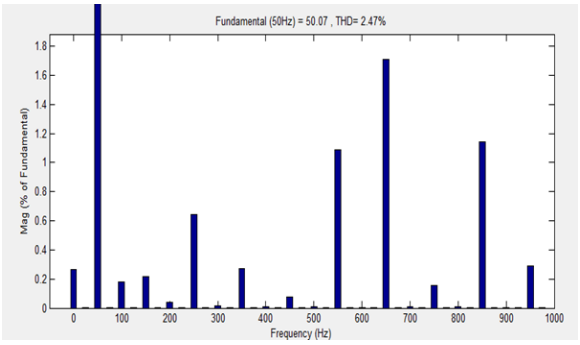

Fig.11. THD value of Single Phase Nine Level TTL Inverter

D) Three Phase Nine Level Inverter

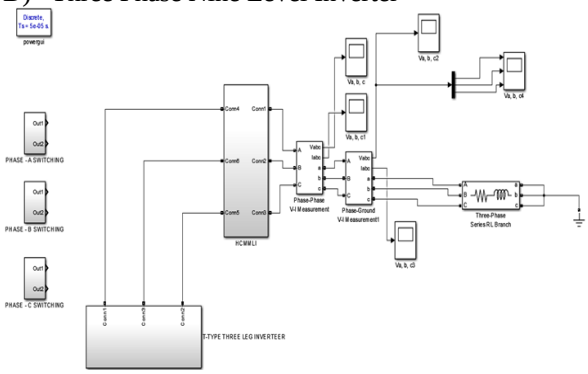

Fig.12. Simulink Model of Three Phase Nine Level Inverter

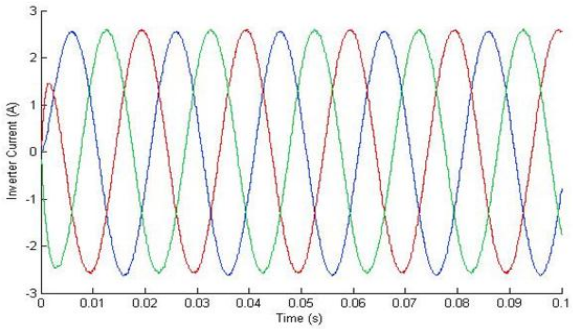

Fig.12 (a). Sinusoidal Current waveform for three phase nine level inverter

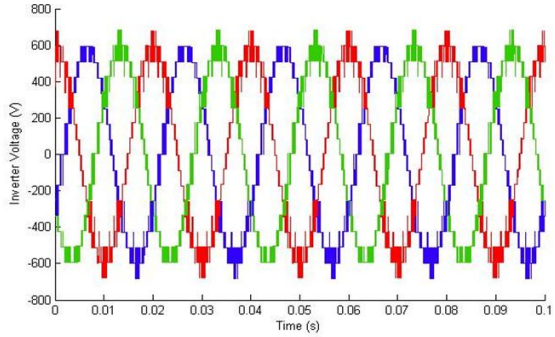

Fig 12 (b). Phase to phase voltage waveform three phase nine level inverter

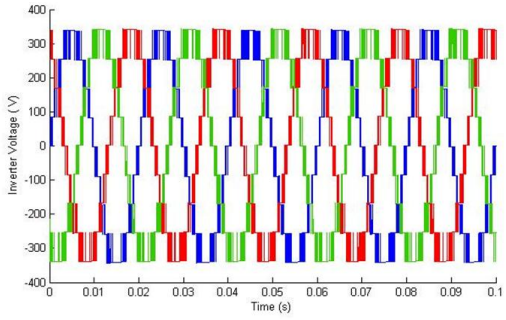

Fig 12 (c). Phase to ground Voltage waveform three phase nine level inverter

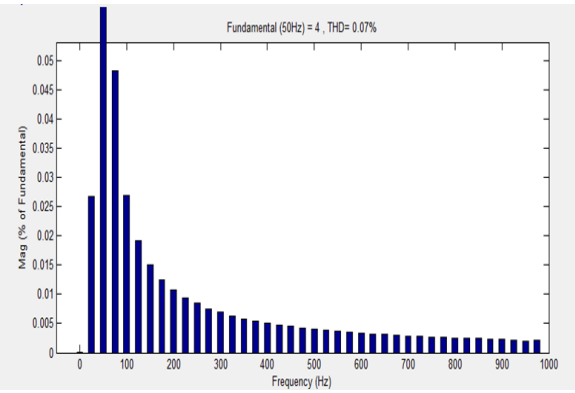

Fig.13. THD value of three phase nine level inverter

VII. CONCLUSION

In this paper, the single phase nine level MHB multilevel inverter, single phase nine level TTL inverter and three phase nine level inverter is discussed. From this paper, the simulation results of single phase nine level inverter and three phase nine level inverter is observed. The simulation of 9-level cascaded H-bridge is studied and observed with it's harmonic analysis. The simulation results shows that the developed nine-level Cascaded H-bridge multilevel inverter has many merits such as reduce number of switches, lower EMI, less harmonic distortion and the THD. Also, it is concluded that THD value of single phase nine level MHB inverter is 19.99% and THD value of single phase nine level TTL inverter is 2.47%. It is also concluded with the THD value of three phase nine level inverter which is reduced to 0.07 %.

Also, in this paper detailed study of Nearest Level Control for multilevel inverter is discussed. In this it is conclude that the nearest control is functionally equivalent to proper common mode voltage and opt for the switching frequency form first to last switch the duty cycles are terminated. The natural balancing of all the capacitors voltages in each module is maintained where the experimental results show the ability of proposed inverter to generate all the levels in both symmetrical and asymmetrical modes. This paper dealt with simulation and comparison of nine level cascaded H-bridge multilevel with different techniques. Here in this paper symmetrical and asymmetrical arrangements of nine levels H-bridge inverters have been compared in order to find optimum arrangement with lower switching losses and optimized output voltage quality.

REFERENCES

[1] Mayur R. Gour, Shankar S. Vanamane, PG Student, Dept of Electrical Engineering, "A Comparative Analysis of Multilevel Inverter: A Theoretical Review", International Conference on Recent Developments on Science, Engineering, Management and Humanities (SEMH- 18).

[2] Sk. Nawaz shareef , G.Tabita , "Design and Analysis of Modular Cascaded H-Bridge Multilevel Inverter for MPPT based PV connected Grid Applications", International Journal of Engineering Research and General Science, Volume 6, Issue 4, July-August, 2018.

[3] J.Gowri Shankar and J.Belwin Edward, "Comparison of Symmetrical and Asymmetrical Cascaded H-Bridge Multilevel Inverter Using Pulse Width Modulation", International Journal of Pure and Applied Mathematics Volume 118.

[4] P. Thirumurugan, D. Vinothin and S.Arockia Edwin Xavier: "New model multilevel inverter using Nearest Level Control Technique", International Journal of Modern Trends in Engineering and Research (IJMTER), Volume 03, Issue 02, 2016.

[5] M. Balamurugan, T.S. Sivakumaran, M.Aishwariya Devi, "Voltage Sag/Swell Compensation Using Z-source Inverter DVR based on FUZZY Controller", 2013 IEEE International Conference on Emerging Trends in Computing, Communication and Nanotechnology (ICECCN)2013.

[6] Aparna Prayag, Sanjay Bodkhe,: "Comparative Study of Symmetrical and Asymmetrical Cascaded H Bridge Multilevel Inverter Topology for Industrial Drive", International Research Journal of the Engineering and Technology (IRJET), Volume: 05 Issue: 02, Feb-2018.

[7] U. B. Tayab, M. A. Roslan and F. N. Bhatti: "Comparative Analysis of Different Switching Techniques for Cascaded H-Bridge Multilevel Inverter Journal of Advanced Research in Computing and Applications" ,Vol. 3, No. 1, 2016.

[8] G. Nageswara Rao Professor, EEE Department, Lakireddy Bali Reddy College of Engineering: "Selective Harmonic Elimination Technique for a Cascaded Multilevel Inverter Using Intelligent

Systems", International Journal of Research in Information Technology, Volume 1, Issue 1, November 2017.

[9] Chitturi Swapna, Rohith Jonnala. "Implementation and Analysis of Symmetrical & Asymmetrical Configurations of Series Connected Sub-Multilevel Inverter with Nearest Level Control Modulation", International Journal of Engineering Research & Technology (IJERT), Volume 4, Issue 07, 2016.