A Performance Evaluation of 1-Phase 3-Level T-Type Multilevel Inverter using Advanced PWM Techniques

Monika Agrawal[1], Prof. Vijay Bhuria[2], Dr.Shishir Dixit[3]
[1,2,3] *Department of Electrical Engineering Madhav Institute of Technology & Science, Gwalior, India*

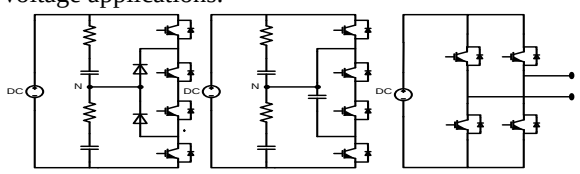
***Abstract*- The elementary concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Multilevel inverter has a capability to increase the output voltage and performance with low switching losses and total harmonic distortion as the level increases the harmonic itself decreases. This paper proposes a 3-phase 3-level T-type inverter with various SPWM strategies having less number of devices which posses high and low power region as compared to conventional inverter. Generally, it is used for low power appliances having maximum efficiency. A 3-phase 3-level T-type inverter was implemented and multicarrier PWM technique is used for multilevel inverter strategies to generate 3-level output phase voltage. Finally simulation results of a 3-level multi-level inverter topology are carried out using MATLAB/SIMULINK R2013a with various SPWM strategies as PD, POD, APOD and its switching on/off pattern of IGBT's.**

Index terms- Multi-level inverter (MLI), T-type inverter and SPWM techniques

I. INTRODUCTION

An inverter is used to convert dc to ac power at a desired ac voltage. But a multilevel inverter can generate a multi-step voltage waveform with less distortion, less switching frequency and higher efficiency. A multilevel inverter belongs to power electronic consists of semiconductor devices that are used for high power applications. While conventional inverter having two voltage level is commonly used for domestic and commercial applications since its configuration is simple and the reliability is better. However , there is a some limitations in high power and performance due to two level inverter output voltage is depend on Vdc. Multilevel inverter provides many advantages over two-level inverter, it increase the output voltage waveform, reduced EMI from the system and (dv/dt) voltage stress on the load, lower switching frequency and low rating devices for high power rating, but the copper loss, torque ripple and higher number of semiconductor switch are increased because of low frequency harmonics. Every switch requires a separate gate driver circuit, therefore increasing the complexity and size of the overall circuit. The SPWM strategy is commonly used to solve the harmonic problem of this six-step method in many applications. The switching loss is more prominent when the switching frequency is increased and the DC link voltage becomes higher. Therefore a three-level inverter is being researched in various applications for further improvement of energy efficiency, reliability, power and density.

The multilevel inverter topology such as the three-level inverter has been developed for both medium and high voltage level. Among various conventional multilevel inverter are categorized as Neutral-Point Clamped multilevel inverter (NPCMLI), Flying Capacitor multilevel inverter (FCMLI) and Cascaded H-bridge multilevel inverter (CHBMLI) have been widely used . In 1981 Nabae introduced a three level diode clamped inverter schemes. These three multilevel inverter the switching loss in each switch is half and the conduction losses become double of the counterpart of the two-level inverter due to the two switch series connection. Therefore, these three-level inverter topologies are not suitable for low-voltage and low-power applications. To overcome these characteristics in the multi-level topology, the three-level T-type inverter (3LTI) has been proposed for the high efficiency and performance in low-voltage applications.



(a) NPCMLI (b) FCMLI (c) CHBMLI

Fig.1. Conventional multi-level inverter topologies

This paper proposes a 3-level T-type multi-level inverter topology which requires less number of switches and gate driver circuits as compared to conventional multilevel inverters. The T-type topology that was previously proposed here is implemented in three-phase with different PWM techniques. The pulse-width modulation (PWM) control is the most efficient method of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the most efficient method, realized by the intersection of a modulating signal with triangular carrier waveform. The paper tries to prove that 3LTI is better than conventional multilevel inverters in terms of their number of components and THD. Even though the 3LTI is generally implemented and investigated to apply in low-voltage applications, it has difficulties to apply in low-voltage and low-power domestic appliances because the increased efficiency is not sufficient due to its complexity and cost problem.

II. THE T-TYPE TOPOLOGY

The basic topology of the 3LTI is depicted in Fig. 2.1. The conventional two-level VSI topology is extended with an active, bidirectional switch to the dc-link midpoint. For low-voltage applications, the high side and the low-side switches (T1 /D1 and T4 /D4) would usually be implemented with IGBTs/diodes as the full dc-link voltage has to be blocked. have any clamping diode and flying capacitor. Cascaded multilevel inverter reaches higher reliability. The cascaded inverter is used for large automotive electric drives. However, the requirement of more number of switches and separate dc source for each cell becomes a problem especially at higher level.

This paper proposes a 3LTI which requires less number of switches and gate driver circuits as compared to conventional multilevel inverters. The Reversing Voltage topology that was previously proposed. Here is implemented in single-phase different PWM techniques. The pulse-width modulation (PWM) control is the most efficient method of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the most efficient method, realized by the intersection of a modulating signal with triangular carrier waveform. The paper tries to prove that optimization method is better than conventional multilevel inverters in terms of their number of components and THD.

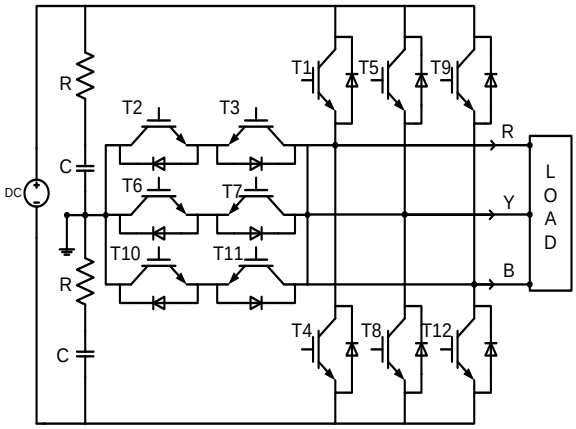


Fig. 2.1 3-phase 3-level T-type Inverter model using NPC topology

Differently, the bidirectional switch to the dc-link midpoint has to block only half of the dc-link voltage. It can be implemented with devices having a lower voltage rating, in the case at hand two IGBTs including anti-parallel diodes are used [cf., Fig. 2(a)]. Due to the reduced blocking voltage, the middle switch shows very low switching losses and acceptable conduction losses, although there are two devices connected in series. Contrary to the three-level NPC topology, there is no series connection of devices that has to block the whole dc-link voltage Vdc. For the NPC topology, switching transitions directly from the positive (P) to the negative (N) dc-link voltage level an device versa are usually omitted as there might occur an uneven share of the voltage to be blocked in the transient case when both IGBTs connected in series turn off at the same time. This undesirable effect cannot occur in the T-type topology. It is not necessary to implement low-level routines which prevent such transitions or ensure a transient voltage balancing among series connected IGBTs.

A single phase 3-level T-type inverter is proposed in this paper implement low-level routines which prevent such transitions or ensure a transient voltage balancing among series connected IGBTs.

A single phase 3-level T-type inverter is proposed in this paper.

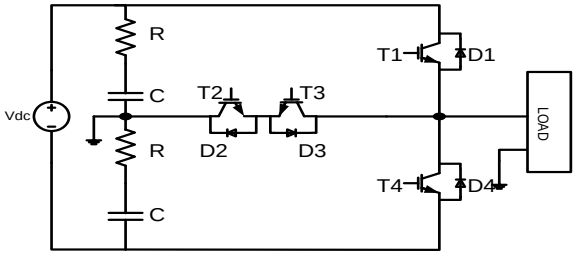


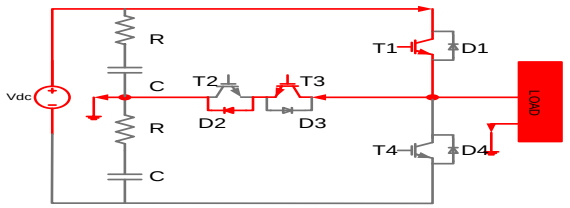
Fig. 2.2 Single Phase 3-level T-type Inverter

TABLE 1

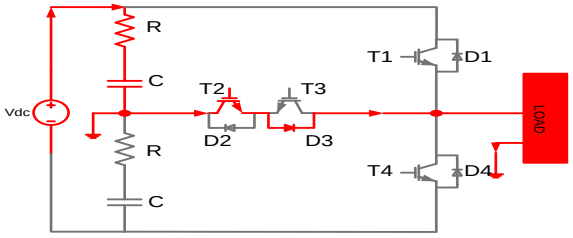
Generation of Level	Switching Devices				Output Voltage
	T1	T2	T3	T4	
+Vdc/2	on	off	on	off	+1v
0	off	on	on	off	0v
-Vdc/2	off	on	off	on	-1v

There are basically two ways the two IGBTs can be configured to form a bidirectional switch, either in common emitter configuration or in common collector configuration. The common emitter configuration [cf., Fig. 2(a)] would require one additional isolated gate drive supply voltage for each bridge leg, summing up to three additional gate drive supplies compared to the two-level VSC topology. This number can be reduced even more if a common collector configuration [cf., Fig. 2(b)] is used. T2 shares now a common emitter with the high-side switch T1 and can be supplied with the isolated gate drive voltage of T1. The emitter of the second IGBT is connected to the midpoint voltage level. If the 3-phase topology is considered, all three IGBTs T3,a,b,c share a common emitter, and therefore only one isolated gate drive supply is necessary. In total, the complete T-type topology can be implemented with only one additional isolated gate drive supply compared to the two-level topology. The necessary power rating of the isolated gate drive supply of the high-side switch T1 is not increased if the gate charges of the IGBT are approximately equal. Because of the implemented commutation and modulation strategy T1 and T2 are newer switched both in the same modulation cycle what will be shown in the next section. It is still necessary to implement six additional gate drive ICs and six additional digital isolators for the switch signals which will increase the costs slightly. Compared to the three level NPC topology the removal of the clamping diodes reduces the necessary diodes from 18 to 12. Furthermore, the reduction of the additional isolated gate drive supplies from six to one is a clear improvement and can drive the costs down.

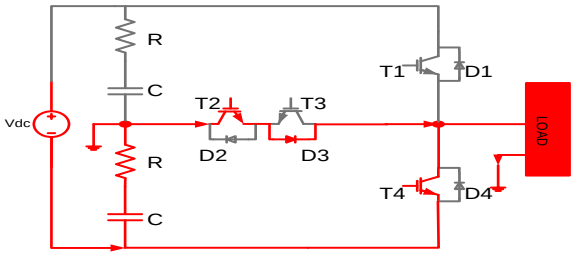
III MODES AND ITS OPERTAION



Mode –I Fig. (a) Level 1(+Vdc/2 volt)



Mode – II Fig. (b) Level 0 (0 volt)



Mode –III Fig. (c) Level -1(-Vdc/2 volt)

Fig. 2.3 Fig. (a), Fig. (b) and Fig. (c) are Switching combination of Single Phase 3-level T-type MLI

Operation of the single-phase 3-level T-type MLI with can be easily explained with the help of fig. 2.1 and table I. When switches T1 and T3 are turned "on" the output voltage will be "+Vdc/2" (i.e., level 1). When switches T2 and T3 are turned "on" the output voltage is zero (i.e., level 0). When Switches T2 and T4 are turned "on" the output voltage will be "-Vdc/2" (i.e., level -1). The voltage blocking capacity of each switch is Vdc [2].

The operation of this topology can also be easily understood by mode of operation of Single-phase 3-level MLI shown in figure 2.3. The voltage source "Vdc" is required 100V. There are three sufficient switching modes in generating the multistep level for a 3-level T-type MLI

IV. MODULATION TECHNIQUES

I. MODULATION STRATEGIES:-

There are different pulse width modulation strategies with different phase relationships. Phase disposition

pulse width modulation (PD PWM):- In phase disposition pulse width modulation strategy, where all carrier waveforms are in same phase shown in fig 3.1 for 3-level MLI.

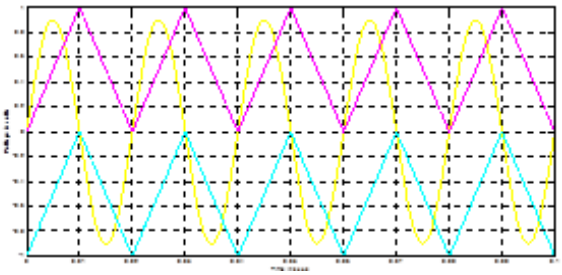


Fig. 3.1: Carrier arrangement for PDPWM strategy

Phase opposition disposition pulse width modulation (POD PWM):- In phase opposition disposition pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below zero reference are 1800 out of phase. Shown in fig 3.2.

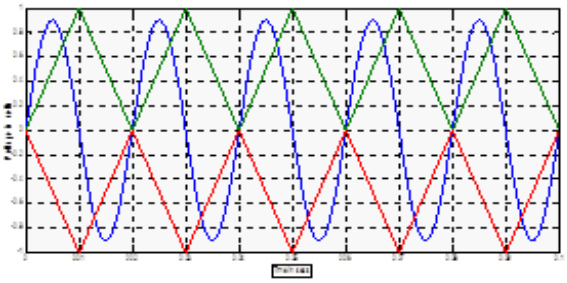


Fig. 3.2: Carrier arrangement for PODPWM strategy

Alternate phase opposition disposition pulse width modulation (APOD PWM):- In alternate phase opposition disposition PWM scheme where every carrier waveform is in out of phase with its neighbor carrier by 1800. Shown in fig 3.3.

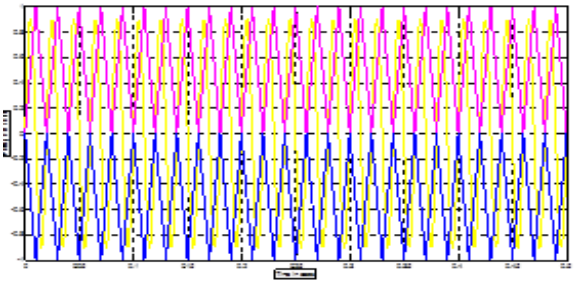


Fig. 3.3: Carrier arrangement for APODPWM strategy

V. SIMULATION RESULTS

The Fig. 2.1 & 2.2 shows the OT model of single-phase & three-phase 3-level T-type MLI. The simulation parameters are as following: dc source voltage is 100V; Frequency of carrier signal is 1 kHz. In this paper, three PWM techniques are used PD, POD, and APOD, with same modulation index (Ma). For Ma = 1.0, and Mf = 20, corresponding (%) THD are PD = 77.92%, POD = 71.01%, APOD =71.01%. Based on the PWM techniques, the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

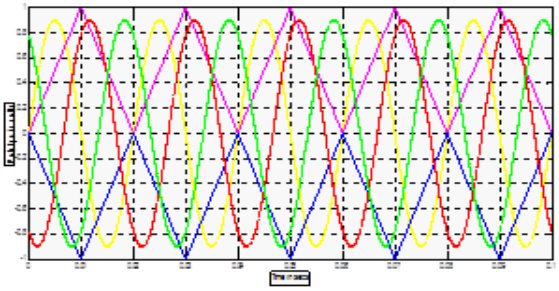


Fig. 3.4: Carrier Modulation Signals of Three-Phase 3-Level T-type

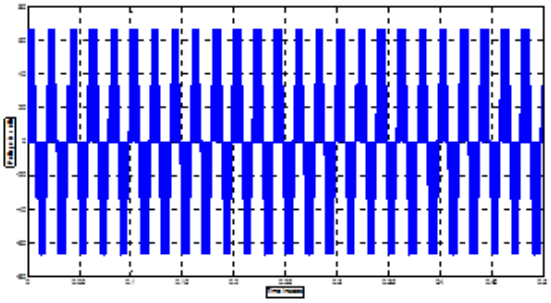


Fig. (a): Line Voltage

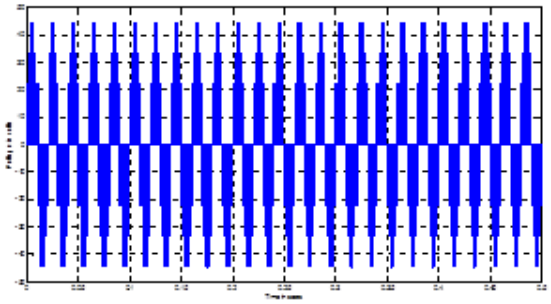


Fig. (b): Phase Voltage

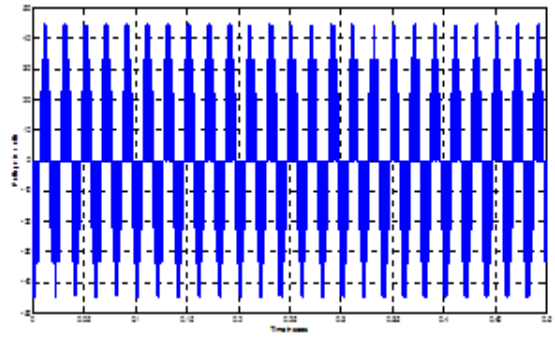


Fig. (c): Phase Voltage

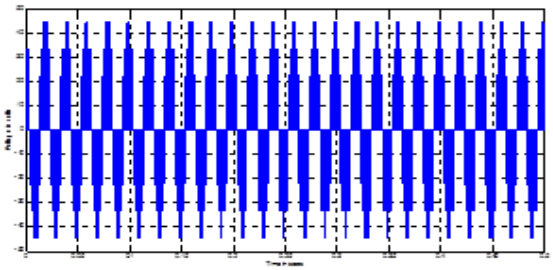


Fig. (d): Phase Voltage

Fig. 4 Fig (a), Fig (b), Fig (c) and Fig(d): Simulated Three-Phase Voltage by PDPWM for R Load

INVERTER TYPE	NPC MLI	FC MLI	CHB MLI	T-TYPE MLI
Main Switches	04	04	04	04
Main Diodes	04	04	04	04
Clamping Diodes	02	0	0	0
DC Bus Capacitor/ Isolated Supplies	02	02	03	02
Flying Capacitor	0	03	0	0
Total Numbers	12	13	11	10

TABLE 2

Table-2, shows that the number of components of the proposed topology is lower than that of other topologies so as the voltage level increases the number of components will decreases particularly for higher voltage levels [7].

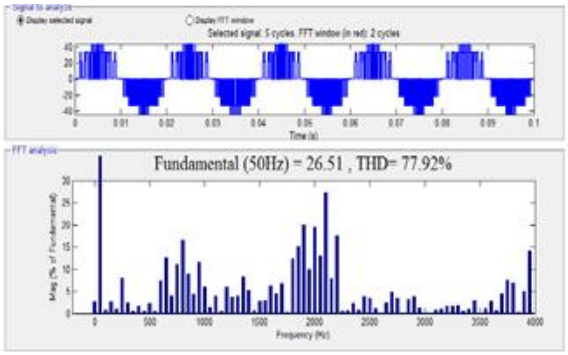


Fig. 5.1: Phase output voltage by PD (Ma=1.0, Mf=20).

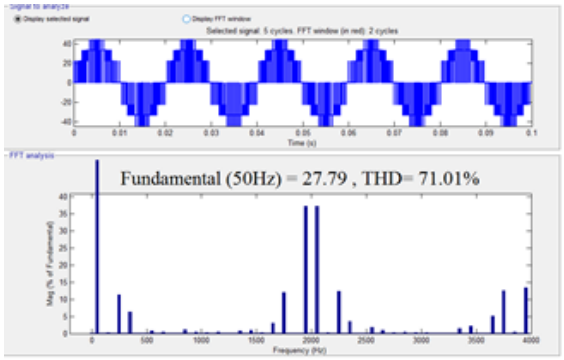


Fig.5.2: Phase output voltage by PODPWM (Ma=1.0, Mf=20).

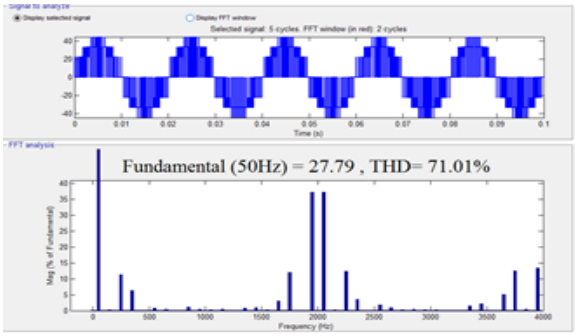


Fig. 5.3: Phase output voltage by APODPWM (Ma=1.0, Mf=20).

TABLE 3

Modulation Index	PDPWM	PODPWM	APODPWM
1	77.92%	71.01%	71.01%
0.9	101.96%	82.62%	82.62%
0.8	134.56%	93.73%	93.73%
0.7	182.43%	107.10%	107.10%
0.6	264.57%	123.56%	123.56%

VI. CONCLUSION

In this paper, a 3-level T-type multi-level inverter using is proposed with different PWM techniques and proposed MLI topology with different PWM techniques is used to generate 3-level output phase voltage. It is proved that, the proposed work of Single phase and three phase 3-level T-type inverter output voltage total harmonics distortion is reduced and improve the efficiency of system compare with different conventional topologies of single phase and three-phase 3-level MLI. Harmonic analysis carried out using Mat Lab R2009a version software. This proposed MLI topology requires less number of components as compared to conventional MLI inverters. Simulation results show the performance of single-phase and three-phase 3-level MLI with different PWM techniques.

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