Design of Low Power 2-D Discrete Wavelet Transform using Hybrid Encoded Booth Multiplier

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Abstract- **The design of low power high performance 2-D Discrete Wavelet Transform (DWT) unit is presented in this paper. A low power multiplier with hybrid encoding scheme is proposed to reduce the power consumption compared with other common multipliers. Multiplication is the main arithmetic operation used in the lifting scheme of the DWT and the proposed method reduces the total power requirements. The lifting step and multiplier are designed and synthesized using XILINX SPARTRN 3E Field Programmable Gate Array (FPGA). The power consumption of the DWT with hybrid encoded Booth multiplier is compared with existing array and Booth multiplier. The simulation results show the total power dissipation of the DWT with hybrid multiplier saves 90% and 76% power compared with array and Booth multiplier.**

Index terms- **Discrete Wavelet Transform, Low power, VLSI Design, Booth Multiplier, Hybrid encoding.**

I.INTRODUCTION

The growing popularity of portable and multimedia devices such as video phones and note books has motivated the research to design low power VLSI circuits in the recent past. The real time implementation of image processing system is expected to consume high computational power and high data throughput rate which limits the use of general purpose processors. Recently, Wavelet-based video coding technique has gained much attention. Based on this technique, Discrete Wavelet Transform (DWT) has been widely applied in many different fields of audio and video signal processing. DWT supports features like progressive image transmission, ease of compressed image manipulation, region of interest. In general, DWT can be implemented by direct convolution and some DWT architectures implemented by filter convolution have been proposed. The high algorithmic performance of the 2D DWT in image compression justifies its use as the kernel of both the JPEG2000 still image compression standard and the MPEG-4 texture coding standard. The JPEG2000 can compress images 100 times smaller than the original image.

With this compression ratio, the reconstructed image of the JPEG2000 still provides good visual quality. However, such an implementation suffers from the disadvantage of a large number of computations and a large storage resource. A new scheme, termed the lifting scheme which reduces the number of computation, has been proposed for the DWT. Lifting scheme has several advantages, including in-place computation of the wavelet coefficients, integer-to-integer wavelet transform, and etc. Up to now, some 2-D DWT VLSI implementations have been proposed based on the lifting scheme. Due to the computational complexity of the DWT there has been a lot of focus on developing fast algorithms with high efficiency and low hardware cost. DSP algorithms have traditionally been used by dedicated DSP chips or Application Specific Integrated Circuits (ASIC). In the last few years the viability of Field Programmable Gate Arrays (FPGAs) has provided an alternative to their sequential counterparts in executing DSP algorithms. It is well known that if the number of switching activities increases dynamic power consumption also increases. This has further motivated the design of low power VLSI circuits, with new concepts. It is also clear that the reduction in power consumption and enhancement in the circuit design are expected to pose challenges in implementing digital image processing system, in which multiplication is the key computations. In the recent past, the researchers proposed various design methodologies on dynamic power reduction by minimizing the switching activities.

II DIMENTIONAL DISCRETE WAVELET TRANSFORM

A 2-D DWT can be seen as a 1-D wavelet transform along the rows and then a 1-D wavelet transform along the columns. The 2-D DWT operates in a straightforward manner by inserting array transposition between the two 1-D DWT. The rows of the array are processed first with only one level of decomposition. This essentially divides the array into two vertical halves, with the first half storing the average coefficients, while the second vertical half stores the detail coefficients. This process is repeated again with the columns, resulting in four sub-bands within the array defined by filter output.

The LL sub-band represents an approximation of the original image, the LL1 sub-band can be considered as a 2:1 sub-sampled (both horizontally and vertically) version of the original image. The other three sub-bands HL1, LH1, and HH1 contain higher frequency detail information (mostly local discontinuities in the edges of the image). This process is repeated for as many levels of decomposition as are desired. The 2-D DWT is a multilevel decomposition technique.

A line-based architecture scan input image row by row manner to produce the wavelet coefficients. However, a block-based architecture scans the input image block-by-block and produces the wavelet coefficients for each block. Consequently, the main difference between the two methods is the selected image traversal method (based on complete image rows or on blocks). The line based architecture needs only few lines of the image to be stored, whereas traditional methods almost need the whole image (or tile) to be memorized. Thus, this technique does not require extra memory or external memory to store the intermediate data. Instead, some internal buffers are used to store the intermediate data, and the required memory size is proportional to image width or height. Our goal mainly focuses on the high-performance, low power consumption and hardware size.

III HYBRID ENCODED LOW POWER MULTIPLIER

The process of the hybrid encoded multiplier is divided into encoder selection, partial product generation and partial product compression. The multiplier and the multiplicand are stored in register M1 and M2, the number of 1's in the multiplier is checked by the bit checker. Based on the number of 1's the encoder selector selects either proposed hybrid encoder or modified encoder. A clock gating circuit is used to avoid the simultaneous operation of the two encoders. In the partial product compression the partial products are compressed using 4:2 compressor and row bypassing can be used when the entire row of the PP is zero.
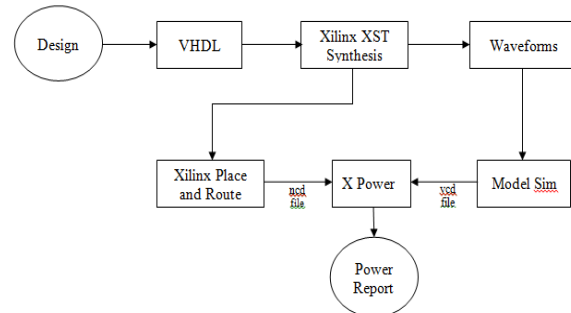

Figure.1 Xpower design flow

This is done by freezing the adder while the above condition occurs. This is expected to reduce the switching activity and hence power consumption. A column bypassing provision is provided at the final adder tree to avoid the unwanted addition operation. The detection logic circuit is used to detect the effective data range. If the part of the input data does not make any impact in the final computing results then the data controlling circuit freezes that portion to avoid unnecessary switching transitions. A glue circuit controls the carry and sign extension unit which manage the sign bit.

IV X-POWER OVERVIEW

XPower is the power-analysis software available for programmable logic design. It enables to interactively and automatically analyze power consumption for Xilinx FPGA and CPLD devices. XPower includes both interactive (xpower) and batch (xpwr) applications. Earlier in the design flow than ever, the total device power, power per-net, routed, partially routed or unrouted designs can be analyzed, all driven from a comprehensive graphic interface or command-line driven batch-mode. XPower also reads VCD simulation data from the ModelSim family of HDL simulators to set estimation stimulus, reducing setup time, as well as from the additional simulators

listed in simulator support. Xpower tool flow is shown in Fig. 1.

Xpower files: XPower recognizes the following file types.

Design files: Design file is an NCD (FPGA device) or CXT (CPLD device) file that contains information about the design.

Physical constraints file: A Physical Constraints File (PCF) is a text file containing two separate sections: a section for those physical constraints created by the mapper and a section for physical constraints entered by the user. Temperature, voltage, max delay and time graphs are read from the PCF.

Settings file: Specifies a settings file (*_xpwr.xml) to be used by XPower. A settings file is an XML-based file that represents the current state of the power data, constrained by the reporting options that already have specified. This file is generated by XPower when settings are saved and is used to restore the settings.

Simulation file: Specifies a simulation file (*.vcd) to be used by XPower. This file is the output of a simulation run on the design. IEEE standard VCD files are accepted for input of simulation data.

V RESULTS AND DISCUSSIONS

The hardware codes for the proposed architectures were written in verilog-hardware description language and evaluated under ModelSim simulation tool. The architectures were synthesized by Xilinx FPGA express tools and evaluated on the Xilinx Spartan 3e FPGA The typical evaluation for the performance of the architectures of 2-D DWT includes the delay, power consumption and device utilization. The architectures of array multiplier, Booth multiplier, and proposed hybrid multiplier are simulated, implemented. Fig 9 and Fig 10 shows the device utilization and power consumption of the proposed hybrid encoded Booth multiplier.

The performance report of array multiplier, Booth multiplier and proposed hybrid multiplier are shown in Table 1.

Table 1. Performance analysis of various multipliers

Multipliers	Power in mW	Device utilization	
		Number of Slices in %	Number of 4 input LUTs in %
Array	88	36	33
Booth	75	18	18
Hybrid encoded	69	9	8

The power consumption, delay and device utilization of array multiplier, Booth multiplier and proposed hybrid encoded multiplier are compared. From the results it is clear that the proposed hybrid multiplier's performance is better compared with other multipliers.

The architecture of 128×128 DWT has been synthesized by Xilinx FPGA Express tools, written in Verilog and synthesized on the Xilinx Spartan 3e FPGA. The power consumption, delay and device utilization of DWT with array multiplier, Booth multiplier and proposed hybrid encoded multiplier are compared in Table 2. From the results it is clear that DWT with the proposed hybrid multiplier's performance is better compared with other multipliers.

Table 2. Performance analysis of DWT with various multipliers

Multipliers	Power in mW	Device utilization	
		Number of Slices in %	Number of 4 input LUTs in %
Array	2904	66	59
Booth	652	22	19
Hybrid encoded	292	7	6

VI CONCLUSION

The design of low power high performance 2-D Discrete Wavelet Transform (DWT) unit is presented in this paper. A low power multiplier with hybrid encoding scheme is proposed to improve the power dissipation compared with other common multipliers. This paper implements a lifting step function used in second generation DWT. Multiplication is the main arithmetic operation used in the lifting scheme and the proposed method reduces the total power requirements. The lifting step and multiplier was designed and synthesized using XILINX SPARTRN 3e Field Programmable Gate array (FPGA). The power consumption of the DWT with hybrid multiplier is compared with existing array and Booth multiplier. The simulation results show the total power dissipation of the DWT with hybrid multiplier saves 90% and 76% power compared with array and Booth multiplier.

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