Design and Implementation of Traffic Light Controller Using FPGA

Parag Burhade[1], Shubham Sonar[2], Onkar Kulkarni[3]
[1,2,3] *Student, MVP's Karmaveer Adv. Baburao Ganpatrao Thakare College of Engineering*

***Abstract*- The traffic in road crossings /junctions is controlled by switching ON/OFF Red, Green & Yellow lights in a particular sequence. The Traffic Light Controller is designed to generate a sequence of digital data called switching sequences that can be used to control the traffic lights of a typical four roads junction in a fixed sequence. It plays more and more important role in modern management and control of urban traffic to reduce the accident and traffic jam in road. The device that involves an analysis of existing sequential machines in traffic lights controllers, timing and synchronization and introduction of operation and flashing light synthesis sequence. The methods that are used in this project are design the circuit, write a coding, simulation, synthesis and implement in hardware. In this project, XILINX Software was chosen to write a code using VHDL (Hardware Description Language) text editor and implements the circuit.**

I.INTRODUCTION

The monitoring and control of traffic is a becoming a major problem in many cities of countries. With the ever increasing number of vehicles on the road, the Traffic monitoring authority has to find new method of overcoming such a problem. Present Traffic Light Controller (TLC) is based on microcontroller and microprocessor. These TLC have limitation because it uses the pre-defined hardware, which is functioning according to the program that does not have the flexibility of modification on real time basis.

The system proposed in this paper is used for traffic light controller using Field Programmable Gate Array (FPGA). FPGA are extensively using in rapid prototyping and verification of conceptual design. Many system designs that used to be built in VLSI are now implemented in FPGA. The main objective of this project is to design a traffic light controller to manage the traffic movement of a junction of four road, and to achieve the best utilization of system for the four way roads. Coding of the design is done using VHDL and the design is tested and simulated on spartan-6 FPGA development kit.

II. LITERATURE REVIEW

Various types of research works have been done and still going on related to traffic light controll. Some are listed below:

N. M. Z. Hashim, A. S. Jaafar, N. A. Ali, L. Salahuddin, N. R. Mohamad, M. A. Ibrahim deals about Traffic Light Control System for Reserve Vehicles Using Radio Frequency. According to all these papers, a suitable wireless communication between reserve vehicles and the traffic light is by using RF. The model of this project is by the radio frequency of 434 MHz compared to the range of about 3 kHz to 300 GHz of frequency which have been reserved for the RF theoretically [1].

Nath, S., Pal, C., Sau, S., Mukherjee, S., Roy, A., Guchhait, A., Kandar, D. (2012), Design of an FPGA based intelligence trafic light controller with VHDL. In this paper discussed about TLC implementation based on FPGA using VHDL language.It gives ideas of different type of modelling style can be use for implementation of TLC. It shows comparison between moore and melay machines [2].

Farheena Shaikh, Dr. Prof. M. B. Chandak describes an approach towards Traffic Management System using density calculation and reserve vehicle aware. In this paper, Wireless Sensor Networks organized along a road can be used to control the traffic load on roads and at traffic crossings. Sensors are deployed on either side of roads at crossing points and in reserve vehicles respectively. These sensors run on both solar energy as well as battery. Present traffic light systems have timers that are set at systematic intervals. This leads to the waste of precious time especially in case of rescue vehicles for reserve conditions. In order to control this situation, they

have planned a system consisting of two parts: Smart Traffic Light Control System (STLC) and Smart Congestion Avoidance System (SCA) during emergencies. STLC System controls the change of traffic lights at crossing points giving high priority to reserve vehicles. SCA System is a smart traffic routing system that chooses the shortest routes having the smallest congestions. The system based on GPS so it has some problems in application. Thus this system is somewhat changeable [3].

Khalaji, A., Seyedtabaii, S. (2013).discussed about implementation of a traffic light controller by CMOS technology. It used a fuzzy logic for implementation and that is a reconfigurable [4].

III. SYSTEM AND OVERVIEW

A. FPGA

The Field Programmable Gate Array (FPGA) is a family of reconfigurable hardware, where Field Programmable means the operation changing capability in the field, and Gate Array means the construction of basic internal architecture of the device. FPGA can be programmed with VHDL (Hardware Description Language).Here FPGA is used for data processing.

Fig.1 A shows simplified version of design flow

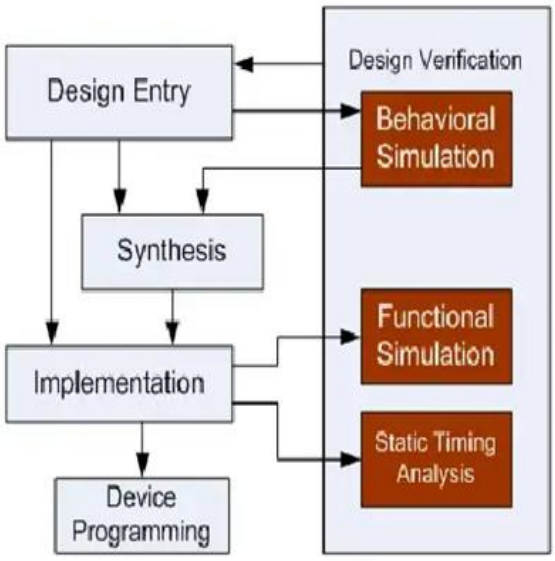


Fig 1: Design Flow of FPGA

There are various techniques for design entry. Schematic based, Hardware Description Language and combination of both etc. Selection of a method depends on the design and designer. If the designer wants to deal more with Hardware, then Schematic entry is the good choice. When the design is complex or the designer thinks the design in an algorithmic way then HDL is the better choice. Language based entry is faster but lag in performance and density.

HDLs represent a level of abstraction that can separate the designers from the details of the hardware implementation. Schematic based entry gives designers much more visibility into the hardware. It is the good choice for those who are hardware adapted to. Another method but rarely used is state-machines. It is the better choice for the designers who think the design as a series of states. But the tools for state machine entry are limited. In this documentation we are going to deal with the HDL based design entry.

B. Design Entry

There are different techniques for design entry. Schematic based, Hardware Description Language and combination of both etc. . Selection of a method depends on the design and designer. If the designer wants to deal more with Hardware, then Schematic entry is the better choice. When the design is complex or the designer thinks the design in an algorithmic way then HDL is the better choice.

C. Synthesis

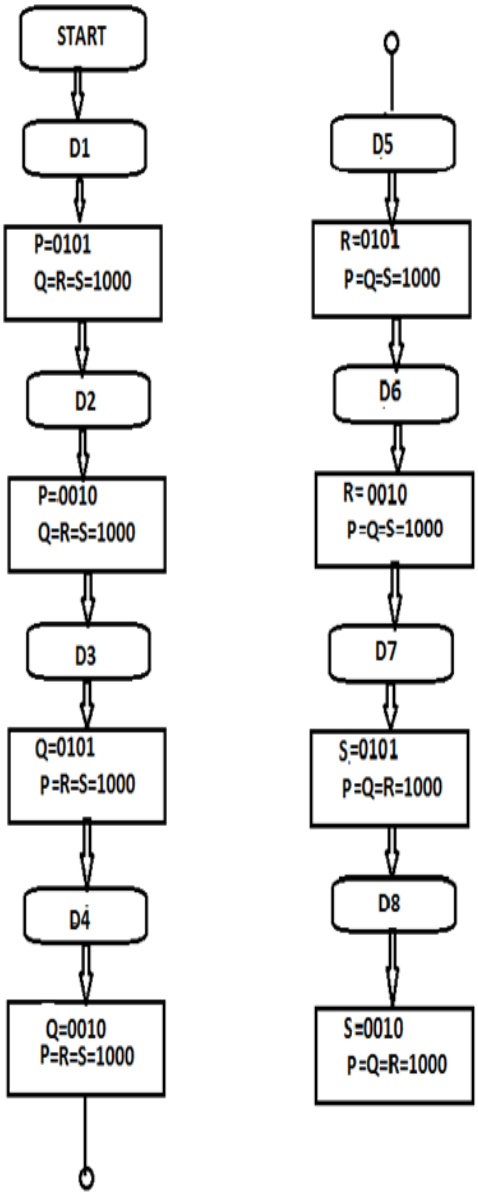
The process which translates VHDL or Verilog code into a device net list format .i.e. a complete circuit with logical elements (gates, flip flops, etc…) for the design. If the design contains more than one sub designs, ex. to implement a processor, we need a CPU as one design element and RAM as another and so on, then the synthesis process generates net list for each design element.

Synthesis process will check code syntax and analyse the hierarchy of the design which ensures that the design is optimized for the design.

D. Hardware Implementation

The Traffic Light Controller was designed using VHDL and was implemented using FPGA. The output of the Traffic light controller is verified with NEXYS 3 FPGA.

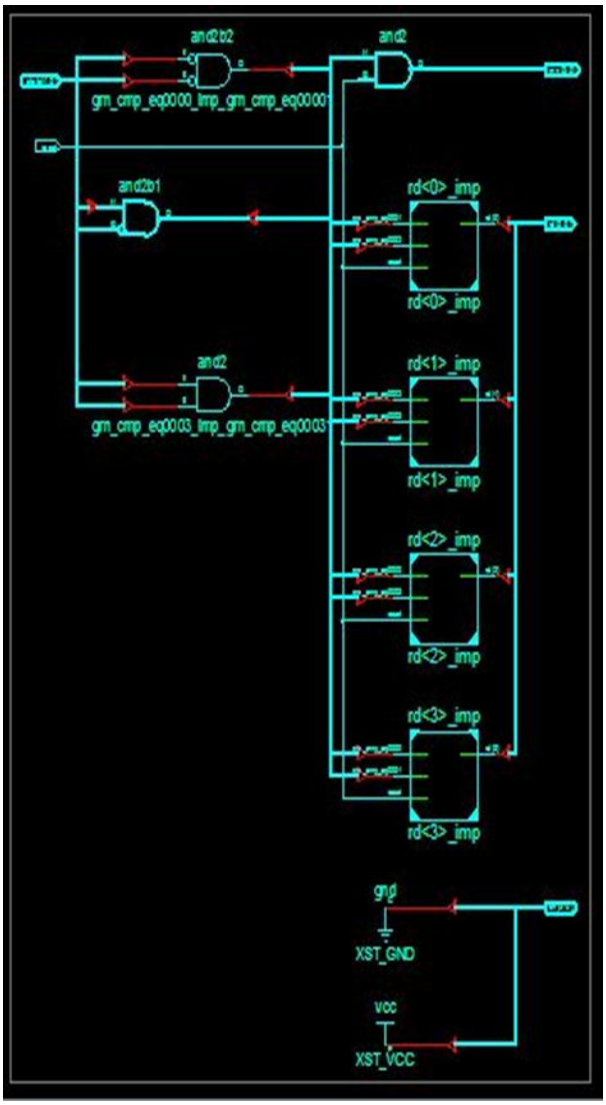
IV. FLOW CHART



IV.SIMULATION RESULT

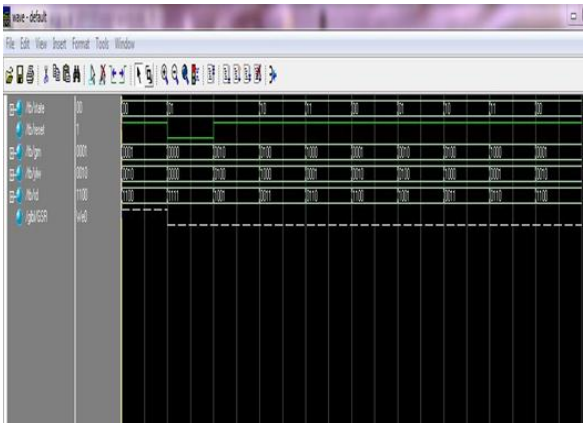
RTL Schematic:

The figure below shows the RTL Schematic diagram of the Traffic Light Controller. Viewing a schematic allows you to see a technology level representation of your VHDL optimized for specific device architecture, which may help to you discover the design issues early in design process.



Wave Forms:

The below figure shows the Wave form of the Traffic Light Controller when the test bench is applied to the source code.



V. CONCLUSION AND FUTURE SCOPE

The modern ways of multi-way traffic management improves the traffic condition up to a large extent. Advanced signaling controllers contribute to the improvement of the urban traffic; which is proportional to the complexity of the controller. These more complex controllers can be well handled using states machines. Methods to reduce the states in the state machine also help in reducing the required hardware thus leading to low power and area efficient design. The future scope of this project is it can be directly applied in real time by employing more number of such circuits.

REFERENCE

[1] Nath, S., Pal, C., Sau, S., Mukherjee, S., Roy, A., Guchhait, A., Kandar, D. (2012). Design of an FPGA based intelligence trac light controller with VHDL.

[2] Khalaji, A., Seyedtabaii, S. (2013). Intricacies in digital CMOS implementation of a recongurable fuzzy logic trac light controller. The fifth Conference on Information and Knowledge Technology.

[3] Traffic light controller Anita Didal, Pragati Sachan, Anchal Katiyar Pallavi Gautam M.Tech Scholar, VLSI, Jayoti Vidyapeeth Womens University Jaipur, Rajasthan, INDIA.

[4] Traffic light controller Anita Didal, Pragati Sachan, Anchal Katiyar Pallavi Gautam M.Tech Scholar, VLSI, Jayoti Vidyapeeth Womens University Jaipur, Rajasthan, INDIA.

[5] FPGA Implementation of an Advanced Trac Light Controller using Verilog HDL B. Dilip, Y. Alekhya, P. Divya Bharathi.

[6] Parasmani, Shri Gopal Modani, FPGA-Based Advanced Trac Light Controller Simulation, International Journal of Scientic & Engineering Research, Volume 4, Issue 9, September-2013.

[7] FPGA Implementation of an Advanced Trac Light Controller using Verilog HDL , Dilip, Y. Alekhya, P. Divya Bharathi ,Advanced Research in Computer Engineering & Technology; Volume 1, Issue 7,pp: 2278 1323,2012.

[8] FPGA-Based Advanced Real Trac Light Controller System Design. El-Medany, W.M.; Univ. of Bahrain, Sakhir ; Hussain.