Design of Inverted Gate Vedic Multiplier in 45, 65, 90 NM CMOS Technologies

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Abstract **- In recent years, due to the rapid growth of high-performance digital systems, speed and power consumption become very vital in multiplier design. In this paper, a Vedic multiplier has been designed using the combination of Urdhva Triyakbyam Sutra and Carry Save Adder. This algorithm satisfied the requirement of a fast multiplication operation because of the vertical and crosswise architecture from the Urdhva Triyakbyam Sutra which minimize the number of partial products compared to the conventional multiplication algorithm. The multiplier is simulated using Microwind Tools with General Process Design Kit (GPDK) of 45, 65, 90 nm CMOS technologies using several voltage supplies to find the most optimum value for the voltage supply to be used. The result shows that with the usage of 1 V voltage supply, the new design of multiplier using a combination of CSA and Vedic mathematics can produce the lowest power consumption and least delay time. Vedic multiplier can yield a full output voltage swing with a power consumption is 0.215 mW in 45nm, 0.235 mW in 65nm and 1.410 mW in 90 nm. delay of 0.27 ns in 45nm, 0.54 ns and 0.72 ns. compact area of 898.6 µm2 in 45nm, 2752.1 in 65nm, 4549.4 µm2 in 90 nm.**

Index Terms **- CMOS 90nm, Inverted Gate, Vedic Multiplier, Urdhva Tiryagbhayam, Carry Save Adder, Layout Design.**

1.INTRODUCTION

With the advent of VLSI technology and the exponential growth in the number of transistors on the chip, there is a need for newer architectures to be faster, and at the same time, power consumption to be at its minimum. The Carry Save adder and 2-Bit Vedic multiplier are proved to be much more efficient when compared to their conventional standard designs. The proposed design of the 4-Bit multiplier using these modified designs helps improve the overall performance of the system. Discrete Cosine Transformation (DCT) plays a crucial role for compression of images, the works of propose a custom multiplication algorithm for reducing the complexity of matrix multiplication.

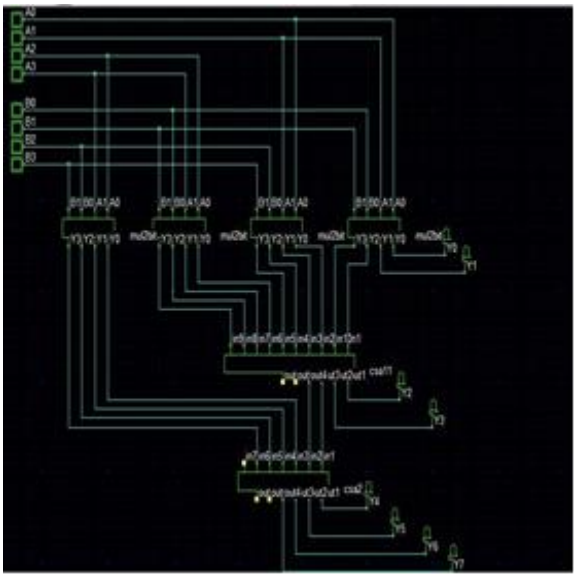


Fig: Schematic of 4 – Bit Vedic Multiplier

Vedic multiplications techniques are proven to be more effective than conventional methods.
which is the main driving factor for our study into Vedic mathematics. Various multipliers and dividers based on Vedic sutras and the authors conclude that the use of these sutras in the computing algorithm of the digital system would reduce the complexity of design, area, execution time and power consumption. Karatsuba algorithm
is preferred for higher bit multiplication and numerous implementations.

2. MULTIPLICATION TECHNIQUE

Urdhva Tiryakbhyam (Vertically and Crosswise), deals with the multiplication of numbers. This Sutra has been traditionally used for the multiplication of two numbers in the decimal number system. In this paper, we apply the same idea to the binary number system to make it compatible with the digital

hardware. Let us first illustrate this Sutra with the help of an example in which two decimal numbers are multiplied.

Example:

234
*316

61724
1222---carry

73944

Steps:

4 X 6 = 24: 2, the carried over digit is placed below the second digit.

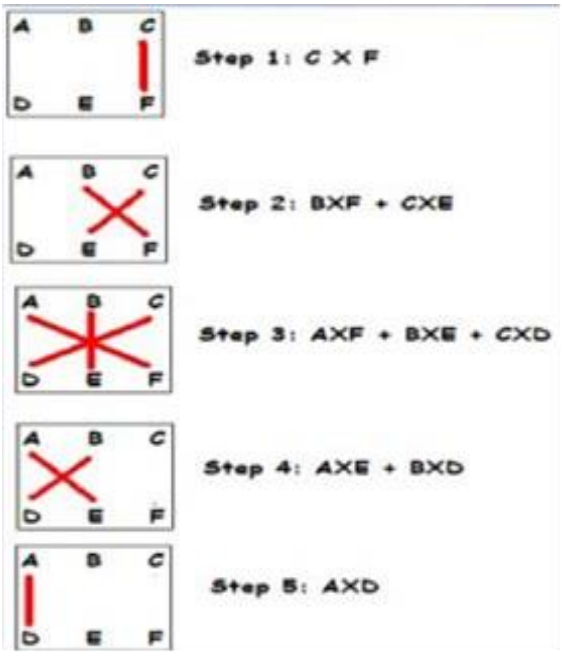
(3 X 6) + (4 x 1) = 18 + 4 = 22; 2, the carried over digit is placed below third digit.

(2 X 6) + (3 X 1) + (4 X 3) = 12 + 3 + 12 = 27; 2, the carried over digit is placed below fourth digit.

(2 x 1) + (3 x 3) = 2 + 9 = 11;1, the carried over digit is placed below fifth digit 5) (2 x 3) = 6

6) Respective digits are added.

Line diagram for the multiplication of two numbers (234× 316) is shown in Fig. 1. The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the results.



3. MODIFIED VEDIC MULTIPLIER

Usage of Vedic multiplier in convolution Vedic multipliers can also be used in the most fundamental operation known as convolution.

3.1 Convolution:

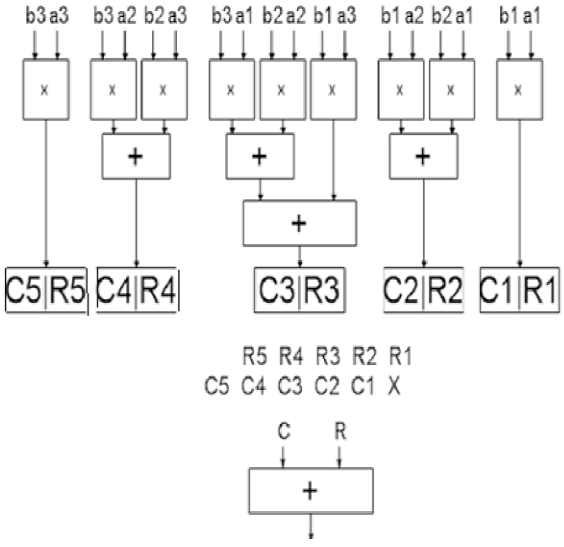
It is a mathematical way of combining two signals to form a third signal. For two finite discrete sequences of length Nx and Nh, the linear or a periodic convolution sum takes on a slightly different form.

3.2 Implementation of sutra in convolution:

1. The power and area for this design can be evaluated after designing original convolution algorithm using conventional multiplier and adder units.
2. The original design can be redesigned to reduce the number of multipliers needed using cyclic data flow and the power, and area for this design can be evaluated
3. The original design can be redesigned to reduce the number of adders needed using cyclic dataflow and power and area for this design can be evaluated.
4. By redesigning the original design with pipeline structure by incorporating latches in critical path, power and area for this design can be evaluated.

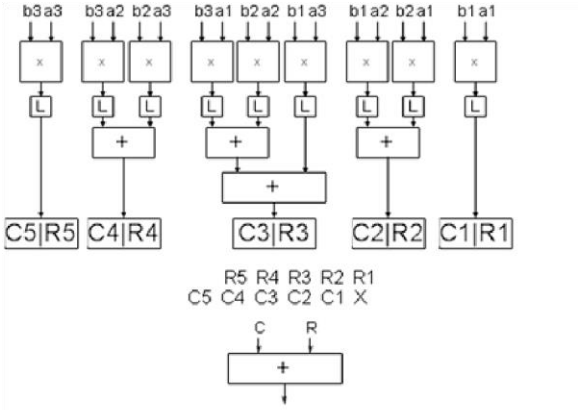
3.3. Usage of Vedic multiplier in convolution operation

Type I



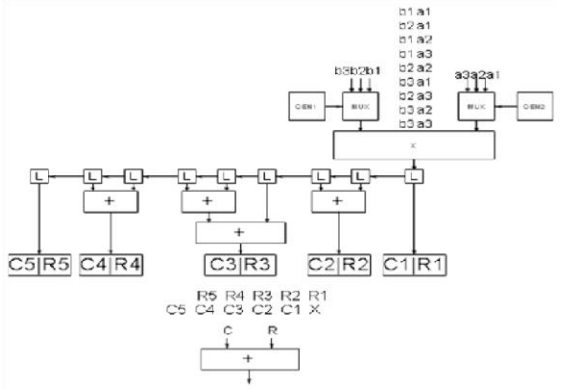
In this architecture 9 multipliers each of 4 bits, 4 adders of 8bits and 9 bits are used respectively

Type II



In this architecture pipeline approach has been implemented and latches have been used. Latches are used to stabilize the initial state.

Type III



In this architecture 1 multiplier is used as compared to 9 multipliers in type I and II respectively.

3.4 Carry Save Adder1

Carry save adder is mainly used in the addition of three or more n-bit numbers. CSA is similar to the full adder. Instead of using any other adder here we use CSA for the addition of the partial product terms of each group. Compared with other adders CSA is fast and it is more easy to understand. We need to add more than two numbers together in many cases, the easiest way of adding together m numbers is by adding the first two, wherein both the numbers are n bits wide. Then their sum is added to the next one and so on.

Consider the sum:

1 2 3 4 5 6 7 8
+ 8 7 6 5 4 3 2 0

=1 0 0 0 0 0 0 0 0

Using basic arithmetic, we calculate right to left, "8+2=0, carry 1", "7+2+1=0, carry 1", "6+3+1=0, carry 1", and so on to the end of the sum. Although we know the last digit of the result at once, we cannot know the first digit until we have gone through every digit in the calculation, passing the carry from each digit to the one on its left. Thus, adding two n-digit numbers has to take a time proportional to n, even if the machinery we are using would otherwise be capable of performing many calculations simultaneously.

3.5 Carry Save Adder 2

Carry save adder is mainly used in the addition of three or more n-bit numbers. CSA is similar to the full adder. Instead of using any other adder here we use CSA for the addition of the partial product terms of each group. Compared with other adders CSA is fast and it is easier to understand. We need to add more than two numbers together in many cases, the easiest way of adding together m numbers is by adding the first two, wherein both the numbers are n bits wide. Then their sum is added to the next one and so on.

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In figure the use of the standard half adder is eliminated, and the circuit is modified which helps reduces the delay and power consumption. The design is tested and verified using Microwind spice tool in TSMC 45, 65, 90 nm CMOS technology.

4. SCHEMATIC AND LAYOUTS DESIGNS IN 45, 65, 90NM CMOS TECHNOLOGY

4.1 Schematic Designing of 2 – Bit Multiplier.

In figure 4.1 the use of the standard half adder is eliminated, and the circuits is modified which helps reduces the delay and power consumption. The design is tested and verified using Micro-Wind spice tool in TSMC 45, 65, 90 nm Technology

2- Bit Multiplier:

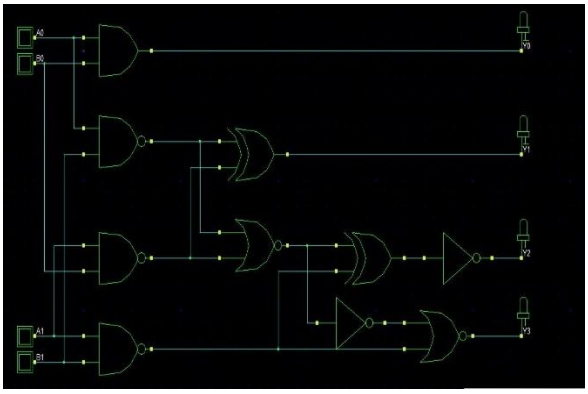


Fig 4.1: Schematic Designing of 2 – Bit Multiplier.

The 4 × 4 multiplication is done considering the grouping 2 bits together each of the 4 – Bit input.

4.2 Schematic Designing of Carry Save Adder 1

Carry Save Adder is used to add three numbers at an instant. Using this property of CSA, eliminates the need for a third adder in the 4 – Bit multiplier design. The use of two adders instead of three decreases the delay, power dissipation and area consumed. CSA has the advantage of using parallelism to significantly boost computational efficiency as there are multiple operands. CSA 1 is modified to suit the needs of the 4 – Bit multiplier. CSA 1 is used to add three numbers, two of which are four bits and the third in two bits wide.

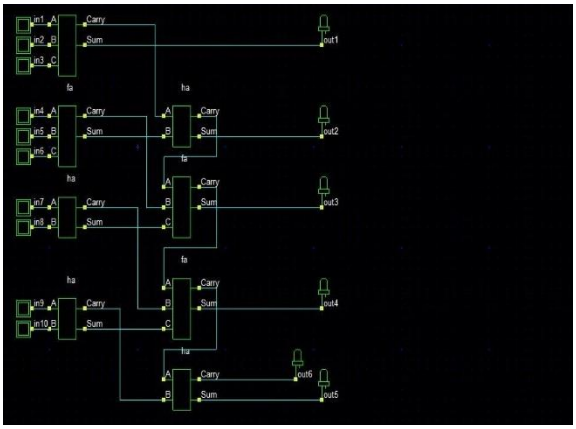


Fig 4.2 : Schematic Design of Carry Save Adder 1

4.3 Schematic Designing of Carry Save adder 2

The figure 4.3.1 shows the Schematic of CSA 2. CSA 2 is modified to add two numbers, one of four bits that is the output of the fourth 2 – Bit multiplier and the other three bits that is the output of CSA 1

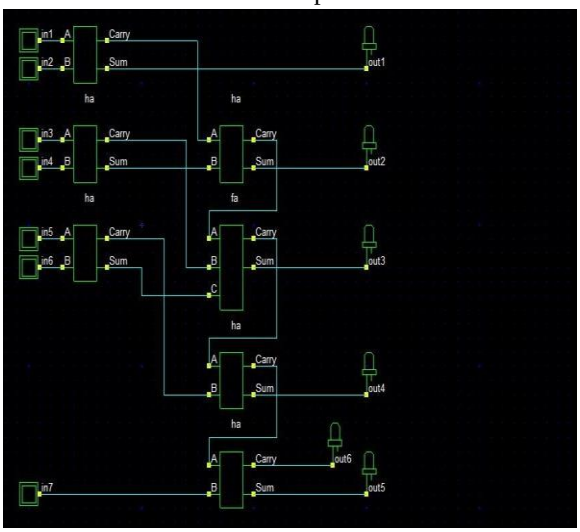


Fig 4.3: Schematic Design of Carry Save Adder 2

4.4 Schematic Designing of 4 – Bit Vedic Multiplier

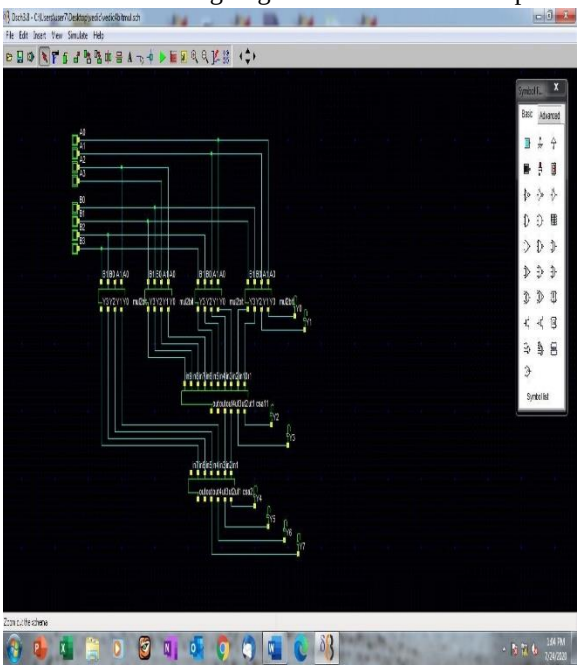


Fig 4.4: Schematic Design of Vedic Multiplier

In above we can see the designing of the 4 -bit Vedic multiplier. Which is consist of four stage 2 – bit multiplier and two stage Carry save adder.

4.5 Layout Design of the Inverted Gate Vedic Multiplier:

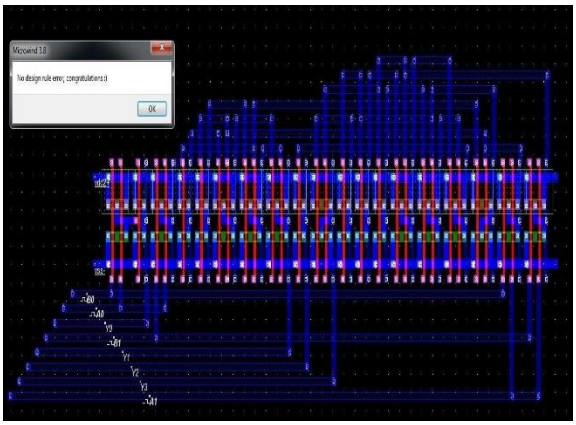


Fig 4.5.1: Layout Design of 2 - bit Multiplier.

So in above we can see that layout design of the 2 – Bit Multiplier and it's DRC (Design Rule Check) was verified on Microwind spice tool. It's area is 53.8 μm^2.

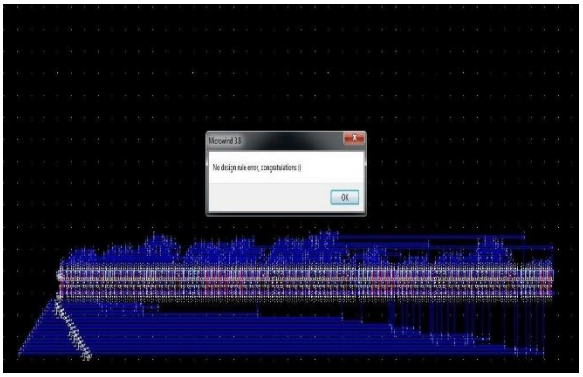


Fig 4.5.2: Layout Design of Carry Save Adder 1

In above we can see that layout design of the CSA 1 and it's DRC (Design Rule Check) was verified on Microwind spice tool. It's area is 72.7 μm^2

Fig 4.5.3: Layout Design of Carry Save Adder 2

In above we can see that layout design of the CSA 2 and it's DRC (Design Rule Check) was verified on Microwind spice tool. It's area is 72.7 μm^2

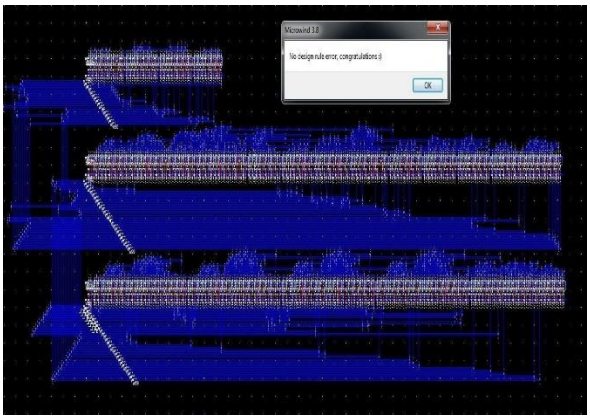


Fig 4.5.4: Layout Design of Inverted Gate Vedic Multiplier.

In above figure is shows that layout design of the inverted gate vedic multiplier and we verified design rule check (DRC).

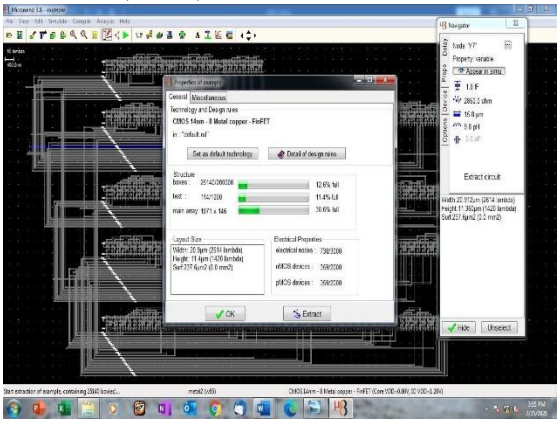


Fig 4.5.5: Area Report of the Design

In above figure we can see the area report of the design and here we can note that no of cells and no of electrical nodes. So we area is 898.6 μm^2 for 45 nm Gpdk technology and 2752.1 μm^2 for 65 nm Gpdk technology, 4549.4 μm^2 for 90 nm.

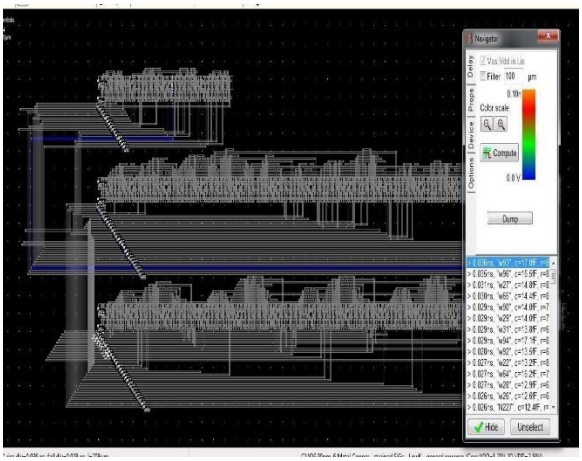


Fig 4.5.6 : Delay Report of the Design

In above we can see that Global delay of the design. So here we can get particular path delay but here we are providing worst delay of the design. By clicking on the Analysis →Global Delay then we can get several paths with their parasitic values like Capacitance and resistance then if you click on desired path then we can get the delay report and the respective path can highlight. So we delay is 0.27 ns for 45 nm Gpdk technology and 0.54 ns for 65 nm Gpdk technology, 0.72 ns for 90 nm.

5.SIMULATION RESUL

The importance of calculating the delay of any circuit is to estimate the speed of the circuit. Now a day's technology is rapidly changing, and every electronic circuit needs some factors (speed, portability, less power consumption) efficiently. In this project concentrated mainly on the area and speed.

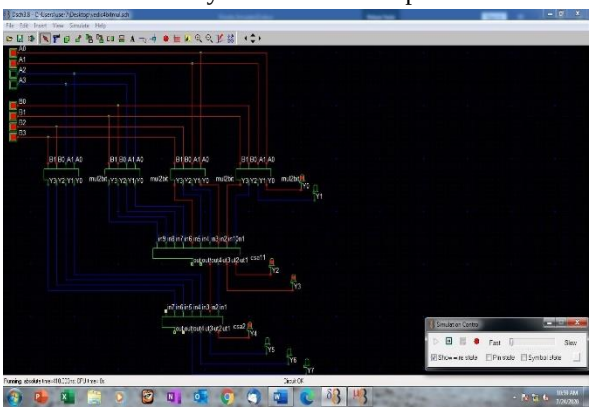


Fig 5.1 Simulation of Inverted Gate Vedic Multiplier.

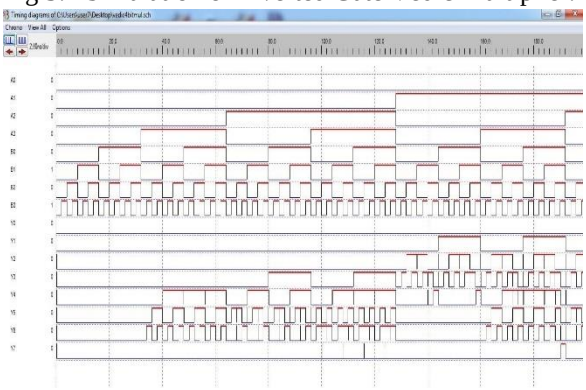
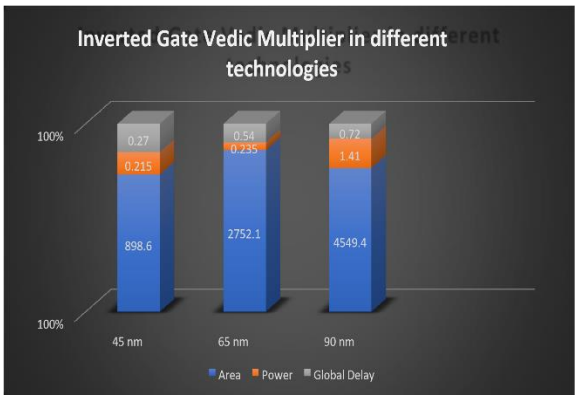


Fig 5.2 Wave form of Inverted Gate Vedic Multiplier.

The figure shows that simulation wave form of the Inverted Gate Vedic Multiplier. So here we can observe the functionality of the Vedic Multiplier output. Based on wave forms we can calculate the delay of the design manually.



From the figure we can observe the area, power, delay in different Gpdk TSMC technologies those are 45, 65, 90 nm Gpdk technologies. As per our observation compared to 45 nm with 65 nm technology 45 nm technology is better because of while comparing their parameters like power, delay and area. 65 nm technology consumes more. And compared with 65 nm with 90 nm technology 65 nm technology is better, while comparing 45, 65, 90 nm Gpdk technologies 45 nm technology best one.

Parameter	45nm	65nm	90nm
Area (μm^2)	898.6	2752.1	4549.9
Power (mW)	0.215	0.235	1.410
Global Delay (ns)	0.27	0.54	0.72

Table 1: Area, Power, Global Delay in 45, 65, 90nm technology.

6.CONCLUSION

The 4- bit Inverted Gate Vedic Multiplier designed the combination of Carry Save adder and 2-bit multiplier. And 4 – Bit Vedic multiplier has been simulated using Micro Wind Tools in General Purpose Design Kit (GPDK) 45, 65, 90 nm CMOS technologies. And observed the differences of power consumption, Global Delay and Area of the 4-bit Inverted Gate Vedic multiplier in 45, 65, 90nm General Purpose Design Kit (GPDK). The Inverted Gate Vedic multiplier is able to yield a full output voltage swing with a power consumption is 0.215 mW in 45nm , 0.235 mW in 65nm and 1.410 mW in 90 nm Delay of 0.27 ns in 45nm, 0.54 ns and 0.72 ns. Compact area of 898.6 μm^2 in 45nm, 2752.1 in 65nm, 4549.4 μm^2 in 90 nm.

In this approach, the Inverted Gate Vedic Multiplier is designed in three different GPDK of CMOS technology those are 45, 65, 90 nm. Have been

analyzed in terms of speed power consumption and power delay products. The analysis showed that the 45 nm Inverted Gate Vedic Multiplier is more suitable for low power applications as a Inverted Gate Vedic multiplier.

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