Design of Ultra Low Voltage GDI Based 10T,12T, 14T Full Adders in TSMC GPDK of 45 NM Technology

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***Abstract* - Addition is a vital arithmetic operation and act as a building block for synthesizing all other operation. A high-performance adder is one of the key components in the design of the application specific integrated circuits. In this approach, three low power GDI full adders designed in TSMC GPDK of 45 nm technology on Micro wind EDA tools. And analyzed the power, area and speed of the design.**

***Index Terms* - GDI Technique, Full Adder, XNOR based full adder , TSMC GPDK 45nm, Layout, Schematics,**

1.INTRODUCTION

This project is dealing with importance of GDI Based Full Adder in current Electronics Industry.
Because of its vital role, concentrated on design metrics of CMOS and GDI based full adders. By using GDI (Gate Diffusion Input) Technology designed the Different Full adders (10T,12T and 14T) which has good design metrics compared to CMOS Technology.
In Designing of 10T,12T and 14T GDI Full Adder used 45nm Technology. Based on this technology designed Schematics and layouts. And calculated the delay.

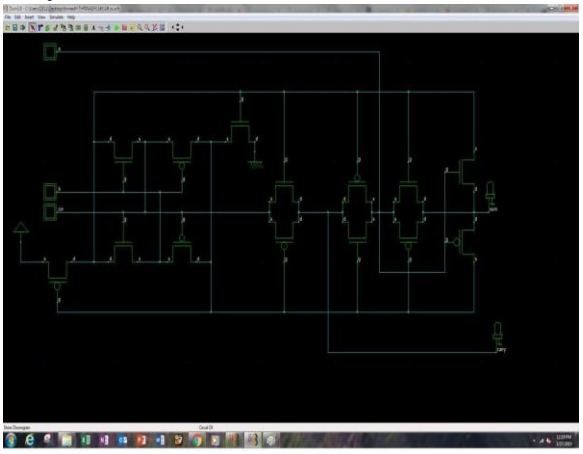


Fig 1.1 14T GDI Full Adder

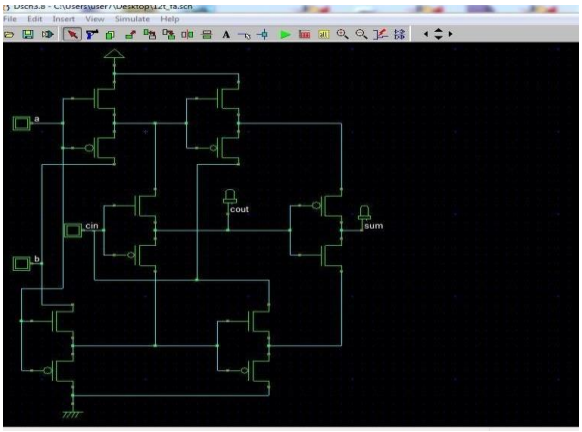


Fig 1.2 12T GDI Full Adder

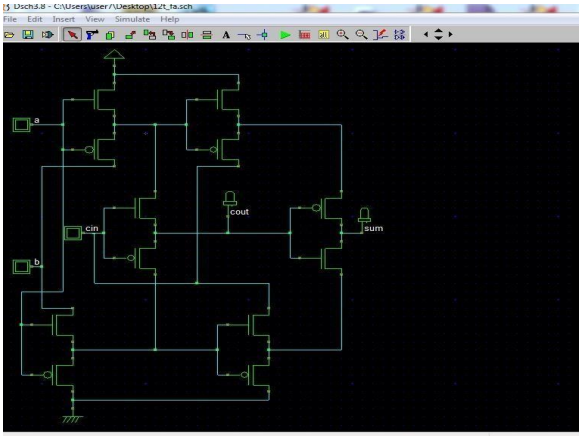


Fig 1.3 10T GDI Full Adder

1. Adders

1.1 High Speed Adders

Introduction Digital computer arithmetic is an aspect of logic design with the objective 1of developing appropriate algorithms to achieve an efficient utilization of the available hardware [1-4]. Given that the hardware can only perform a relatively simple and primitive set of Boolean operations, arithmetic operations are based on a hierarchy of operations that are built upon the simple ones. Since ultimately, speed, power and chip area are the most often used measures of the efficiency of an algorithm, there is a strong link

between the algorithms and technology used for its implementation.

Half Adder

Half adder is a combinational logic circuit. The half adder accepts two binary digits on its inputs and produce two binary digits outputs, a sum bit and a carry bit. The half adder is an example of a simple, functional digital circuit built from two logic gates. The half adder adds to one-bit binary numbers (AB). The output is the sum of the two bits (S) and the carry (C)

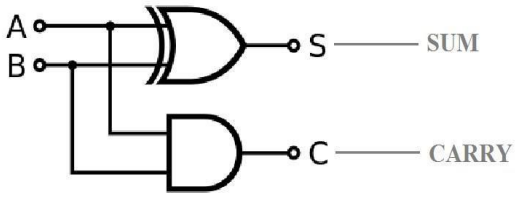


Fig 2.1.1 Half Adder Block Diagram

Full Adder

Full adder is a combinational logic circuit. Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A full adder logic is designed in such a manner that can take eight inputs together to create a byte wide adder and cascade the carry bit from one adder to the another.

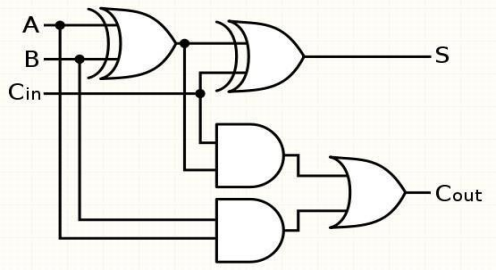


Fig 2.1.2 Full Adder block Diagram

2.2.1 Truth table for Half Adder

Input		Output	
A	B	Sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2.2.2 Truth Table for Full Adder

Inputs1			Outputs	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2. GDI Adders

A new technique of low power digital circuit design is GDI. This technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. Performance comparison with traditional CMOS and various PTL design techniques is presented, with respect to the layout area, number of devices, delay and power dissipation, showing advantages and drawbacks of GDI as compared to other methods. A variety of logic gates have been implemented in 0.35μm technology to compare the GDI technique with CMOS and PTL.

The GDI method is based on the use of a simple cell as shown in Figure 3.1. One may be reminded of the standard CMOS inverter at the first glance of this circuit, but there are some important differences: The GDI cell contains three inputs—G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased in contrast to CMOS inverter

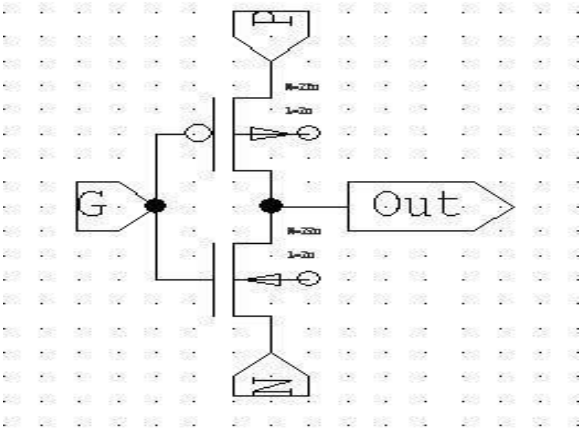


Figure 3.1 Basic Gate-Diffusion-Input Cell

The GDI cell with four ports can be recognized as a newly multifunctional device, which can achieve six functions with different combinations of inputs G, P and N. Table 3.1 shows that simple configuration changes in the inputs G, P, and N of the basic GDI cell can lead to very different Boolean.

Table 3. 1 Functions of the Basic GDI Cell

Input			Out	Function
P	G	N		
B	A	0	l.B	F1
1	A	B	l+ B	F2
B	A	1	A+ B	OR
0	A	B	A.B	AND
B	A	C	l.B+A.C	MUX
1	A	0	l	NOT
Input			Out	Function
P	G	N		
B	A	0	l.B	F1
1	A	B	l+ B	F2
B	A	1	A+ B	OR
0	A	B	A.B	AND
B	A	C	l.B+A.C	MUX
1	A	0	l	NOT

Functions (Callaway and Swartz lander 1996) at the output. Most of these functions are complex (usually consuming 6-12 transistors) in CMOS, while they are very simple (only 2 transistors per function) in the GDI design methodology. Meanwhile, multiple-input gates can be implemented by combining several GDI cells (Po-Ming lee et al 2007).

The GDI based on XOR and XNOR gates cells are, in fact, applications of the GDI technique. As shown in Figure 3.2, each of them requires only four transistors. Obviously, the proposed GDI XOR and XNOR gates use less transistors compared with the conventional CMOS counterparts. Owing to some attractive features which allow improvements in design complexity.

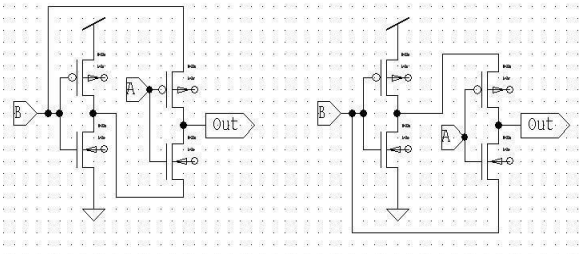


Figure 3.2 (a) GDI XOR gate (b) GDI XNOR gate

Transistor counts, static power dissipation and logic level swing, research on GDI is becoming vigorous in VLSI area. But, the GDI scheme suffers from the need for special CMOS process. Specifically, it requires twin-well CMOS or Silicon on Insulator (SOI) process (Bui et al 2002)], which are more expensive than the standard p-well CMOS process. This challenges its applicability in many CMOS circuits. Two design strategies have been used to size each topology. The former aims to minimize power consumption, adopting minimum. size transistors and the latter achieve minimum PDP by suitable transistor sizing. Then the Performance for both design strategies has been compared for different supply voltage values.

3.1 GDI 14-T Full Adder

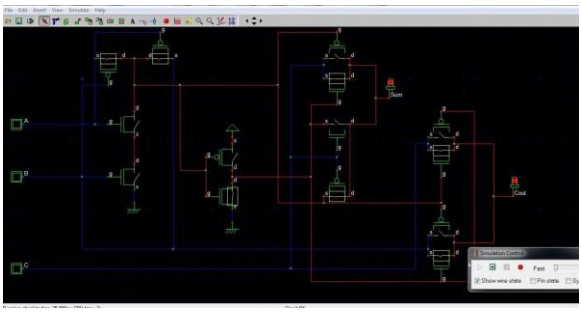


Figure 3.1.1 14 T Full Adder Cell.

Figure shows the schematic configuration of the full adder cell consisting of 14 Transistors. It ensures both low power and high-speed performance. The power consumed by this circuit is less when compared with that of 10T GDI full adder (Roy and Prasad 2000) and more compared with 10TSERF full adder (Matsuzawa 19994).

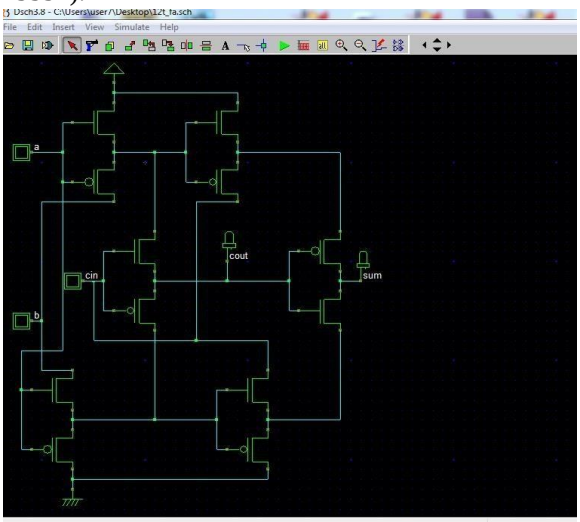


Figure 3.1.2 GDI XNOR based 12 T Full Adder Cell.

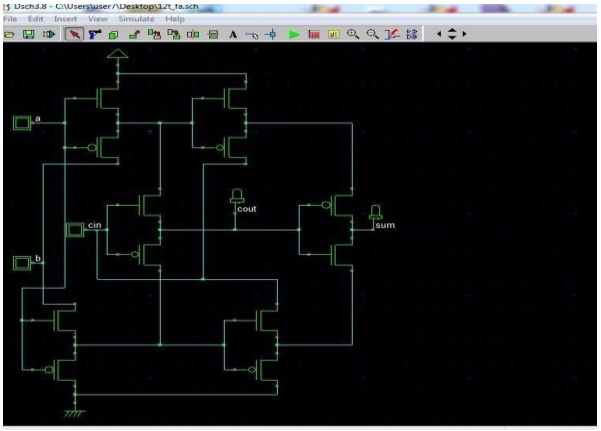


Figure 3.1.3 GDI XNOR based 10 T Full Adder Cell.

To overcome the low output voltage swing of the SERF adder cell, the GDI XNOR based 10 T adder cell is proposed. The proposed design has the advantages of flexibility, less transistor counts.

3. LAYOUT DESIGNING OF ULTRA LOW VOLTAGE BASED 10T,12T,14T FULL ADDERS

3.1 Layout Designing of 14T Full Adder

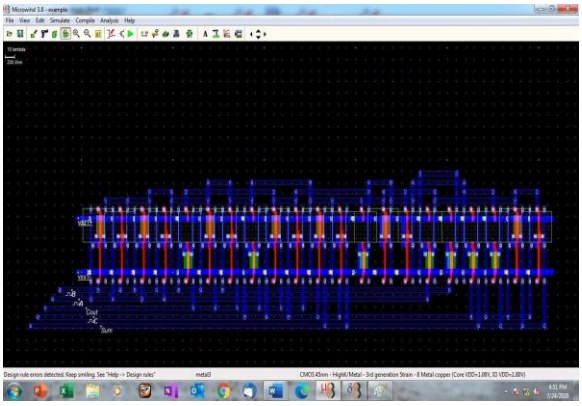


Fig 4.1.1 Layout Design of GDI based 14T Full Adder

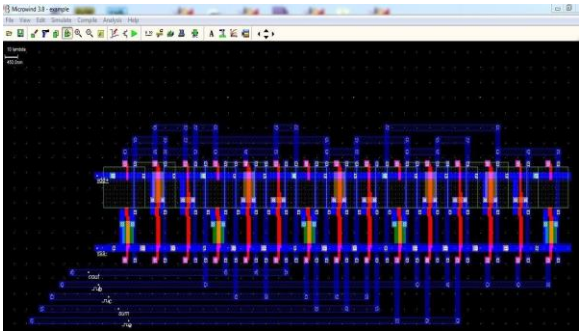


Fig 4.1.2 Layout Design of GDI based 12T Full Adder

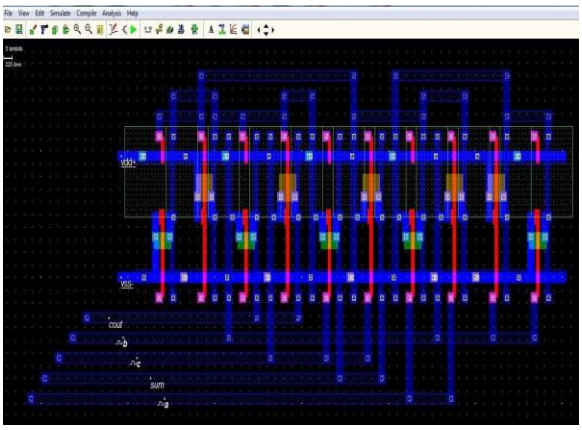


Fig 4.1.3 Layout Design of GDI based 10T Full Adder

4. SIMULATION RESULTS AND WAVE FORMS OF THE DESIGNS

As we observed in designing the number of transistors required to Design the GDI based Full Adder. And also observe the simulation of the adders.

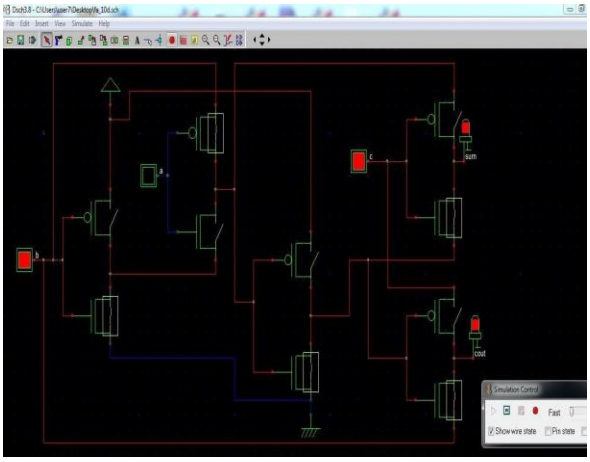


Fig 5.1.1 Simulation of GDI Based 10T Full Adder

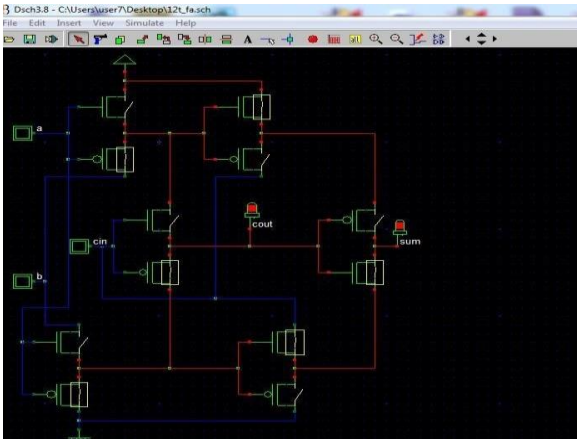


Fig 5.1.2 Simulation of GDI based 12T Full Adder

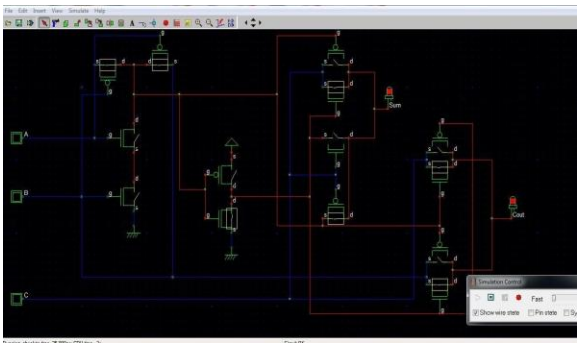


Fig 5.1.3 Simulation of GDI based 14T Full Adder

In the above screenshots the simulation of GDI based 10T Full Adder, GDI based 12T Full Adder and 14T Full Adders are present. From the screenshots we can summarize the below table

Technology	No. of symbols	No. of Lines
GDI based 10T	16	60
GDI based 12T	22	65
GDI based 14T	21	77

Table 5.1 Property Analysis

From the table we can observe the GDI technology is less complexity technology we can observe for each stage the symbols and lines are decreasing.

5.2 Wave forms of 14T, 12T, 10T Full Adder designs.

The importance of calculating the delay of any circuit is to estimate the speed of the circuit. Now a day's technology is rapidly changing, and every electronic circuit needs some factors (speed, portability, less power consumption) efficiently. In this project concentrated mainly on the area and speed.

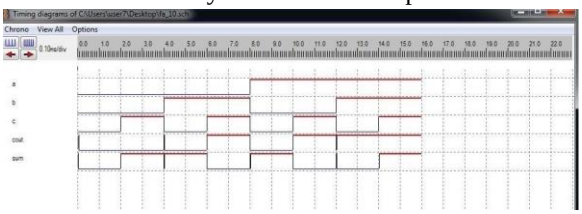


Fig 5.2.1 Simulation of GDI based 10T Full Adder

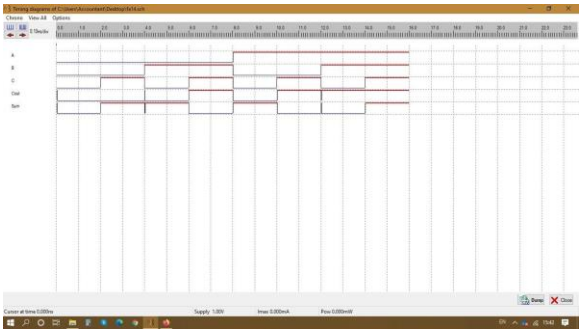


Fig 5.2.2 Simulation of GDI based 10T Full Adder

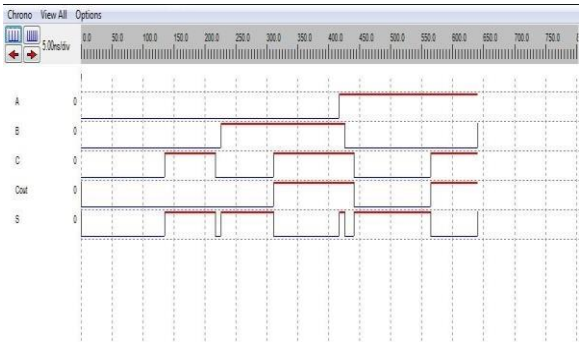


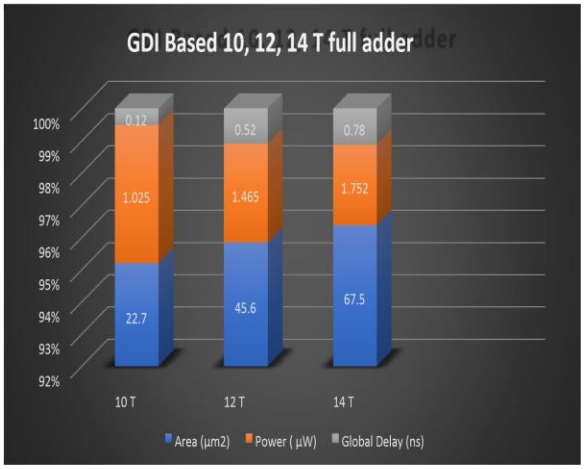
Fig 5.2.3 Simulation of GDI based 10T Full Adder

In above figures 5.2.1, 5.2.2, 5.2.3 are 10T, 12T, 14T GDI Based full adders simulation wave forms so here we can verify the functionality of the Full adder by giving know inputs and will get the out. Like if I give a = 1, b =1, c = 1 then out of sum = 1 carry = 1. This functionality was satisfied here.

5. CONCLUSION

Full adder Circuit is a very important component in the design of application of the integrated circuits in VLSI. The main objective of these full adders is providing high speed, low power, compact area also provide good voltage swing. Compared the most important parameters of the design those are Area, Power, Global Delay.

Comparison of the Different GDI based full adders.



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