Effective GDI Based Array Multiplier and Braun Multiplier with TSMC 45nm

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***Abstract* - In the recent trends of any application depends on delay, area, and Power consumption. The delay, area and power consumption are the three important considerations of the industrial. These three parameters are considered for any industry application. This type of application can be developed by the different methods that are used in VLSI technology. The Array Multiplier and Braun multiplier was developed by GDI method. Braun multiplier is helpful for increasing the speed of the system. The Array multiplier and Braun multipliers are designed in the Micro Wind DSCH (Schematics) and Micro Wind 3.8 (Layout) EDA tool.**

1.INTRODUCTION

Due to the heavy interest in usage of digital integrated circuits for portable devices such as cellular communications, phones, battery, laptops, and personal digital assistant (PDAs), etc., the need for small chip circuits, power consumption and speed are vital factors should be taken into consideration while choosing the VLSI design with high performance. An addition is a basic arithmetic operation heavily demanded in VLSI design such as multiplier and accumulator (MAC), microprocessor, digital signal processing applications, so the system performance will be affected by the performance of full adder. A full adder is essential in the arithmetic operation such as division, subtraction, addition, and multiplication.

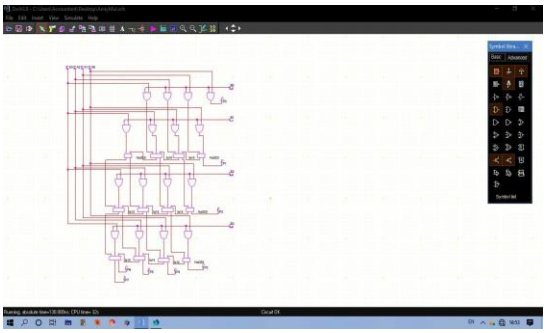

Fig 1.1 : Schematic Design of 4 x 4 Array Multiplier

Enhancing energy will influence the whole system so energy must be improved. This can be achieved by GDI technique. The aim of this work is to design 4 – bit multiplier using a full adder circuit based on full swing GDI to reduce power consumption, delay, and area in addition to achieve full-swing output with high performance.

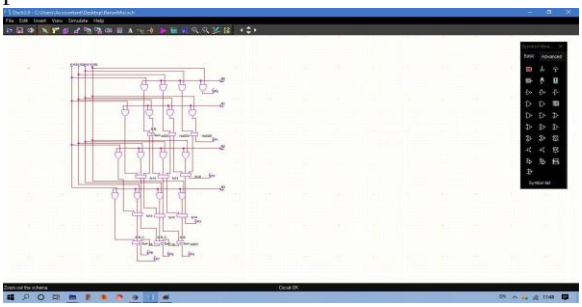

Fig 1.2: Schematic Design of Braun Multiplier

2. MULTIPLIER

A multiplier is one of the key hardware blocks in the most digital signal processing (DSP) system. Typically, DSP application where a multiplier plays an important role include digital filtering, digital communications, and spectral analysis (Ayman, A et al (2001)). analysis (Ayman. An et al (2001)). Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design. Multiplications are very expensive and slows the overall operation.

2a. Array Multiplier

The composition of an array multiplier is shown in the figure There is a one to one topological correspondence between this hardware structure and the manual multiplication shown in figure the

generation of n partial products requires N*M two bit AND gates. Most of the area of the multiplier is devoted to the adding of n partial products, which requires N-1, M-bit adders. The shifting of the partial products for their proper alignment‘s performed by simple routing and does not require any logic. The overall structure can be easily be compacted into rectangle, resulting in very efficient layout.

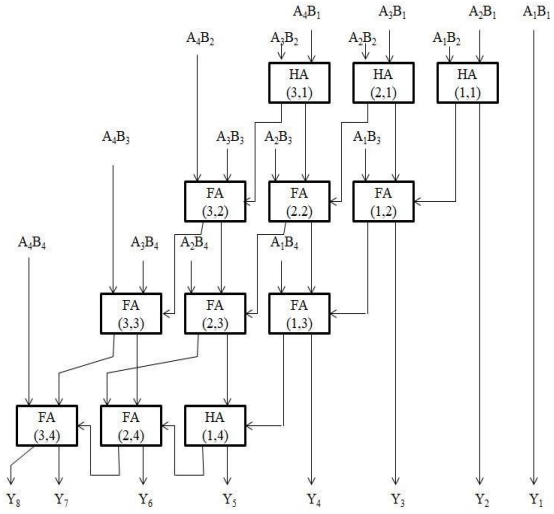

Fig 2a : Array Multiplier.

2b. Braun Multiplier.

The simplest parallel multiplier is the Braun array. All the partial products are computed in the parallel , Then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. Note that this multiplier is only suited for positive operands. The structure of the Braun algorithm for the unsigned binary multiplication is shown in the figure.

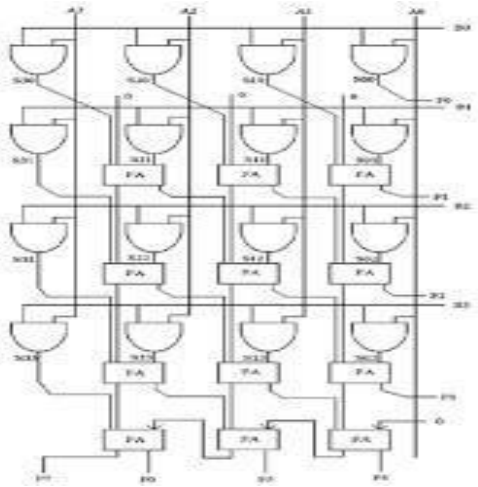

Fig 2b : Braun Multiplier.

3. GDI (GATE DIFFUSION INPUT)

A new technique of low power digital circuit design is GDI. This technique allows reducing power consumption, Delay, and Area of digital circuits, while maintaining low complexity of logic design. Performance comparison with traditional CMOS and various PTL design techniques is presented, with respect to the layout area, number of devices, delay and power dissipation, showing advantages and drawbacks of GDI as compared to other methods. A variety of logic gates have been implemented in 0.35μm technology to compare the GDI technique with CMOS and PTL.

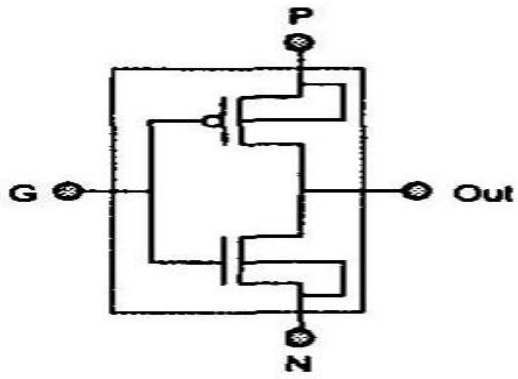

Fig 3.1 : GDI Basic Cell

GDI method is based on the use of a simple cell as shown in GDI basic cell. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences: GDI cell contains 3 inputs-G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), N (input to the source/drain of nMOS). It must be remarked that not all the functions are possible in standard p-well CMOS process, but can be successfully implemented in twin-well CMOS or SOI technologies. Table 3.1 shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions.

Most of these functions are complex (6 -12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method. The reasons for this are as follows: 1) F1 is a complete logic family(allows realization of any possible 2-input logic function),), 2) F1 is the only GDI function that can be realized in a standard p-well CMOS process, because the bulk of any nMOS is constantly and equally biased.

As can be seen, GDI cell structure is different from the existing PTL techniques, and has some important features, which allows improvements in design complexity level, transistor count, static power dissipation and logic level swing. Understanding of GDI cell properties demand a deeper operational analysis of the basic cell in different cases and configurations.

N	P	G	Out	Function
'0'	B	A	$\acute{A}B$	F1
B	'1'	A	$\acute{A}+B$	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\acute{A}B+AC$	MUX
'0'	'1'	A	$\acute{A}$	NOT

Table 3.1: Various logic functions of GDI cell for different input configurations.

4. GDI BASED ARRAY AND BRAUN MULTIPLIER

4.1 GDI based full adder.

The Proposed full adder design employs only 14 transistors. It mainly consists of five logical blocks designed using MVT-GDI technique. One XOR/ XNOR, two multiplexers, one Swing Restored Transmission Gate (SRTG), and other Swing Restored Pass Transistor (SRPT) block. The XOR/XNOR block is designed using GDI Technique. Since the inverters used in the XOR/XNOR blocks has no voltage drop, they are incorporated with standard VT devices. Since the GDI MUX-1, multiplexes the output of the XOR (A ⊕ B) and the XNOR (A XNOR B) with a control input (Cin) to obtain the sum function Sum = Cin (A ⊕ B) + *C*in(A ⊙ B. The generated by the GDI MUX – 2, which multiplexes the inputs Cin and B with control line (A XNOR B). Cout = (A ⊙ B) *C*in + (A ⊙ B)B.

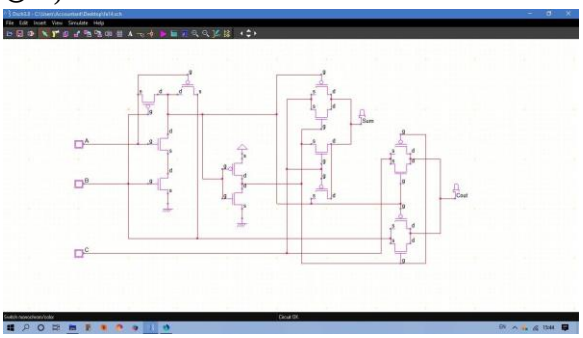

Fig 4.1 : GDI based 14 T Full adder.

However, the proposed structure looks similar to many previous XOR/XNOR logic-based designs and authors' previous GDI-based design [25], but none of the previous designs provides full swing is ensured using a SRTG at the output of the sum and SRPT's at the carry output (*C*out). The functionality of this full adder with respect to states of the transistors is shown in Table 4. It can be observed that the swing restoration transistors (M11, M12, M13, M14) are _ON' when there is a *VT* drop at the output of the sum generation GDI MUX1 and *C*out generation GDI MUX-2 to provide full swing logic. Since there is no *VT* drop at the output in most of the cases as stated in Table 4, the transistors (M11, M12, M13, M14) are also incorporated with standard VT transistors.

4.2. GDI based Array Multiplier

Array multiplier is the simplest structure of parallel multiplier. This multiplier using the standard add and shift operation based on 'add and shift' algorithms to perform a multiplication operation. The partial products generator consists of n number of 'AND' gates to multiply the multiplicand with each bit of the multiplier and then these partial products are shifted depending on their order and this summation operation can be performed by using full adder and a half adder. In 4x4 array multiplier, 4x4 AND gates used to generate partial products and 4x (4-2) full adders and 4 half adders used to generate. Here design is done using GDI technology.

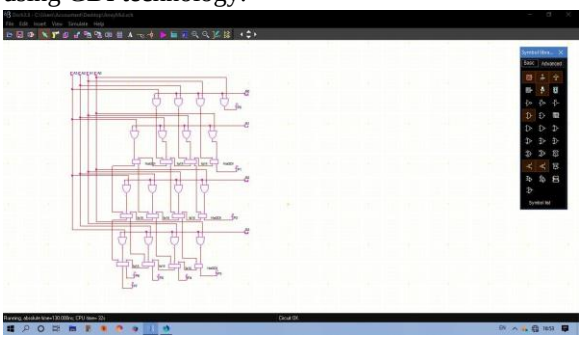

Fig 4.2 : GDI based Array Multiplier.

4.3 GDI based Braun Multiplier.

Braun multiplier is a linear multiplier, which has a regular structure and known as carry-save array multiplier. This multiplier operates based on the fact that does not add immediately "the carry bits" that are outputs of the first stage but are saved for the next addition stage. 4x4 Braun multiplier, which consists of

(41) rows of carry-save adders (CSAs) and a (4-1) bit ripple-carry adder in the last row and each row contains (4-1) full adder (FAs). The main advantage of Braun multiplier that it has only one critical path rather than many paths found in the array multiplier and this is the most widely used in DSP applications due to consuming low power.

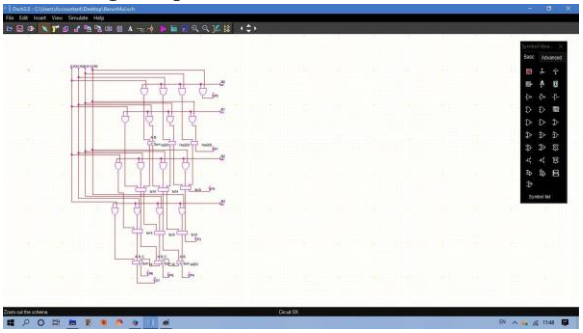

Fig 4.3: GDI based Braun multiplier

5. SCHEMATIC AND LAYOUT DESIGNS OF ARRAY AND BRAUN MULTIPLIER IN 45 NM TECHNOLOGY

5.1 Schematic design of 4 x 4 Array Multiplier.

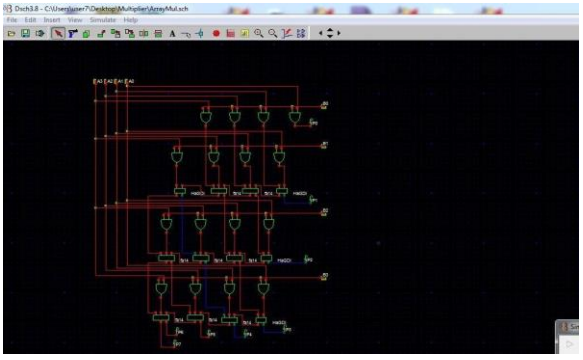

Fig 5.1: Schematic designing of 4 x 4 Array multiplier

5.2 Layout Designing of 4 x 4 Array Multiplier

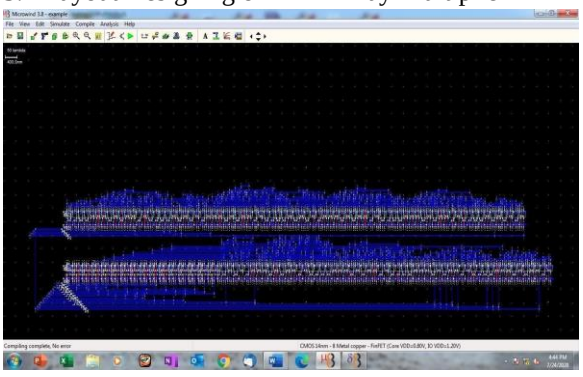

Fig 5.2: Layout designing of 4 x 4 Array multiplier

5.3 Schematic Designing of 4 x 4 Braun Multiplier.

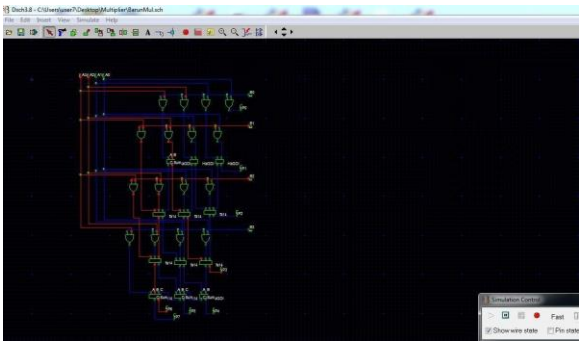

Fig 5.3: Schematic designing of 4 x 4 Braun multiplier

5.4 Layout Designing of 4 x 4 Braun Multiplier.

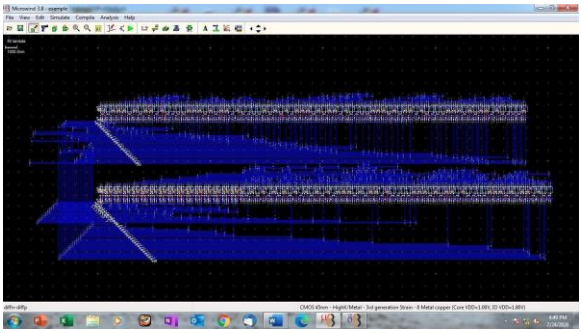

Fig 5.4: Layout designing of 4 x 4 Braun multiplier

6. SIMULATION RESULT AND WAVEFORMS

The importance of calculating the delay of any circuit is to estimate the speed of the circuit. Now a day's technology is rapidly changing, and every electronic circuit needs some factors (speed, portability, less power consumption) efficiently. In this project concentrated mainly on the area and speed and power consumption.

6.1 Simulation of Array Multiplier and Braun Multiplier.

First simulated the design by forcing the known inputs. After that generated the waveforms. So here simulated the design

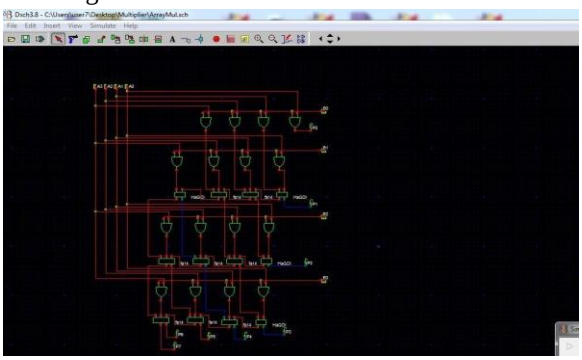

Fig 6.1.1: Simulation of 4 x 4 Array multiplier

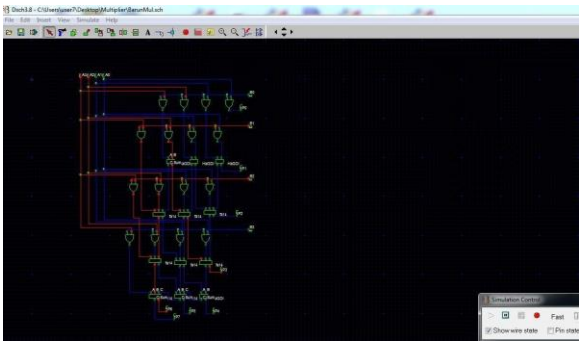

Fig 6.1.2: Simulation of 4 x 4 Braun multiplier

The above figure shows that simulation of Braun Multiplier in GPDK of 45 nm technology.

6.2 Wave forms of Array Multiplier & Braun Multiplier

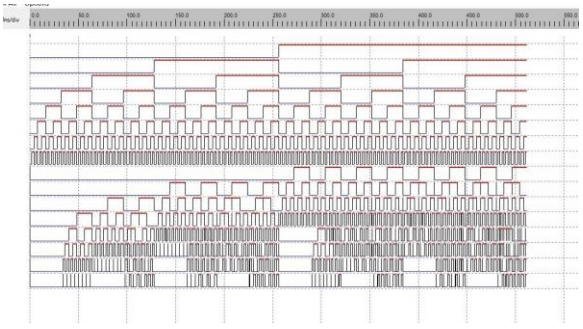

Fig 6.2.1: Waveform of 4 x 4 Array Multiplier.

The figure shows that simulation wave form of the 4 x 4 Array Multiplier. So here we can observe the functionality of the 4 x 4 Array Multiplier output. Based on wave forms we can calculate the delay of the design manually.

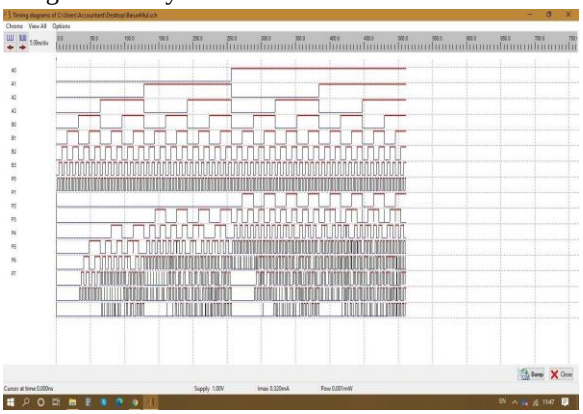

Fig 6.2.2 : Waveform of 4 x 4 Braun Multiplier.

The figure shows that simulation wave form of the 4 x 4 Braun Multiplier. So here we can observe the functionality of the 4 x 4 Braun Multiplier output. Based on wave forms we can calculate the delay of the design manually.

Design Parameter in 45nm	Braun Multiplier	Array Multiplier
Area (μm^2)	2245.4	3379.4
Power (µW)	35.495	50.036
Global Delay (ns)	0.13	0.18

The Array multiplier and Braun multiplier can be used in the applications where the speed of the operation is to be increasing. These multipliers are implemented on GDI technique it is better compared to CMOS. The Braun and Array multipliers able to yield a full output voltage swing with a power consumptions are respectively 35.495 µW , 50.036 µW in 45nm and Global delays Braun and Array Multipliers are respectively 0.13 ns, 0.18 in 45nm, Finally compact area of Braun and Array multiplier are respectively 2245.4 μm^2, 3379.4 μm^2 in 45nm.

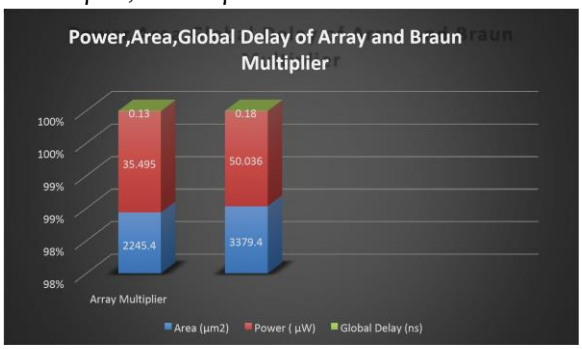

Fig 7.1: Power, Area, Global Delay comparison of Array and Braun Multiplier.

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