Seven Level Fault Tolerant Inverter for Photovoltaic Applications

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Abstract **- This paper reveals a seven-level inverter topology for photo-voltaic (PV) power generation system. The 7- level inverter created by cascading single phase full and half bridge inverter topology sustained with three separate PV strings. The output has 7-levels: +Vdc, +2/3Vdc, +Vdc/3, 0, Vdc/3, -2Vdc/3, -Vdc. The 7-level inverter function is possible by using seven semiconductor switches. The designed inverter configuration has able to maintain consistent operation as inverter even though there is source and semiconductor switch breakdown. The developed inverter is differentiating with conventional multilevel inverters in terms of number of components, losses, and reliability. The result of a 7-level inverter topology is confirmed by using MATLAB/SIMULINK software.**

Index Terms **- 7-level inverter, PV generation system, reliability.**

I.INTRODUCTION

As the world is facing with shortage of fossil fuels there is an enormous amount of demand for renewable sources especially wind and solar energy. PV sources are used in wide areas as they are pollution free and easy to maintain. Cost of production of sun energy-based power generation is decreasing and meeting the consumer needs. The price of production is decreased to half of the cost of production of thermal energy in developed countries like U.S.A [1].

Multilevel inverters are used in many applications due to their high voltage withstanding and high-power conversion capabilities. Interest for multilevel inverters, day by day it is continuing expanding because of its superior qualities like high voltage operation capability, low switching losses, high efficiency [2]. The multilevel inverter has been used in a variety of applications ranging from intermediate to high-power levels, such as electric drives, power strengthening devices, also conventional or sustainable power generation and distribution system [3].

In the past so many varieties of converters are designed to operate as multilevel inverter, those are cascaded H-bridge, diode clamped and flying capacitor multi-level inverter these all treated as conventional multi-level inverters. Decrement of Total harmonic distortion (THD) in output voltage of inverter is possible with increment of number of output voltage levels. If it is done with conventional multi-level inverters need more switching components count as the number of output voltage level increases. It leads to increment of size of the inverter and difficulty level of control increases [4]. Unlike conventional multilevel inverters, different topologies which can reduce the switching losses are welcomed in [5-7]. A 5-level fault-tolerant inverter configuration with reduced number of switches and with energy balancing between sources is presented in [8]. A new multilevel inverter topology in [9] using reverse voltage component concept to overcome the drawbacks of conventional multilevel inverter proposed but, it uses more switches for lower levels.

The above issues are addressed by using a seven- level fault tolerant inverter which is superior to conventional multi-level inverters. Out of all conventional inverter topologies the planned inverter configuration has an excellent inherent feature i.e., it can be able to operate as inverter with decreased number of output voltage levels in case of failure in semiconductor device and source. The paper is organised as follows: the inverter configuration and operation are discussed in segment-II and the simulation results are discussed in segment-III and the advantage of proposed topology is concluded in segment IV.

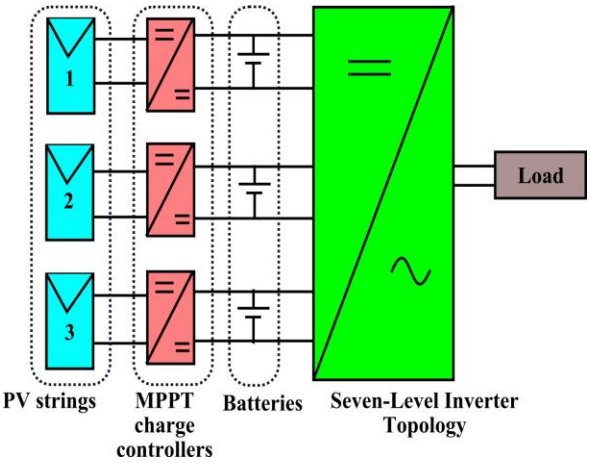

Fig. 1 Schematic diagram of seven-level inverter

II.SEVEN LEVEL FAULT TOLERANT INVERTER CONFIGURATION AND OPERATION

Multilevel inverter for multiple PV strings application concept is shown in schematic form in Figure 1. The multiple PV strings are possible for cascaded H-bridge configuration because it requires isolated sources which are not possible in case of diode clamped and flying capacitor multilevel inverters.

A. Conventional Cascaded H-bridge multilevel inverter

Fig.2 represents a cascaded H-bridge inverter with 7-level [10]. This topology needed three cascaded H-bridge modules, in which each one module is separately connected to individual DC voltage source. The output voltage generated by this topology is the sum of output voltage of each H-bridge module since all these module output terminals are connected in series to generate the high output voltage levels across the load. The highest possible output voltage with this is $V=V_1+V_2+V_3$. Where V stands for output voltage, V_1,V_2 and V_3 are the output voltages of the each H-Bridge module respectively. There are 7- level of output voltage i.e., $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $2V_{dc}$, $-3V_{dc}$. The primary favourable feature of cascaded HBridge inverter is that it requires least number of switching components. However, the principle detriment is that when the voltage level increases, the quantity of switches increments and furthermore the sources, this essentially expands the expense and weight. This issue can be addressed by replacing a new 7- level inverter which is later part of this section.

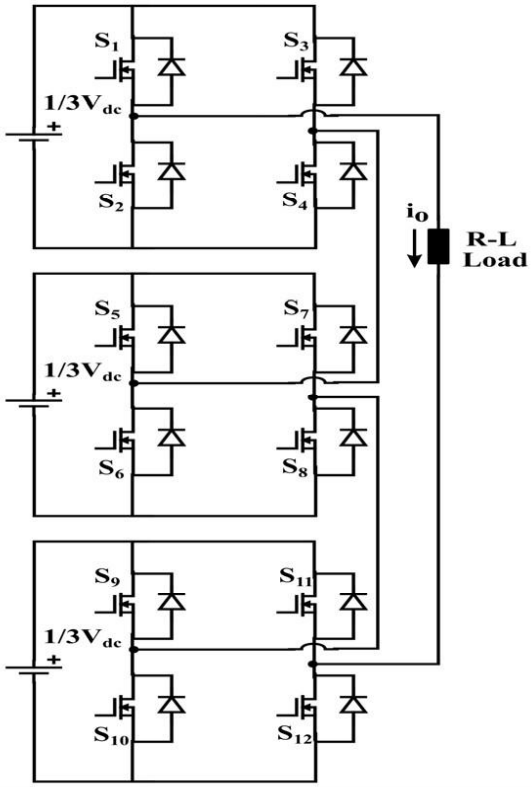

Fig.2 7- level cascaded H Bridge multilevel inverter [8]

TABLE I SWITCHING ARRANGEMENT CHART FOR 7-LEVEL OUTPUT VOLTAGE

S_1	S_2	S_3	S_4	S_5	S_6	S_7	Vo
1	0	0	1	1	0	0	+Vdc
1	0	0	1	0	0	1	+2Vdc/3
0	1	0	1	1	0	0	+Vdc/3
0	1	0	1	0	0	1	0
1	0	1	0	0	1	0	-Vdc/3
0	1	1	0	0	0	1	-2Vdc/3
0	1	1	0	0	1	0	-Vdc

B. Proposed seven-level fault tolerant inverter.

Fig.3 shows the seven-level fault tolerant inverter which is formed by cascading H Bridge and half bridge voltage source inverter. The half bridge inverter is modified with help of bi-lateral switch S7 (four quadrant operating semiconductor device), in which bi-lateral switch S7 is connected in between the two lower level (+1/3 Vdc) DC voltage sources which can be seen in fig.3. Under normal operating conditions with Proper switching control strategies, it has able to generate 7-level output voltage. i.e., +Vdc, +2Vdc/3, +Vdc/3, 0, -Vdc/3,2Vdc/3, -Vdc. The switching

patterns are shown in Table- I. The key role of bi-lateral switch S7 is, it made this converter to operate as an inverter even during fault conditions but with reduced output voltage level to avoid the interruption of power supply to the load.

In regular the inverter failures are occurs due to source failure, inverter switch failure, PCB failure and DC link capacitor failure [11]. The semiconductor switch failures are two types i.e., short and open circuit failure. In planned configuration open circuit switch failures and source failure is analyzed. The Table II shows the switching combinations in case different switch and source failure. During fault, it can generate only three level output voltage by maintaining interrupt free operation.

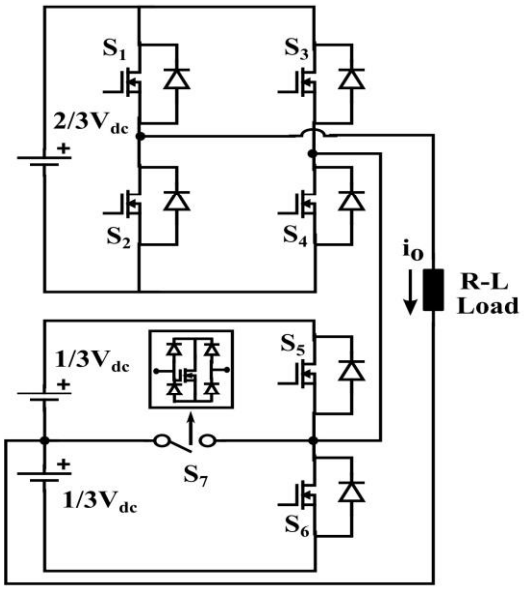

Fig .3 7- level fault tolerant inverter

TABLE II SWITCHING ARRANGEMENT FOR UNLIKE FAILURE CASES

	1/3Vdc source or S_5, S_6 switch open circuit failure						
Level of output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7
$+2/3V_{dc}$	1	0	0	1	0	0	1
0	1	0	1	0	0	0	1
$-2/3V_{dc}$	0	1	1	0	0	0	1
	2/3Vdc source or S1, S3 switch open circuit failure						
Level of output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7
$+1/3V_{dc}$	0	1	0	1	1	0	0
0	0	1	0	1	0	0	1
$-1/3V_{dc}$	1	0	1	0	0	1	0

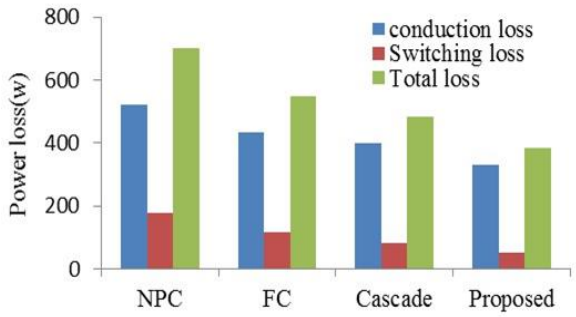

Fig. 4 . Power Loss of conventional and planned multi-level inverter.

The Table III shows the contrast of different 7-level topologies with planned topology. From Table III, it can be experiential that a reduced amount of components of planned inverter is sufficient enough to generate 7-level output. Therefore, the topology has less switching loss compared to other conventional multilevel inverters such as neutral point clamped (NPC), a flying capacitor (FC), and cascade H-bridge multilevel inverter which can be calculated using [13] and approximate losses are shown in fig.4. Here for a 100KW system the power losses are calculated for IGBT rating of FD300R06KE3 with the help of equations obtainable in [13].

Contrast of Different 7-Level Topologies

Nature of Elements	Number of Components Necessa In Conventional Topologies			Topology Proposed in [9]	Ry In Proposed Topology
	NPC	FC	H-bridge		
Switches	12	12	12	10	7
Diodes	10	0	0	0	4
DC sources	1	1	3	3	3
Capacitors	6	21	0	0	0
Fault Tolerance	No	No	Yes	No	Yes

III.SIMULATION AND RESULTS

The planned topology is designed and simulated in MATLAB/SIMULINK software. The three DC voltage sources magnitude of 200V, 100V and 100V. The load parameters are R=80Ω, L=40mH. The parameters are shown in Table IV.

TABLE IV PARAMETERS FOR SIMULATION

Source Voltage (Equal voltage)	V_1=200V,V_2=V_3=100V
Output voltage (rms)	232V
frequency of Modulating wave	f_m=50Hz
Carrier frequency	f_{cr}=2050Hz
Modulation index	m_a=0.98
Load Resistance, inductance values	R=80Ω, L=40mH

The Phase disposition carrier pulse width modulation technique for 7-level output voltage is shown in fig.5. The inverter switching pulses for 7-level output is generated by comparing the modulation signal (Vm) with six carriers (Vcr1-Vcr6) [13]. The load current waveform and 7-level output voltage is shown in fig.6. The fig.7 represents the load current and three-level output voltage during switch S6 open circuit fault. During fault the output voltage magnitude is reduced to 2/3Vdc. To maintain the same voltage rating as normal operation a transformer with tapping's on primary is suggested.

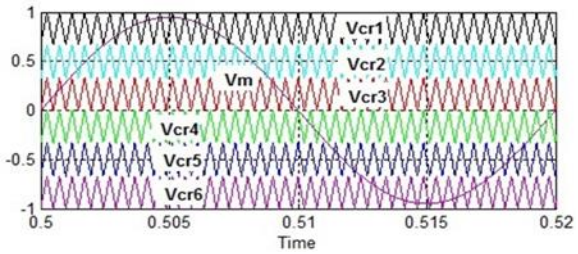

Fig.5. 7-level carrier pulse width modulation

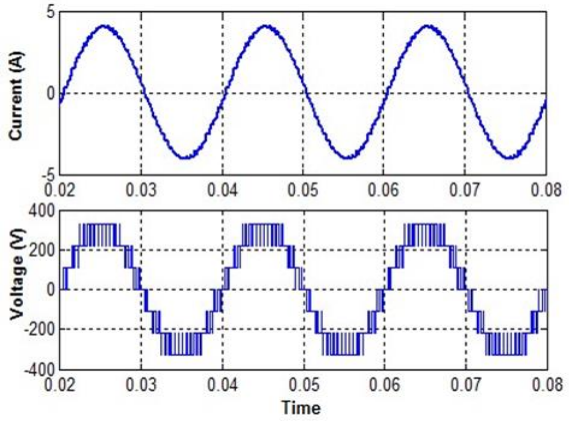

Fig. 6 Load voltage and current waveform

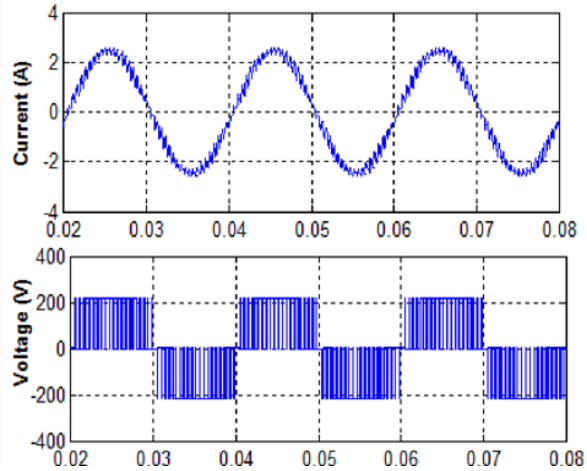

Fig.7 Load voltage and current waveform during switch S6 failure

The total harmonic distortion of load current and voltage waveform without filter is shown in fig.8 and fig.9. The voltage waveform THD is without filter at the load side of the inverter.

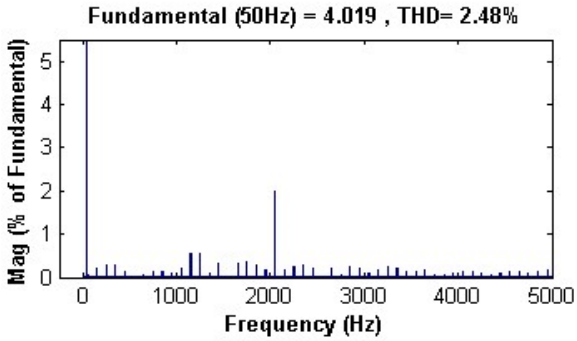

Fig.8 Current THD without filter

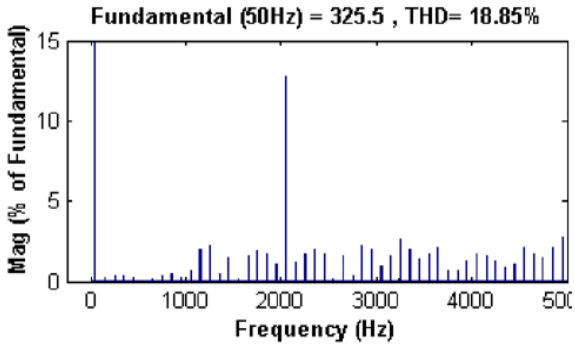

Fig. 9 Voltage THD without filter

IV. CONCLUSION

In this paper a 7-level fault tolerant inverter is presented for photovoltaic applications. The configuration shows that it needed a reduced amount of switching components than conventional multilevel inverters and some recently developed topologies. The topology not having capacitors and clamping diodes unlike flying capacitor multi-level inverter and diode clamped multilevel inverters. There is no capacitor voltage balancing and neutral point voltage balancing issues. The topology has less power loss because of lower number of switching devices. It also has the extra advantage of fault tolerance in terms of switch open circuit fault and source failure.

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