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Power Reduction in SRAM Cells Using Gated VDD Methodology

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Abstract - **The most significant component of portable battery-operated digital devices is memories. Since standard SRAM cells consume a lot of capacity, lowering memory power dissipation helps the device work better. In this new age of fast mobile computing, traditional SRAM cell designs are power hungry and underperforming. A static RAM with a low power consumption. The Gated VDD technique is used to investigate cell architecture. The SRAM cell's power consumption has been reduced using gated VDD and MTCMOS architecture techniques. In terms of power consumption and write delay, the results show that the MTCMOS-based SRAM cell is the best performer. Simulations are run on the Cadence Virtuoso tool, which uses 180nm technology.**

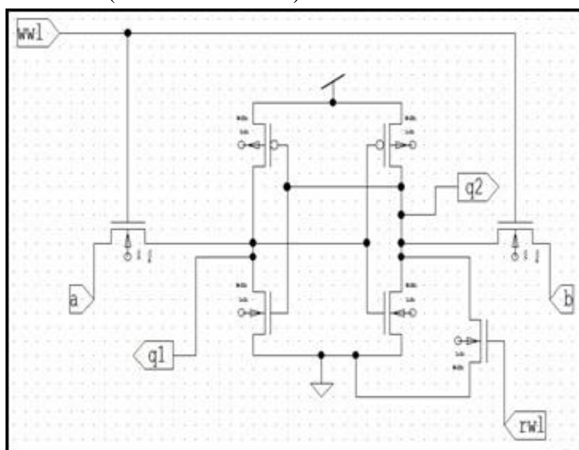
I.INTRODUCTION

Battery life is extremely important when it comes to using cartable devices. Many advanced devices have been created that require hardware architecture that is energy efficient. Energy-efficient hardware architecture is needed as new devices such as smart watches, small sensor nodes, wireless communication units, and so on are created. As long as power is supplied to the cell, static random-access memory (SRAM) cells do not need frequent refreshing to maintain their contents. This is why static random-access memory (SRAM) is favored over dynamic random-access memory (DRAM) (DRAM). A 7-transistor SRAM cell was engineered with a low supply voltage and performed well in terms of noise reduction. In terms of delay, Static Noise Margins (SNMs), and power consumption, different designs of 7T SRAM cells performed well. Leakage capacity is becoming a major source of power consumption as existing technologies scale down to deep submicron levels. The overall complexity of these circuits, relative to the traditional 6T SRAM cell, makes it more difficult to implement and ensure stable operation. SRAM architectures like 7T, 8T, and a novel 9T concept, the overall complexity of these circuits makes it more difficult to implement and ensure stable operation. As a result, Random Access Memory (RAM) chips are used in almost all digital systems. The work of Dynamic Random-Access Memory (DRAM) cells necessitates a periodic power refresh. Static Random-Access Memory (SRAM) cells, on the other hand, depend on a constant power supply. The Multi Threshold CMOS (MTCMOS) technique was applied to a 7T SRAM cell, yielding promising power reduction results. A SRAM cell with ten transistors is built that has a high Static Noise Margin (SNM) and a reduced power of about analyses a 9T Static RAM cell with stacking and dual threshold voltage to reduce leakage power.

The two SRAM cells are shown: one with NMOS pass transistors to reduce gate leakage current and the other with PMOS pass transistors to reduce gate leakage current. A new model of 7T SRAM cell was developed that performed well in terms of delay but dissipated more power, which could be reduced using power reduction techniques. The delay and power consumption of various SRAM cells have been planned and analyzed. The delay and power parameters were compared to those of a traditional 6T SRAM cell using gated VDD and MTCMOS design techniques. The Gated VDD technique is used to reduce the amount of power consumed by the Static RAM cell, which is comparable to regular 6T and 7T Static RAM cells. The papers are organized in the following pattern. Section-II depicts a typical 6T static RAM cell, while Section-III illustrates how a 7T static RAM cell works.

II 7T SRAM CELL

A 7t a static RAM cell displayed uses two PMOS Transistors labeled an m1 and an m3, and two NMOS Transistors labeled an m2 and an m4 which are cross coupled to each other to stabilize the inverters to their respective state. Two more NMOS transistors labeled M5 and M6, which act as pass transistors are connected to the nodes Q and respectively. Additional transistor labeled a m7 is connected in correspondence to the M4 transistor who's a gate terminal is given to the RWL (Read Word Line).



7T SRAM Cell

When WWL (Write Word Line) gets charged, the write operation will be achieved with the help of access transistors M5 and M6. When RWL (Read Word Line) gets high, the Read operation will be performed. For a Standby state both the RWL and WWL gets discharged by discarding M5, M6 and M7. To perform a write operation; WWL is stand to logic1. To write a logic0 to the cell, BL is stand to the logic0 and BL Bar is stand to logic1. Thus, the storage nodes Q stores logic, '0' and Q stores logic1. As Q gets a logic0, it will turn ON the transistor M3 and turn OFF the transistor M4. Similarly, as Q gets a logic1, it will turn ON the transistor M2 and turn OFF the transistor M1. Thus, the access transistor passes the stored logic values from the two-bit lines into the cell. To perform a Read operation, RWL (Read Word Line) is stand to logic1 and with use of sense amplifiers, the data is read properly. The design performs better regarding delay but consumes more power. To save the power, different power reduction techniques can be used.

III MTCMOS (Multi Threshold CMOS)

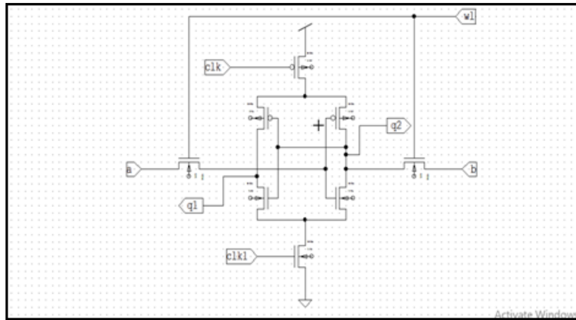
This technique uses transistors with multiple thresholds voltages to optimize a delay and a power. Low Vt transistors switch faster but have a higher static power leakage. On the other hand, High Vt transistors reduce a static power leakage but a switch slower. MTCMOS design techniques use carefully designed circuits to optimize the power and a delay without incurring penalties. The most common implementation of MTCMOS to reduce a leakage power uses sleep transistors. With the help of sleep transistors, virtual power rails are created which supply the logic. High Vt sleep transistors are used to connect the physical power rails to the virtual power rails. These transistors are turned on in an active mode and off in a sleep mode by the Clock signal. These sleep transistors help reduce static leakage power by a great amount when the SRAM cell is not in use. PMOS (High Vt) a transistor is used between the pull up a network and a vdd while a NMOS (High Vt) a transistor is used between the pull down a network, and a ground. Since critical path transistors are required to switch fast in an order to avoid incurring penalty in delay times, all the transistors in the SRAM cell are modeled as Low Vt. Only the sleep transistors are modeled as High Vt to reduce a leakage power. This configuration gives optimized a result regarding a power consumption and a write/a read delay.

SRAM Cell using MTCMOS

In power gating techniques, such as Gated VDD and MTCMOS, the formation of virtual power rails (virtual VDD and ground) is very important, and these are formed only when the sleep transistors are turned off. Due to the cross coupled inverters, data bits, '0' (ground) and '1' (VDD) are present on either side of the SRAM cell at all times. So, when the sleep transistors are turned off, VDD and ground get disconnected from the cell, and the data bits, '0' and '1' on either side of the SRAM cell create the virtual power rails by charging them via the pass transistors of the inverters. These virtual power rails will always have a lower potential than VDD and generally, virtual VDD will be just enough for data reinforcement in the cell and not enough to perform any operation. To perform an operation (read/write), we switch the sleep transistors on, thereby restoring the actual VDD and ground. The formation of virtual power rails as mentioned above, makes power gated circuits prone to data loss, and this can be risky for an SRAM cell. In

sleep mode, virtual VDD and virtual ground are responsible for data retention in the cell. However, as time progresses in sleep mode, the virtual VDD slowly discharges. This phenomenon thus only allows for a particular amount of time, in sleep mode, for which data in the SRAM cell can be retained after which it will be lost. To solve this problem, the sleep transistors can be turned on before this particular amount of time elapses. This then restores actual VDD and ground thereby preventing data loss in the cell. Therefore, the designer must take great care in setting the frequency of the Clock pulse that controls the sleep transistors. Alternatively, a smart power management unit can be designed which provides the Clock signal to the sleep transistors as and when required.

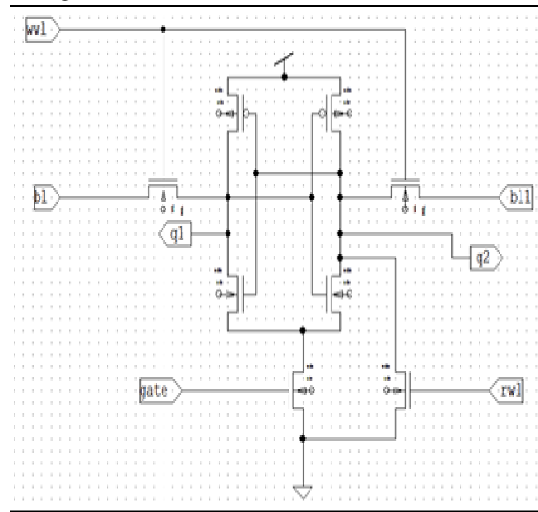
IV PROPOSED METHOD



The proposed Static RAM cell uses a potent power reduction technique called as Gated VDD. This technique uses an additional NMOS transistor connected to the ground path.

Gated VDD Methodology

The technique instigates a switching mechanism which disables Vdd, the supply voltage, when the Static RAM is not used by terminating the leakage current. Introducing such a transistor help in reducing the leakage power dissipated by a huge amount. To attain such a mechanism, a transistor of High threshold voltage, ―High Vt‖ should be used in the ground path enabling all the remaining transistors to Low threshold voltage, ―Low Vt.‖ Low Vt Transistors are utilized since they switch quicker than the High Vt Transistors. _Gated Vdd control‗signal is used to switch, _ON‗ or switch, _OFF‗ the Static RAM cell. Hence, the word‖ Gated‖ is mentioned to explain such a mechanism. Main benefit of using such a technique is to maintain the system performance though the transistors' threshold voltages and supply voltage are diminished.



Gated VDD Methodology

PERFORMANCE ANALYSIS

SRAM	AVERAGE POWER
Standard 7T	7.124
MTCMOS	4.482
GATED VDD	1.181

V CONCLUTION

Potent power reduction technique for different SRAM cells is designed named as a gated VDD in an 180nm technology. Two power reduction techniques for SRAM cells have been analyzed namely Gated a VDD and a MTCMOS based designs. The MTCMOS based SRAM cell uses the least power and is the fastest among the designs discussed in this paper. The MTCMOS based SRAM cell achieves 26.4% power savings when compared with the conventional 7T SRAM cell while the Gated VDD SRAM cell achieves 33% power savings when compared with the MTCMOS.

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