HDL Implementation of 8-Bit Signed Calculator on Seven Segment

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Abstract **- In whole, this design performs following arithmetic operations: 8-bit binary addition, subtraction, multiplication and division. All these operations are performed by combining different modules such as Adder, Subtractor, Multiplier and Divider using sub modules in which basic gates were used.**

This calculator performs required operation of positive as well as negative numbers. Digital Circuit of these combinational circuits were firstly designed on the Schematic Sheet on EDA (Electronic Design Automation) tool then Verilog codes of all those circuits were successfully written.

The result of simulation was attained with successful execution of Verilog Hardware Description Language (VHDL) which was performed using XILINX ISE Design Suite 14.7. Afterwards the Design is being Implemented on FPGA board, FPGA board accepts the input from user and gives output as led's off(0) and on(1) respective to the final output of calculator.

Index Terms **- Signed Calculator, Schematics, Verilog, FPGA, EDA Tool.**

1.INTRODUCTION

In today's world all the things are directly or indirectly connected to computer, whose building blocks are the strings of binary numbers (i.e. 0's and 1's). Some basic operations are Addition, Subtraction, etc. As we all are aware calculation is the base of everything and binary calculation is the basics of operations in computer, as the calculator is a device which is used to perform arithmetic operations, and this design is capable of doing so. This design accepts any binary sequence of 8 bit binary input data and performs required operation accordingly user and gives suitable output. User have to select that which operation he/she wants to perform and also have to select the polarity of bit's and afterwards this design will give suitable result.

This design will perform: -

Minimum of 00000000 (+/−/÷/×) 00000000 which will be executed in 8 binary digits.

Maximum of 11111111(+/−/÷/×) 11111111 which will successfully be executed in 9 binary digits.

Techniques such as Boolean logic gates basics, Boolean logic expressions, Binary calculations, Circuit Designing, Karnaugh maps and 2's complement are implemented in this design.

This design is simulated in XILINX ISE Tool, which allows Designing and synthesizing of HDL designs and examine the RTL Design.

This design is capable of simulated on the FPGA board through the EDA tool, FPGA are semiconductor devices which contains Programmable logic block they are used to simulate electronics circuits. This can be Programmed or reprogrammed in accordance to the conditions. 25 led's (16 led's for input and 9 led's for output) of FPGA board will display our final result using some of those led's. This board is connected via programmable interconnects which let the simulator tool decides that which led's is/are going to show the output.

2.BLOCK DIAGRAM OF CALCULATOR

The block diagram consist of:

1. Input
2. Reset
3. Mode Selection
4. Sign Selection
5. Mode Selection
6. Airthematic Operation
7. FPGA

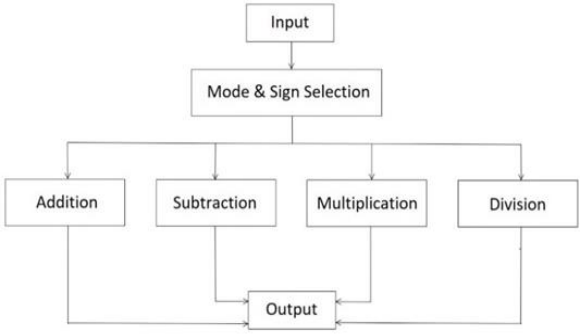


Fig.1 Block diagram of working of the calculator.
This block diagram shows the functioning of the calculator.

2.1.INPUT
In this section user gives 2 inputs A and B. Each inputs is of 8 bits along with several other inputs like inputs for sign selection which is of 1 bit (0 for positive and 1 for -ive) and inputs for mode selection which is of 2 bits (00 for summation, 01 for minus 10 for multiply and 11 for divide).

2.2. MODE SELECTION
Mode Select is the module used for the selecting the mode of the execution.
00:- Addition,
01:- Subtraction,
10:- Multiplication,
11:- Division.
This is achieved by transferring the output of the different modules to the input of decoder 2X4 which gives the output based on the operation selection by the user.
A 4X1 multiplexer can also be used in instead of a 2X4 decoder to achieve the same operations. But in that case the mode selection inputs will be connected to the select lines of the 4X1 multiplexer.

2.3.SIGN SELECTION
This block selects the sign of the input, 0 – positive, 1 – negative. Binary data is being converted into its 2's complement form for their negative representation. We have constructed a sign selection which is responsible for selection of sign (positive or negative) according to the corresponding input.
The Sign Selection module used here is of 8-bit which decides the input based on the input provided by the user. A logic '0' indicates the positive (+ve) sign and a logic '1' indicates negative (-ve) sign. This is done by the xor gate and the 2's complement converter based on the input. 0 to xor gate doesn't change the other input but 1 inverts the other input. This is how the sign selection is achieved.

2.4.RESET
This is a separate input which reset the circuits (when 1) and set every output to zero state. In case of any failures there is a reset pin which resets the output on applying 0 to it and the design works by itself if input is 1.

2.5. ADDITION, SUBTRACTION, MULTIPLICATION AND DIVISION
There are different operations that a calculator can have. Some of these may contain subtraction, addition multiplication, division, power, logarithmic calculations and many more. So add, subtract, multiply and divide are the four modules designed in this in order to perform their respective operation which has been selected by the user in the mode selection.

2.6.FPGA
FPGA are semiconductor devices which are made up of the table of the configurable logic blocks (CLBs) those are interlace together through the programmable interconnects. The FPGA contains an array of the programmable logic blocks, and the re-configurable interconnections that would allow all the blocks and logic gates to get them connected through wire altogether, to accomplish the complex combinational functions, or only some simple logic gates functions.. FPGAs are reprogrammable devices that can be reprogrammed to a suitable and needed application or functionality prerequisite after fabrication.
FPGAs are widely used in quick prototyping and verification of theoretical design and as well as useful in electronic systems. The primary use of the FPGA's is to avoid the high expenses for the custom VLSI projects such as ASIC for a small quantity.
The Nexys A7 is rebranded version of Nexys DDR4 board, which is the updated form of the Nexys 4 board With the its very large-capacity FPGA, general external memory, and collection of USB's, Ethernet, and many other ports, the board of Nexys_A7.

3.SEVEN SEGMENT DISPLAY

In our project we have focused to display the output of the 8-bit calculator on the seven-segment display for which our output values are changing. As our proposed project is generating outputs in binary format at the end so we require a seven-bit decoder to generate specific bit signals to generate the required output which is to be applied as an input to the seven-segment display. So, we have an output to display it we require four seven segments' LEDs to represent it. Here is the diagram of seven segment display given below as figure 3.A.

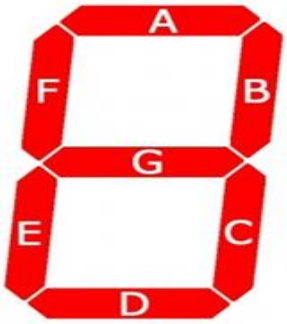


Figure 3.A

Here we can see seven segment denoted as A ,B ,C, D, E, F and G each segment is set of LED's and anode of these are set to be High always to make a particular segment active we have to make its cathode to be low. For example we want to display 3 number so we have to make cathode of the F and E to be HIGH and kept others at low voltage for displaying the number. We have denoted each segment cathode as CG, CF, CE, CD, CC, CB and CA in the table. The more detailed description is given in the below table :

No	CG	CF	CE	CD	CC	CB	CA	Cathode
0	H	L	L	L	L	L	L	7'b0000001
1	H	H	H	H	L	L	H	7'b1001111
2	L	H	L	L	H	L	L	7'b0010010
3	L	H	H	L	L	L	L	7'b0000110
4	L	L	H	H	L	L	H	7'b1001100
5	L	L	H	L	L	H	L	7'b0100100
6	L	L	L	L	L	H	L	7'b0100000
7	H	H	H	H	L	L	L	7'b0001111
8	L	L	L	L	L	L	L	7'b0000000
9	L	L	H	L	L	L	L	7'b0000100

Table 1 : I/O table of seven segment

4.RTL VIEW OF CALCULATOR

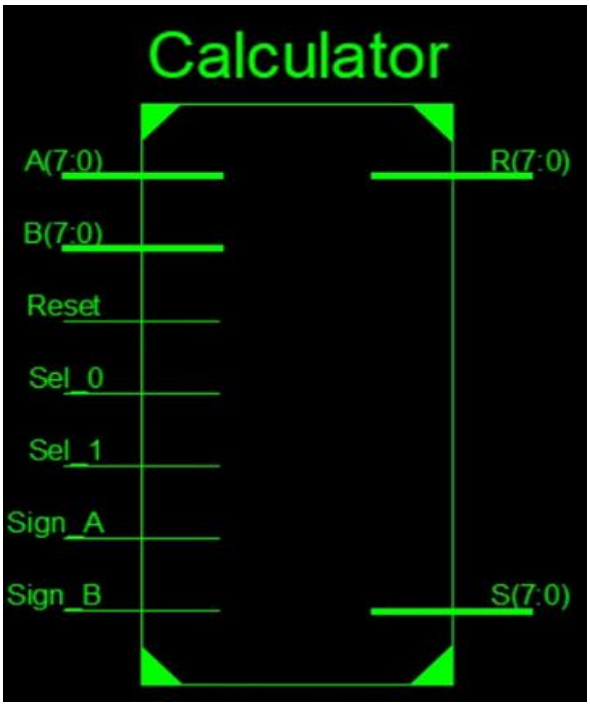
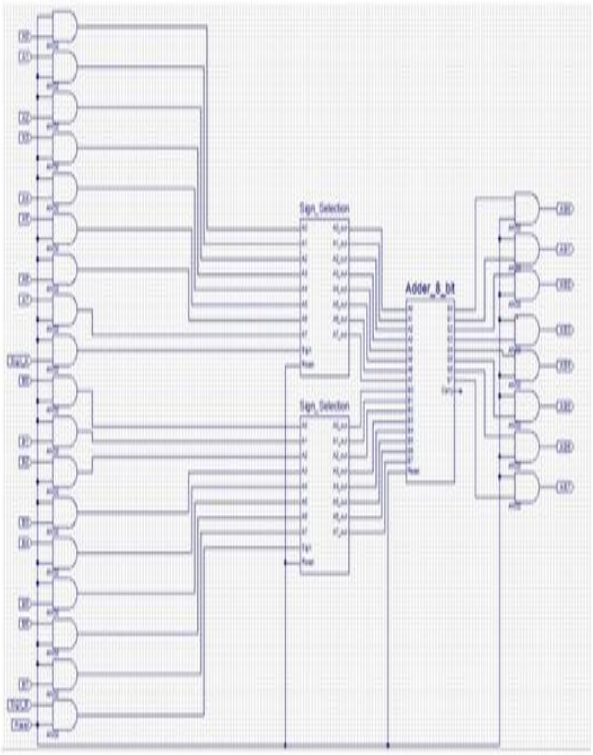


Figure 4.A

5.SCHEMATICS & SIMULATIONS



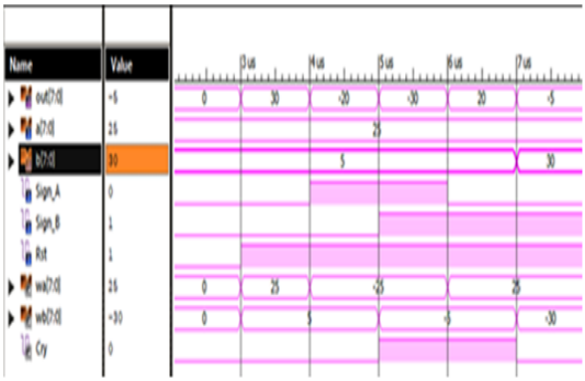


Fig. 5.A - 8 - Bit Adder

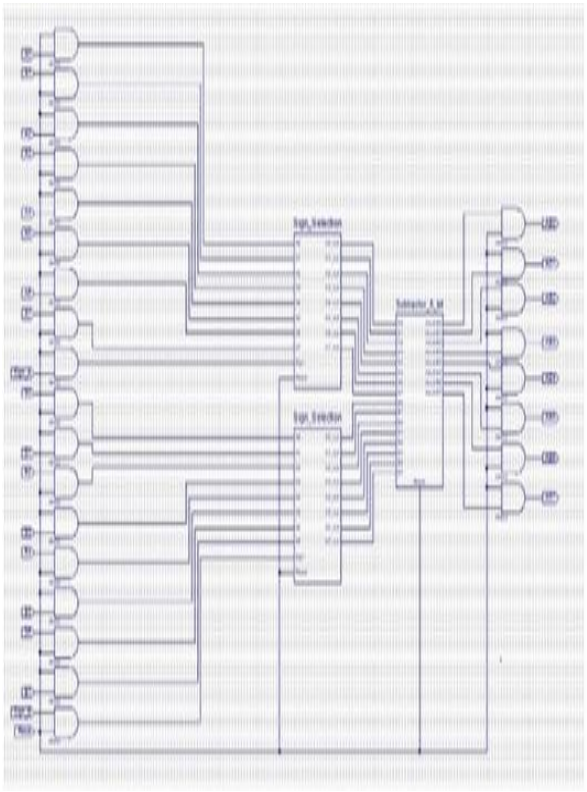
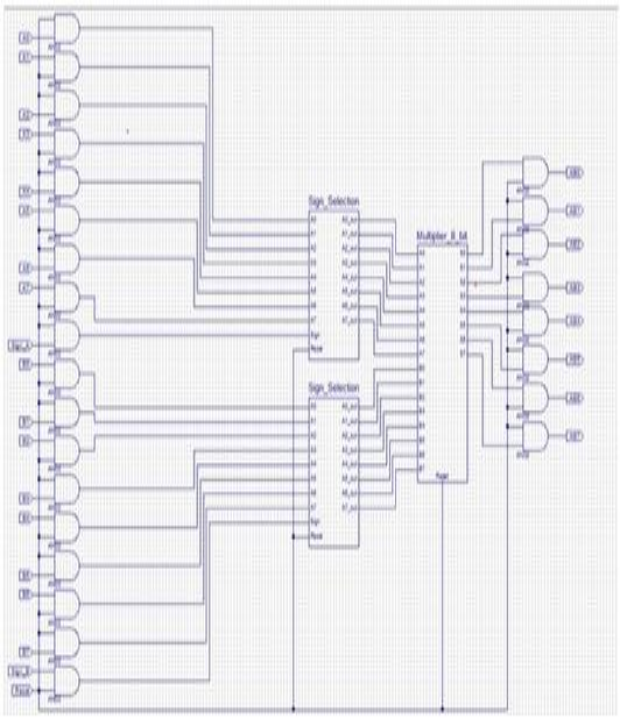


Fig. 5.B – 8-Bit Multiplier



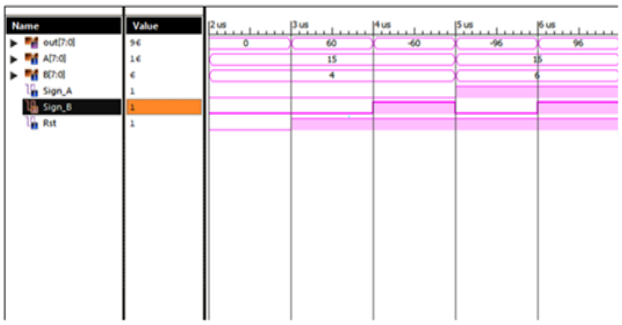
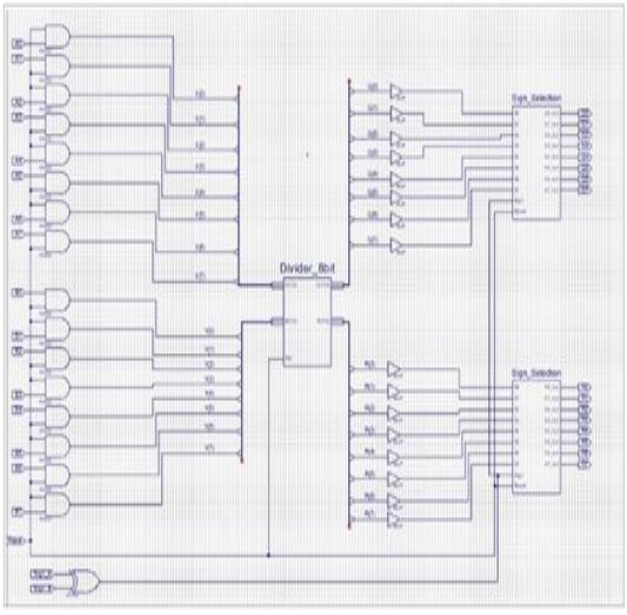


Fig. 5.B – 8-Bit Multiplier



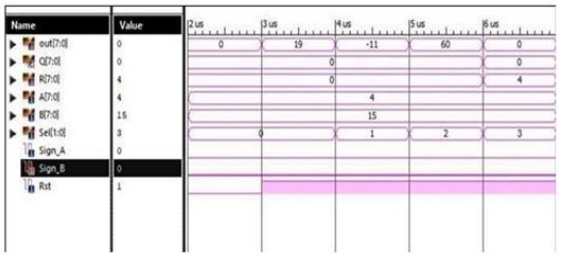


Fig. 5.B – 8-Bit Multiplier

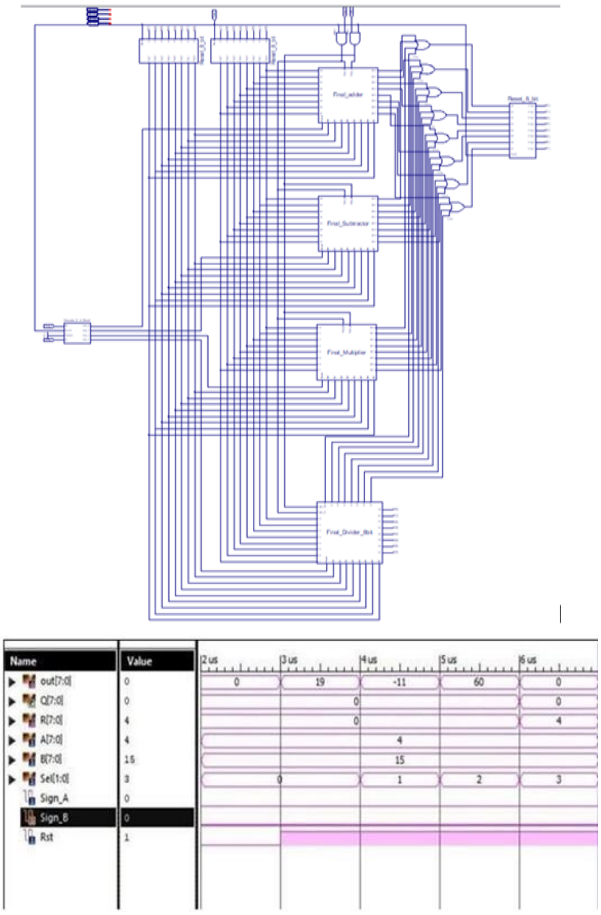


Fig. 5.B – 8-Bit Calculator

6.THEORY

6.1. 8-BIT ADDER

Here we have constructed an 8 bit signed adder circuit which is an top module which have many sub-blocks like 8-bit adder, full adder, half adder, etc. The Sign Selection module used here is of 8-bit which decides the input based on the input provided by the user.

6.2 8-BIT SUBTRACTOR

Subtractor used in this module is of 8-bit. It consists of inner sub-modules of full adder and half adder There are two inputs A and B and here B is subtrahend from A is minuend In case of any failures there is a reset pin which resets the output on applying 0 to it and the design works by itself if input is 1. Sign selection also works for negative numbers subtracting negative of B from A will add it to A.

6.3 8-BIT MULTIPLIER

Here we have constructed an 8-bit signed multiplier circuit which is an top module which have many sub-blocks like 8-bit multiplier, 8*1 multiplier, 8-bit adder, etc. A logic ‘0’ indicates the positive (+ve) sign and a logic ‘1’ indicates negative (-ve) sign. This is done by the xor gate and the 2’s complement converter based on the input. 0 to xor gate doesn’t change the other input but 1 inverts the other input. This is how the sign selection is achieved.

6.4 8-BIT DIVIDER

Here we have constructed an 8-bit signed divider circuit which is an top module which have many inner sub-blocks like 8-bit divider, comparator, 8-bit subtractor, etc. In thi module A is the dividend and B is the divisor.

6.5 8-BIT CALCULATOR

In this whole we conclude, this design can performs the following functions: arithmetic operations - 4-bit binary addition, subtraction, multiplication and division. These operations can be performed by combining many different modules like as Subtractor, Adder, Multiplier and Divider using their sub modules in which the basic gates were used.

7.CONCLUSION

Our binary calculator is successfully synthesized and simulated. The output we get is up to the mark as expected. FPGA board successfully accepts the input and Led’s of FPGA shows the output as expected. This might be further expandable by using FPGA implementation of this project on LCD (liquid-crystal display), VGA (Monitor), Hyper Terminal. This could have been done even by Arduino IDE or other micro controllers but that restricts our learning from getting farther from Digital Fundamentals. The purpose of this project is to utilize all these digital components to study and create our own 8-bit calculator.

At last we have connected our implements design to the hardware FPGA board through the JTAG connection. And then the implemented design can be seen on the hardware the switches can be turned on and off correspondingly representing logic '0' and logic '1' respectively.

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