CNFET-Based Ternary Logic Circuits

K. Chandrika[1], K. Mamatha[2]
[1]*Student Dept of ECE, Ananthapuram, AP*
[2]*Assistant Professor Adhoc, Dept of ECE, JNTUACEA, Ananthapuram, AP*

***Abstract*— In today's world, binary logic is implanted utilising CMOS. However, CMOS has a number of drawbacks, including high leakage power and short channel effects. CNFET is used to implement ternary logics to avoid these drawbacks. The main benefit of ternary logics is that they take up less space on the chip and need less memory. Half Adder circuit for ternary logic is proposed in this paper. To begin, a decoder is employed to convert ternary to binary signals. Following that, binary signals are processed using a binary Half Adder before being transformed to ternary using an Encoder. The disadvantage of utilising a basic encoder is that it has a low resistance route and so consumes a lot of power. To deal with this, different encoders are used, such as the basic encoder and the enhanced encoder. In order to save energy, Encoders with low power consumption are employed. To eliminate latency, high-speed encoders are used. Variables such as chirality, diameter, pitch, number of tubes, oxide thickness, and dielectric materials are used to perform a detailed analysis of the encoder's power consumption and delay. This optimised Encoder is used in conjunction with a Half Adder.**

***Index Terms:* CNFET, ternary logic, basic Encoder, enhanced, low power, high speed Encoder, Half Adder.**

I.INTRODUCTION

Multi-Valued Logic (MVL) circuits have received a lot of interest recently due to the benefits they provide in terms of lowering connection complexity and enhancing information content per unit area. Ternary Logic is a variant of MVL with three layers of logic. Voltage mode implementation Transistors with distinct threshold voltages are required in ternary logic circuits. Because body biassing is used to adjust the threshold voltage of classic Metal-Oxide-Semiconductor (MOS) transistors, designing ternary logic circuits with MOS transistors becomes complicated. Carbon Nanotube Field Effect Transistor (CNFET), on the other hand, is gaining popularity in the implementation of ternary logic circuits. This is due to the fact that carbon nanotubes (CNTs) are employed as a conduction channel in CNFETs, and changes in CNT diameter generate changes in CNFET threshold voltage. This kind of CNFET nature makes it suitable for MVL circuits and henceforth for ternary logic circuits as well.

Any of numerous multi-valued logic systems are referred to as ternary logic circuits. Because ternary increases the speed of computation and increases the complexity [3] there are three truth values logic0,1,2. It is created utilising CMOS by adding MVL to binary to lessen the complexity of the ternary logics. CNFETs are utilised to produce excellent performance with minimal power consumption. The required threshold can be obtained by altering the diameter. There are numerous CNFET-based Arithmetic circuit implementations (comparator, adder, and ALU)[3].

Scaling silicon MOSFETs gets more difficult as their size decreases. CNFETs can be used as a channel material if great performance is required. Strong covalent bonds in CNFETs result in a high driving current and a large conductance. As shown in [10], a CNFET-based approach eliminates the need for resistance by using p-type CNFETs as an active load. Ternary logic designs based on CMOS can be found in [2][3], but because CMOS-based designs have a high power consumption and propagation latency, CNFET-based ternary logics have been implemented[8]. To acquire the final ternary output, these ternary signals are first transformed to binary signals, then transmitted via binary gates and an encoder.

Encoder is a necessary component for converting binary to ternary signals. This paper examines the power consumption and delay of various encoder designs by altering various parameters. An appropriate encoder is utilised to implement the ternary half adder[18].

II. LITERATURE SURVEY

Regular ternary logic functions have been defined as a major and useful family of ternary functions, and their fundamental features have been addressed. We focused on their representations and canonical forms in particular. Three-valued majority functions have recently been introduced as a family of noteworthy ternary logic functions by Yamamoto [10]. The three-valued majority functions discussed in this study are a special case of normal ternary logic functions.[1]

The design of a new ternary circuit based on carbon nanotube field effect transistors was reported in this research (CNTFETs). A novel multi-diameter CNTFET-based ternary design has been presented for cost and performance effective ternary inverters, based on the fact that the threshold voltage of the CNTFET is a function of the CNTFET geometry (i.e. the chirality).When compared to prior CNTFET-based designs, the suggested ternary inverter design uses multidiameter (threshold voltage) CNTFETs, and the proposed ternary inverters achieve three times higher performance, low power, and small area due to the removal of resistors. All simulations were carried out in HSPICE with the CNTFET model from [9]. The proposed ternary inverters' power and delay improvements are practicable and viable, according to simulation results.[2]

The design of a new ternary logic family based on CNTFETs has been reported in this research. Because the CNTFET's threshold voltage is a function of its geometry (i.e. chirality), this research focuses on a novel multi diameter (multi threshold voltage) CNTFET-based ternary design. Using multi diameter CNTFETs, a complete set of ternary gates has been created. A few ternary arithmetic circuits, including as the HA and multiplier, have also been created to demonstrate the utility of the proposed ternary family for circuit construction. Because of the removal of resistors and the use of binary gates in the construction of arithmetic circuits, the suggested ternary gates provide excellent performance, low power, and a compact space as compared to previous CNTFET-based designs. All of the simulations were completed.[8]

This paper presented the design of a new a ternary circuit based on carbon nanotube field effect transistors (CNTFETs). Based on the fact that the threshold voltage of the CNTFET is function of the geometry of the CNTFET (i.e. the chirality), a novel multi-diameter CNTFET-based ternary design has been proposed for the cost and performance effective ternary inverters. The proposed ternary inverter design uses multi diameter (threshold voltage) CNTFETs, and the proposed ternary inverters achieve three times higher performance, low power, and small area due to the removal of resistors compared with previous CNTFET-based designs,. All simulations have been performed in HSPICE using the CNTFET model provided by [9]. Simulation results confirm that the power and delay improvement is practical and viable by the proposed ternary inverters.[9]

In CNTFET, new single-trit and multitrit adder architectures are presented. It's worth mentioning that the transistor-based design method (rather than gate-level design) used for the encoder and carry generation yields a cost-effective result. The proposed ideas result in a product with a low power delay. [12]

Several ternary arithmetic adder circuits were discussed, and their power consumption was measured. The usefulness of ternary logic is demonstrated using the proposed adder circuit, which shows significant reductions in power dissipation. As a result, the suggested innovative ternary full adder provides outstanding performance with very low power consumption. The simulations were carried out utilising the Synopsys HSPICE programme and the Stanford university CNTFET model files. The findings show that using a ternary logic design method in combination with binary logic implementations is a viable alternative for high-performance and low-power VLSI architectures. [13]

This research proposes a new ternary full adder cell (TFA) design based on CNTFETs. A resistive voltage divider is used as an integral part of the design and output buffer in the proposed TFA. In terms of delay and energy cost, the proposed structure outperforms existing TFA circuits. It also has a strong driving power and is durable. The notion of modulo-3 addition is also used to create a three-input ternary XOR circuit. This design also has a high level of energy efficiency. [15]

In this research, we describe low-complexity multi-digit adder designs based on unary operators of multi-valued logic in CNTFET technology. Low-delay and low-transistor-count designs of ternary

conditional sum and carry look ahead type adders have resulted from efficient CNTFET circuits for select unary operators. Furthermore, to reduce power consumption, the designs have been upgraded with diode linked CNTFETs. The designs were also tested for robustness as well as the influence of PVT changes. The work presented here, we feel, is a step toward the creation of tools for electronic design automation in many developing nanotechnologies. The proposed technique based on unary operators, in particular, is predicted to be useful for various device technologies (such as resonant tunnelling diodes [35], fins [36], [16]

Encoders are used to transform intermediate binary signals to final ternary outputs and are an important part of the design of ternary logic circuits. This study proposes better encoder designs for use in ternary logic implementation. circuits. Encoders are subjected to a thorough examination.to comprehend the impact of employing CNFETs with varying dimension CNTs on total propagation delay and power consumption. Optimization methods are developed based on this analysis.are offered, which select appropriate encoders for various applications. When optimising delay in the output stages of a ternary circuit Product with power or power-delay. Based on ternary ripple-carry The proposed encoder is an example of an adder. It is subjected to mapping algorithms. The ternary that results HSPICE is used to implement and compare adder designs. With alternative ternary adders in the literature in terms of many design characteristics .According to simulation results, ternary adder designs that use encoder mapping obtained from the proposed algorithms reduce power consumption by 54 to 82 percent 0-75 percent in propagation delay and 54–94 percent in consumption When compared to conventional ripple carry-based ternary adders, this device has a lower power delay [18].

III. REVIEW OF CNTFETS

Single walled CNTs are used as a conducting channel between source and drain in single walled CNFETs. Double walled CNTs are used as a conducting channel between source and drain in single walled CNFETs.CNFETs with desired chiralities(n,m) are manufactured[18].

The integer pair of the chirality vector is n, m. The zigzag model uses m=0 nanotubes, while the armchair model uses n=m nanotubes. The tensil strength is considerable in this zigzag pattern[3]. Depending on the folding angle and diameter, it can be metallic or semiconductor. When n=m or n-m=3i, it behaves like a metal; otherwise, it behaves like a semiconductor. In ternary logic, CNFETs with three chiralities are often utilised.[8]. The diameter and threshold voltage relationships can be deduced from the relationships described in[8]. In [3,] some of the most significant basic gates are discussed, as well as how they are implemented. The diameter of a carbon nanotube can be estimated using the equation below.

$$D_{CNT} = \frac{\sqrt{3}a}{\Pi}\sqrt{n^2+m^2+nm}$$

The interatomic distance of each carbon atom is a=0.142nm. The CNFET's I-V characteristics are similar to MOSFETs. The threshold voltage, which is the voltage required to turn on transistors, is also vital to consider while designing the circuit. From the relationship, the threshold voltage is inversely proportional to the diameter.

$$\frac{Vth1}{Vth2} = \frac{DCNT2}{DCNT1} = \frac{N2}{N1}$$

CNFETs offer a one-of-a-kind way to regulate threshold voltage by varying the chirality vector or CNT diameter. This method has been proposed for fabricating SWCNTs with the desired (n,m) chirality structure.

IV. SIMULATION METHODOLOGY

The Stanford CNFET model is used to implement CNFET-based ternary logic circuits. Hspice is used to implement and simulate these. Hspice's circuits all ran on a 0.9v power supply at room temperature. CNFETs with the same chirality but a default pitch of 20nm and a switching frequency of 500MHz. There are CNFET-based models in the literature [18]. Depending on the requirements, parameters such as oxide thickness and the number of carbon nanotubes can be mentioned. Based on the technology we want, several parameters should be added in. This project makes use of 32nm technology.

V. CNTFET-BASED TERNARY ENCODERS

Various encoders are built in this section to determine the best circuit for power consumption and

propagation delay optimization, and their circuit operation is explained below. And the truth table that corresponds to them is shown below.

Encoder:

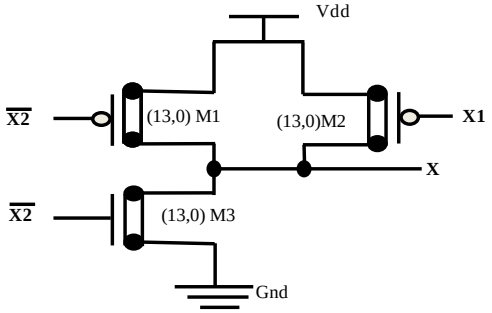


Figure 1.1 Encoder

The Encoder circuit is depicted in Figure 1.1. This path has a low resistance. A direct link from Vdd to Gnd is built using the inputs X1 and X2=0. At the output, logic1 is formed because to the low resistance route. The circuit draws a huge static current and consumes a lot of power as a result of this. Where M2 and M3 are in the ON state, and M1 and M3 are in the ON state for X1 and X2=2. In other circumstances, logic 2 or logic 0 is generated at the output by a direct connection to Vdd or Gnd.

Truth Table:

X1	X2	M1	M2	M3	X
0	0	ON	ON	OFF	2
0	2	OFF	ON	ON	1
2	0	ON	OFF	OFF	1
2	2	OFF	OFF	ON	0

Figure from[18]Enhanced Encoder, a low resistance path is created by using an additional diode between the P-CNFET and N-CNFET transistors, resulting in an enhanced encoder as shown in fig. 1.2. M1 and M5 transistors are both ON when the inputs x1=0 and x2=0. M2 and M4 transistors are also ON when the inputs x1=0 and x2=0. Because Vgs=Vds (Vds=Vd-Vs), the source voltage is greater than the drain voltage, M2 is in the ON state. When the drain voltage exceeds the source voltage, M4 is in the ON state. There is a direct path between Vdd and Gnd because M1, M2, M4, M5 are in the ON state, so the output is logic1. Another case for generating logic1 is when x1=2 and x2=2, and M3 and M6 transistors are ON, so there is a direct path between Vdd and Gnd. Transistors ON/OFF position at when logic 0 and logic 2 input is given below:

Figure [18] shows how to make a low-power encoder by varying the resistance path between Vdd and Gnd while producing logic 1 at the output. The power consumption varies depending on the amount of resistance in the circuit. Additional transistors are added in series between the P-CNFET and the N-CNFET in this circuit to produce a high resistance channel. If the resistance of the Vdd – Gnd route is increased, the encoder will be changed for power consumption. Despite the fact that the high resistance path between Vdd and Gnd reduces power consumption, it causes an increase in encoder propagation delay.

High speed Encoder:

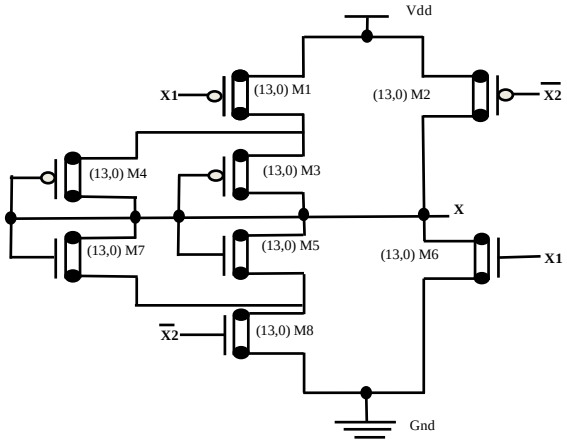


Figure 1.4. High speed Encoder

Figure 1.4 shows an encoder circuit that is optimized for propagation latency. To achieve low resistance in the Vdd and Gnd paths of the encoder, transistor pairs are linked in parallel. Although the latency will be minimized, the circuit's power consumption will increase. When the input is presented as logic 0 and logic 2 by truth table, the transistors ON/OFF position is described.

Truth Table:

X1	X2	M1	M2	M3	M4	M5	M6	M7	M8	X
0	0	ON	ON	ON	ON	ON	ON	OFF	OFF	2
0	2	ON	OFF	ON	ON	ON	ON	OFF	ON	1
2	0	OFF	ON	ON	ON	ON	ON	ON	OFF	1
2	2	OFF	OFF	ON	ON	ON	ON	ON	ON	0

VI.TERNARY HALF ADDER:

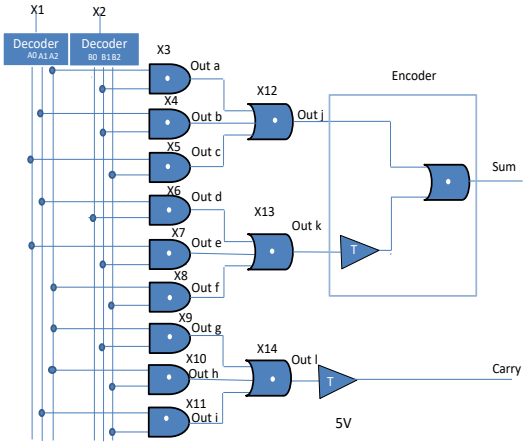


Fig 1.5 Schematic diagram of Ternary Half Adder

The signals are converted from ternary to binary or vice versa using ternary half adder, decoder, and encoder circuits. In this case, a ternary decoder is utilized to transform ternary signals to binary signals, which are subsequently fed into binary computations. The binary stage outputs are fed into the encoder, which converts binary to ternary signals. The encoder generates the sum and carry functions. The output equation from the Half Adder is[3] when using the karnaugh map.

Sum: $A_2B_0+A_1B_1+A_0B_2+1.(A_1B_0+A_0B_1+A_2B_2)$

Carry: $1.(A_2B_1+A_2B_2+A_1B_2)$

TERNARY DECODER:

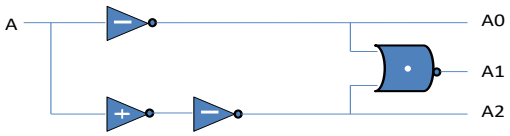


Fig1.6. Symbolic representation of Ternary Decoder

PTI, two NTI inverters, and a NOR gate make up the ternary decoder. The decoder has one input and three outputs, producing unary functions with three logic values of 0, 1, and 2.Only two logic values, logic2 and logic0,can be used in these decoder outputs, which correspond to binary logic0 and logic1.

Truth Table for Ternary Half Adder:

Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

VII. RESULTS AND DISCUSSION

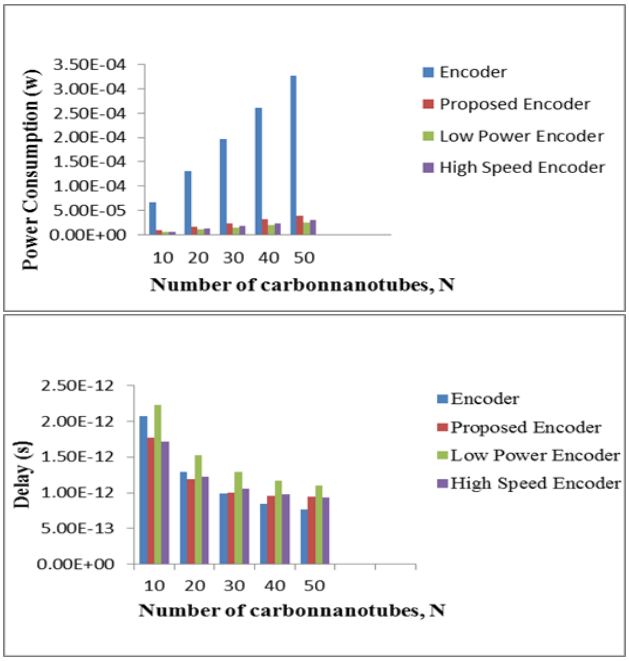


Fig.1 Different nanotube-based encoders' delay and power consumption

TABLE 1(a). For different encoders, power consumption increases as the number of tubes increases.

Tubes	Power Consumption (µW)			
	Encoder	Enhanced encoder	Low Power	High Speed
10	15.2	8.51	5.70	6.67
20	29.6	16.0	10.3	12.3
30	43.9	23.3	15.1	18.0
40	58.3	31.0	19.7	23.7
50	72.6	38.0	24.6	29.4

TABLE 1(b) Delay for different encoders based on the number of tubes

Tubes	Delay (ps)			
	Encoder	Enhanced encoder	Low Power	High Speed
10	28.2	1.77	2.23	1.72
20	17.9	1.19	1.53	1.22
30	12.2	1.00	1.29	1.06
40	10.4	0.96	1.17	0.98
50	9.68	0.94	1.10	0.92

As the number of nanotubes in a CNTFET rises, the transistor produces more current, which lowers resistances and increases power consumption.

$$I_{CNFET} = \frac{N g_{CNT}(v_{dd} - v_{th})}{1 + g_{CNT} L_s \rho_s}$$

Rapidly charging capacitances and higher current levels minimise the propagation delay time.

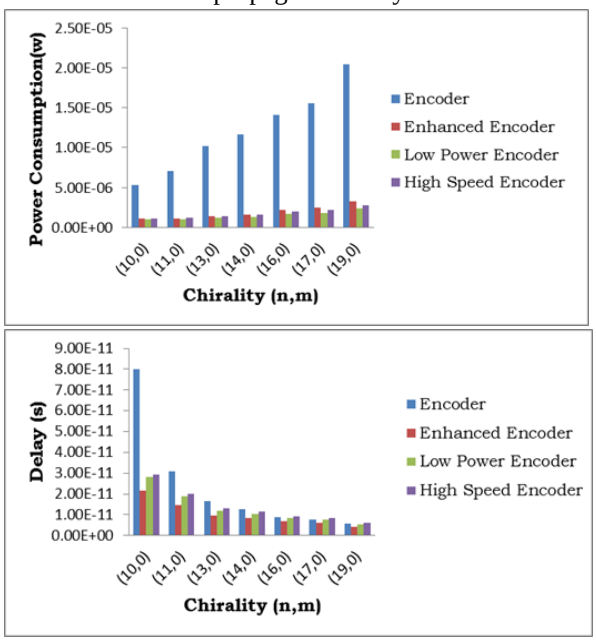


Fig.2 Different encoders' delay and power usage based on chirality (n, m)

TABLE 2(a) The power consumption of different encoders varies depending on their chirality.

Chirality (n,m)	Power Consumption(µW)			
	Encoder	Enhanced encoder	Low power	High Speed
(10,0)	5.25	1.08	1.02	1.14
(11,0)	7.09	1.11	1.03	1.16
(13,0)	10.2	1.39	1.18	1.39
(14,0)	11.6	1.62	1.33	1.57
(16,0)	14.1	2.15	1.65	1.95
(17,0)	15.5	2.64	1.80	2.17
(19,0)	20.4	3.26	2.39	2.77

TABLE 2(b) Delay caused by different encoders' chirality

Chirality (n,m)	Delay (ps)			
	Encoder	Enhanced encoder	Low Power	High Speed
(10,0)	80.0	21.7	28.2	18.8
(11,0)	30.8	14.5	18.7	12.8
(13,0)	16.5	9.50	11.9	8.55
(14,0)	12.8	8.30	10.4	7.60
(16,0)	8.94	6.79	8.54	6.18
(17,0)	7.84	6.09	7.60	5.50
(19,0)	5.80	4.38	5.50	4.03

The chirality, which is represented by an ordered pair of numbers, is a vector (n, m). This vector is used to determine whether or not something is metallic or semiconductor. The diameter of CNTs grows as chirality increases. The area of the cross section grows as the diameter increases, and the capacitance increases as a result. The power consumption of the various encoders grows as the capacitance increases, as seen in the equation below. $P_{con}=cv^2f$

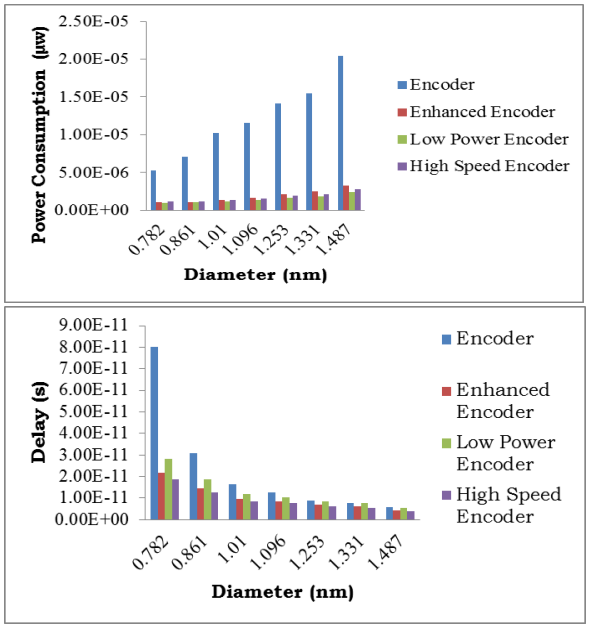


Fig.3 Different encoders' delay and power usage as a function of diameter

TABLE 3(a) The power consumption of different encoders varies depending on their chirality.

Diameter (nm)	Power Consumption (µW)			
	Encoder	Enhanced encoder	Low Power	High Speed
0.782	5.25	1.08	1.02	1.14
0.861	7.09	1.11	1.03	1.16
1.010	10.2	1.39	1.18	1.39
1.096	11.6	1.62	1.33	1.57
1.253	14.1	2.16	1.65	1.95
1.331	15.5	2.46	1.80	2.17

TABLE 3(b) Delay caused by different encoders' chirality

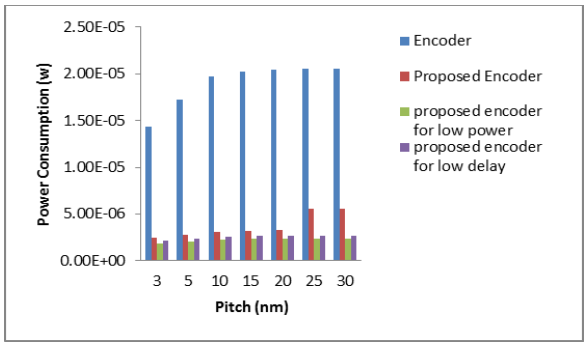
Diameter (nm)	Delay (ps)			
	Encoder	Enhanced encoder	Low Power	High Speed
0.782	80.0	21.7	28.2	29.5
0.861	30.8	14.5	18.7	20.0

1.010	16.5	9.50	11.9	13.0
1.096	12.8	8.30	10.4	11.4
1.253	8.94	6.79	8.54	9.30
1.331	7.84	6.09	7.60	8.33
1.487	5.80	4.38	5.50	6.13

As the diameter of the CNTs grows, the band gap between them narrows, increasing the on-current. As the diameter of the nanotubes grows, so does the trans conductance.

$$V_{th} = \frac{av_{\Pi}}{\sqrt{3}eD_{CNT}}$$

According to the above relationship between diameter and threshold voltage, the threshold voltage drops as the diameter rises, and as the threshold voltage decreases, the power consumption of various encoders increases. Despite the fact that the switching speed of FETs improves, the device achieves saturation faster than MOSFETs.



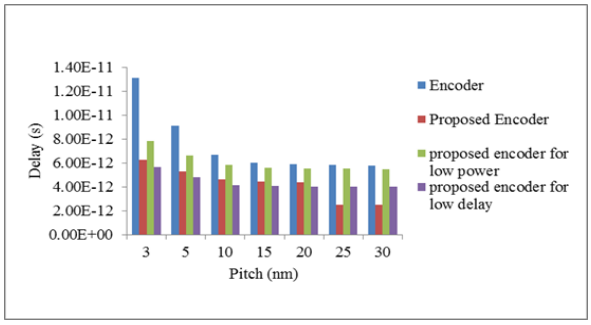


Fig.6 Different encoders' delay and power usage as a function of pitch

TABLE 6(a). For various encoders, the effect of increasing pitch on power usage.

Pitch (nm)	Power Consumption (µW)			
	Encoder	Enhanced encoder	Low Power	High Speed
3	14.4	2.45	1.83	2.12
5	17.2	2.78	2.04	2.35
10	19.7	3.13	2.29	2.59
15	20.2	3.22	2.38	2.65
20	20.4	3.26	2.39	2.68
25	20.5	5.56	2.40	2.69
30	20.6	5.58	2.41	2.70

TABLE 6(b) Delay as a function of pitch for various encoders.

Pitch (nm)	Delay (ps)			
	Encoder	Enhanced Encoder	Low Power Encoder	High Speed
3	13.1	6.24	7.85	5.65
5	9.10	5.27	6.64	4.78
10	6.65	4.62	5.82	4.15
15	6.01	4.44	5.60	4.07
20	5.86	4.38	5.54	4.03
25	5.81	2.51	5.51	4.01
30	5.78	2.50	5.49	4.01

Pitch refers to the distance between nanotubes and controls the amount of screening effect. The gate-to-channel capacitance and the consequent current produced by nanotubes can be increased by increasing the intertube gap. As a result of the decrease in the screening effect, the breadth of the channel narrows. Placing the nanotubes far apart results in the shortest delay.

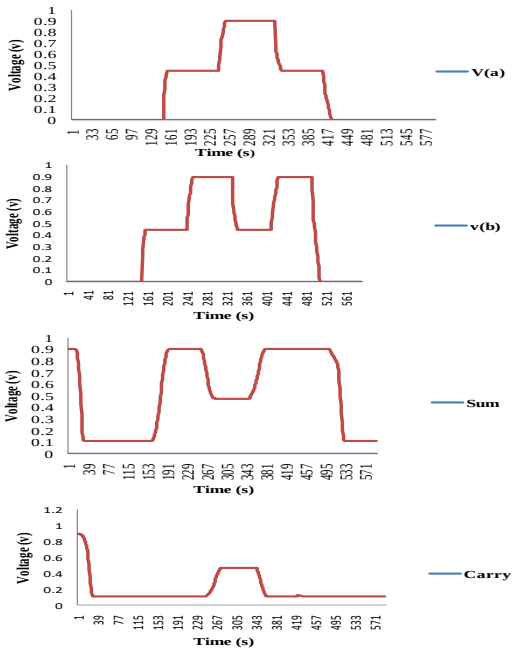
The following table shows a comparison between CMOS and CNFETs for various encoders.

From the table above, it is clear that CNFETs outperform CMOS.

Encoder types	CMOS		CNTFET	
	Avg Power(µw)	Delay(ps)	Avg Power (µw)	Delay(ps)
Modified Encoder	2.33E-05	6.64E-12	1.03E-05	1.81E-12
Proposed Encoder	3.12E-05	1.43E-12	9.74E-06	7.18E-13
Proposed encoder for low power	6.24E-05	2.12E-12	9.70E-06	9.06E-13
Proposed encoder for low delay	3.61E-05	8.60E-13	1.62E-05	7.24E-13

TERNARY HALF ADDER OUTPUT WAVEFORMS:

The Ternary Half Adder has two inputs v(a) and v(b) with ternary logic levels logic0,logic1,logic2, and sum and carry outputs with x-axis Time (s) and y-axis Voltage (V) (v). Logic0 has a voltage of 0V, logic2 has a voltage of 0.9V, and logic1 has a voltage of 0.45V.



CNFET INVERTERS OUTPUT WAVEFORMS:

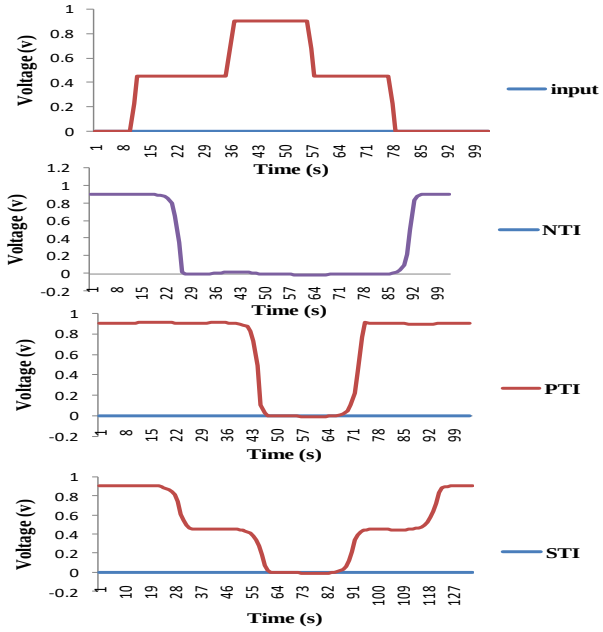


Fig output Waveforms of CNTFET Inverter

VIII.CONCLUSION

An encoder is a common component in the design of ternary logic circuits**. So,** in this study, many encoders are presented, and a complete examination of the above-mentioned encoder is performed by modifying parameters like chirality, diameter, pitch, oxide thickness, and dielectric material. An optimised encoder with 1.5nm diameter, zirconium dioxide as a dielectric constant, 4nm oxide thickness, and 20nm internanotube spacing with 10 number of CNTs is employed based on power consumption and delay study, resulting in decreased power consumption and delay for enhanced encoder. The core circuit is a Ternary Half Adder, to which various encoders are added. In this Half Adder, an improved Enhanced encoder is used to design and implement the Half Adder, and H-spice simulation is used to analyse it.

REFERENCE

[1] M. Mukaidono, "Regular ternary logic functions ternary logic functions suitable for treating ambiguity", *IEEE Trans. Comput.*, vol. C-35, no. 2, pp. 179-183, Feb. 1986.

[2] S. Lin, Y. B. Kim, F. Lombardi, "A novel CNTFET-based ternary logic gate design", *Proc. 2009 52nd IEEE Int. Midwest Symp. Circuits Syst.*, pp. 435-438, Aug. 2009.

[3] S. Lin, Y. B. Kim, F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits", *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 217-225, Mar. 2011.

[4] S. L. Murotiya, A. Gupta, "Design of high speed ternary full adder and three-input XOR circuits using CNTFETs", *Proc. 2015 28th Int. Conf. VLSI Des.*, pp. 292-297, 2015.

[5] Y. Ohno, S. Kishimoto, T. Mizutani, T. Okazaki, H. Shinohara, "Chirality assignment of individual single-walled carbon nanotubes in carbon nanotube field-effect transistors by micro-photocurrent spectroscopy", *Appl. Phys. Lett.*, vol. 84, no. 8, pp. 1368-1370, 2004.

[6] B. Wang, C. H. P. Poa, L. Wei, L.-J. Li, Y. Yang, Y. Chen, "(n m) selectivity of single-walled carbon nanotubes by different carbon precursors on Co-Mo catalysts", *J. Amer. Chem. Soc.*, vol. 129, no. 29, pp. 9014-9019, 2007.

[7] An Efficient Design Methodology for CNFET Based Ternary Logic CircuitsP. Sai Phaneendra, chetan vudadha, M. B. Srinivas.

[8] Sheng Lin, Yong-Bin Kim, F. Lombardi, "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits", *IEEE Transactions on*

Nanotechnology, vol. 10, no. 2, pp. 217-225, March 2011.

[9] P.V. Saidutt, V. Srinivas, P.S. Phaneendra, N.M. Muthukrishnan, "Design of encoder for ternary logic circuits", *Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia) 2012*, pp. 85-88, 5-7 Dec. 2012.

[10] Optimization of CNFET Parameters for High Performance Digital Circuits Shimaa Ibrahim Sayed, Mostafa Mamdouh Abutaleb, and Zaki Bassuoni Nossair. Electronics, Communication, Helwan University, Helwan, Egypt, Received 11 March 2016; Accepted 14 July 2016 Advances is in Materials Science and Engineering Volume 2016, Article ID 6303725.

[11] P. C. Balla, A. Antoniou, "Low power dissipation MOS ternary logic family", *IEEE J. Solid-State Circuits*, vol. 19, no. 5, pp. 739-749, Oct. 1984.

[12] J. Liang, L. Chen, J. Han, F. Lombardi, "Design and evaluation of multiple valued logic gates using pseudo N-Type carbon nanotube FETs", *IEEE Trans. Nanotechnol.*, vol. 13, no. 4, pp. 695-708, Jul. 2014.

[13] S. A. Ebrahimi, P. Keshavarzian, S. Sorouri, M. Shahsavari, "Low power CNTFET- based ternary full adder cell for nanoelectronics", *Int. J. Soft Comput. Eng.*, vol. 2, no. 2, pp. 291-295, 2012.

[14] P. Keshavarzian, R. Sarikhani, "A novel CNTFET-based ternary full adder", *Circuits Syst. Signal Process.*, vol. 33, no. 3, pp. 665-679, 2014.

[15] Cho, G., Kim, Y., Lombardi, F.: 'Performance evaluation of CNFET based logic gates'. Proc. IEEE Int. Instrumentation and Measurement Technology Conf., Singapore, May 2009, pp. 909-912.

[16] chetan Vudadha ; Sowmya Karaganda ; P Sai Phaneendra," 2:1 Multiplexer based design for ternary logic circuits" Date of Conference: 19-21 Dec. 2013 DateAdded to IEEE *Xplore*: 06 February 2014 INSPEC Accession Number: 14079984

[17] Chetan vudadha, srinivasan Rajagopalan, Aditya Dusi, p.Sai Phaneendra, M.B.Srinivas,"Encoder Based Optimization of CNFET Based Ternary Logic Circuits. Published in: IEEE Transactions on Nanotechnology (Volume:17, Issue: 2, March 2018) Date of Publication: 31 January 2018.

[18] ‘Encoder-Based Optimization of CNFET-Based Ternary Logic Circuits’, Chetan vudadha, srinivasan Rajagopalan, Aditya Dusi, p.Sai Phaneendhara , M.B.Srinivas.