Comparative Analysis of NAND Gate and D Flip-Flop in Terms of Delay and Power

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***Abstract*— The NAND gate is the highest priority gate in VLSI industry and D Flip-Flop is the basic element in shift register. The NAND gate and D Flip-Flop are implemented in different technologies like CMOS (180nm, 90nm, 45nm) technology and FINFET (18nm) technology. This work compares NAND gate as well as D Flip-Flop in various technologies in terms of delay and power. The Cadence tool is the leader of VLSI industry. This Cadence tool is used to implement the NAND gate and D flip flop. The simulation results were performed through Cadence Virtuoso environment at temperature 27 °C.**

Index Terms: **NAND, D Flip flop, CMOS, VLSI.**

I.INTRODUCTION

Flip-flops or the data storage elements are almost essential components are just about a fundamental part of each consecutive hardware. Among different flipflops, D flip-flop is generally utilized. It catches the worth of the D contribution at a specific predefined piece of the clock beat (rising or falling edge of the clock) and its result isn't impacted at different pieces of the clock. According to the timing point of view, defer created by goes back and forth consumes an enormous piece of the process duration while the working recurrence increases [8]. There are various methods for limiting the proliferation postpone in view of circuit level [10], architecture [4], format, and cycle technology [5]. Here flip-flop with a smaller number of transistors [3] for low proliferation delay [7] is planned. In this technique we utilized a smaller number of semiconductors consequently it requires less area [11] and along these lines consumes lesser power when contrasted with regular flip flops having more semiconductors. Various D flip-flop geographies [6] are accessible in the writing. In this manner, it turns out to be truly challenging for a circuit fashioner to pick fitting one for his plan from all those accessible geographies to meet the given prerequisite. In the current situation there is a steadily expanding interest for fast [8] and robust [2] gadgets. Thus, fitting choice of components at the exceptionally fundamental level, i.e., goes back and forth is vital to get the ideal attributes to help the greater framework.

In different ways, CMOS rationales are utilized to carry out the NAND entryway and the D flip-flop. The thickness of semiconductors on a solitary wafer chip has expanded as innovation propels, as has the recurrence of activity. Subsequently, the power utilization of battery-worked gadgets increments. The spillage current in these SoCs has expanded as the thickness has expanded.

The main test is to diminish power use while speeding up. The FinFET has been proposed as an option in contrast to constant scaling gadgets in request to resolve these issues. Along these lines, notwithstanding CMOS rationales, FINFET rationales have been utilized to carry out the NAND entryway as well as D flip-flop in different advances.

The NAND gateway and D flip-flop are planned utilizing the Virtuoso Schematic Editor's particulars. The utilitarian way of behaving of the circuits should be confirmed after they have been planned utilizing the Virtuoso Schematic Editor. The Specter with Cadence device is utilized to reproduce these plans. Following the execution of the NAND gateway and D flip-flop, the estimation of postponement and normal, greatest, and least power is performed.

II.LITERATURE SURVEY

NAND GATE USING FINFET FOR NANO TECHNOLOGY by Vijaya Kumar, Sam Jabaraj, Nirmal FinFET logics had been proposed with double gate transistors (FinFETs) and various logic circuits to attain leakage power savings.

DESIGN AND IMPLEMENTATION OF UNIVERSAL GATE USING DGFinFET 32NM TECHNOLOGY by Seema Mehta, Aastha, Devesh.

The universal gates were designed to implement the short gate [SG] FinFET device, and the circuit's transient behaviour and power consumption were examined.

PERFORMANCE ANALYSIS: D-LATCH MODULES DESIGNED USING 18NM FINFET TECHNOLOGY by V.RajeevRatna, G. Yamini, S. Sanath , T. Vinitha

Various methods to design the D-Latch using 18nm FinFET technology that reduces energy consumption than existing latches were proposed.

DESIGN & IMPLEMENTATION OF SEQUENTIAL CIRCUIT BASED ON LOW POWER USING 45NM TECHNOLOGY by S.Mohamedsulaiman, B.Jaison, M.Anto Bennet, Yacooprahman.S, Shanmugapriyan.V, Albert Santhosh Raj .J, V.Sathishkumar

Based on power gating Frequency dividers are made with low-power transistors to reduce size and only six Pmos to reduce delay, and they outperform traditional frequency dividers.

LOW-POWER DESIGN OF SEQUENTIAL CIRCUITS USING A QUASISYNCHRONOUS DERIVED CLOCK by Xunwei Wu, Jian Wei, MassoudPedram, Qing Wu

In sequential circuits, power dissipation is decreased by producing a quasi-synchronous derived clock from the master clock and utilising it to separate the circuit's flip flops from the master clock's undesirable triggering action.

POWER EFFICIENT CLOCK PULSED D FLIP FLOP USING TRANSMISSION GATE by S.B.Prakalya, Dr.T.Kumanan, Dr.V.Prabhu

Designers used Current Mode Clock Distribution Networks (CM-CDN) instead of Voltage Mode Clock Distribution Networks (VM-CDN) and Transmission Gate instead of Static CMOS Logic to reduce power consumption in D Flip-Flop.

DESIGN OF LOW POWER VLSI CIRCUITS USING TWO PHASE ADIABATIC DYNAMIC LOGIC (2PADL) by P. Sasipriya and V. S. Kanchana Bhaaskaran

Two phase adiabatic dynamic logic (2PADL) is a low-power quasi-adiabatic logic that uses charge recovery technology and is run by a two-phase sinusoidal clock signal.

PERFORMANCE ANALYSIS: D-LATCH MODULES DESIGNED USING 18NM FINFET TECHNOLOGY by Rajeev RatnaVallabhuni, G. Yamini, T. Vinitha, S. Sanath Reddy In the cadence virtuoso tool, D-Latches are created using 18nm FinFET technology.

When compared to typical D-Latch designs, the suggested FinFET latches consume less power and have a lower power delay product.

DESIGN OF LOW POWER VLSI CIRCUITS USING TWO PHASE ADIABATIC DYNAMIC LOGIC (2PADL) by Sasipriya P, V S Kanchana Bhaaskaran.

The quasi-adiabatic logic called two phase adiabatic dynamic logic (2PADL) for low power operated by two phase sinusoidal clock signal that uses charge recovery technique is designed.

IDENTIFICATION OF EMI INDUCED CHANGES DURING THE DESIGN OF ICS USING A POST-PROCESSING FRAMEWORK by Dominik Zupan; Bernd Deutschmann

A post-processing framework is applied during the design phase of integrated circuits which helps to identify the electromagnetic interference issues.

III.PROPOSEDMETHODOLOGYMOSTECHNOLOGY

The MOS Technology is utilized to assemble most of memory and microchip circuits in the Large-Scale Integration (LSI) and Very Large-Scale Integration (VLSI) sizes. MOS innovation, which enjoys a huge upper hand over bipolar intersection semiconductor circuits, considers significant semiconductor and circuit functionalities to be accomplished on a solitary chip.

The MOSFET has two modes of operation. Enhancement and Deflection modes are available for both p-channel and n-channel MOSFETs. When there is no voltage on the gate, the channel exhibits its maximum conductance in the depletion state.

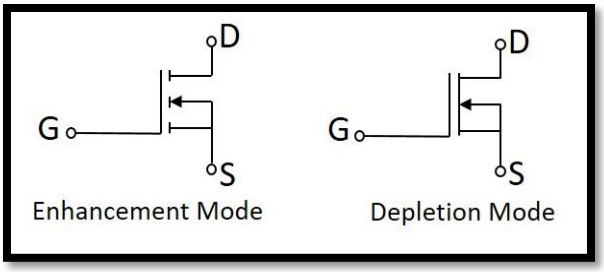

Fig 3.1: Symbols of N-Channel MOSFET

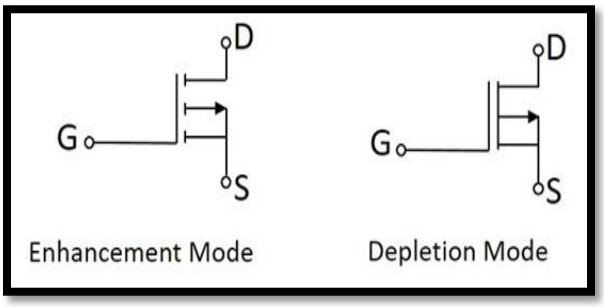

Fig 3.2: Symbols of P-Channel MOSFET

CMOS TECHNOLOGY

Complementary Metal Oxide Semiconductor (CMOS) innovation is one of the most notable MOSFET advancements accessible today. The diminished power scattering of CMOS over BIPOLAR and NMOS innovations is a huge benefit. Static power scattering is almost non-existent in a Complementary Metal Oxide Semiconductor circuit. Just when the circuit switches in all actuality do power become disseminated.

The Source and Drain of a P-channel MOSFET are diffused on an N-type substrate. Carriers who make up the majority of the population are holes. The PMOS will not conduct when a high voltage is supplied to the gate. The PMOS will conduct when a low voltage is applied to the gate. PMOS devices are more noise-resistant than NMOS devices.

NMOS is constructed on a p-type substrate with a diffused n-type source and drain. Electrons make up the majority of the carriers in NMOS. The NMOS will conduct when a high voltage is supplied to the gate. NMOS will also not conduct when a low voltage is given to the gate. Because the carriers in NMOS, which are electrons, travel twice as fast as the holes, they are regarded to be faster than PMOS.

CMOS logic gates have a group of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail in place of the load resistor seen in NMOS logic gates (often named Vdd). Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure below.

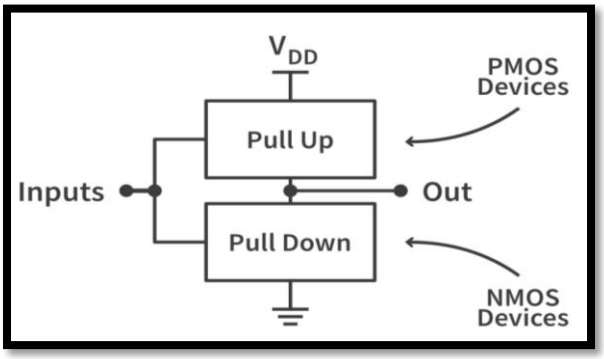

Fig 3.5: CMOS Logic Gate using Pull-Up and Pull-DownNetworks

FINFET TECHNOLOGY

A FinFET is a multi-gate Metal Oxide Semiconductor Field Effect Transistor (MOSFET). A multi-gate transistor is a device that integrates many gates into one. The conductor channel is encased in a thin silicon layer that serves as the body. The FinFET receives its name from the fact that when viewed from above, the structure resembles a sequence of fins. The channel length of the gadget determines its thickness. The distance between the sources and drain junctions determines the channel length of a MOSFET.

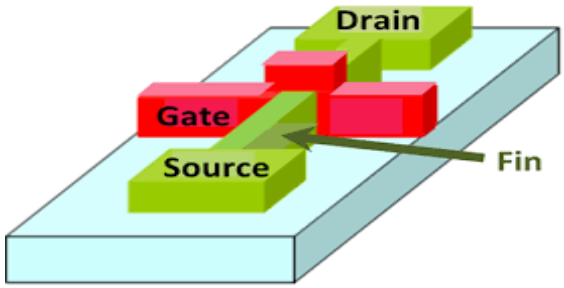

Fig 3.6: Structure of FINFET

The operation of a FinFet is identical to that of a conventional MOSFET. There are two modes of functioning for the MOSFET. Both n-channel and p-channel MOSFETs have enhancement and depletion modes. When there is no voltage on the gate terminal, the channel exhibits the highest conductivity. The conductivity of the channel diminishes when the voltage changes from positive to negative.

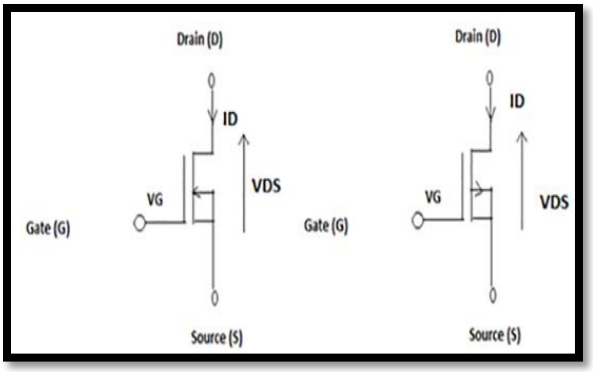

Fig 3.7: N-Channel FINFET, P-Channel FINFET

The channel in a FinFET is elevated, allowing conduction to proceed. As a result, the width (W) of the FinFET is determined by the channel height (Hfin). This results in a unique FinFET feature known as width quantization. This characteristic specifies that the FinFET width must be a multiple of Hfin, implying that widths can be increased by using different fins. As a result, self-assured FinFET widths are impossible. Smaller fin heights, on the other hand, provide more flexibility.

Shorted-Gate (SG) and Independent- Gate (IG) FinFETs are the two most normal assortments (IG). SG FinFETs are otherwise called three-electrode (3T) FinFETs, though IG FinFETs are known as four-electrode (4T) FinFETs. Both the front and back entryways are truly more limited in SG FinFETs, however the gates in IG FinFETs are actually secluded.

In SG FinFETs, the two gates are utilized to control the electrostatics of the direct along these lines. Accordingly, when contrasted with IG FinFETs, SG FinFETs seem to have higher on-current (Ion) and off-current (Ioff or underneath limit current). IG FinFETs permit you to apply various signs to their two entryways utilizing various voltages then again.

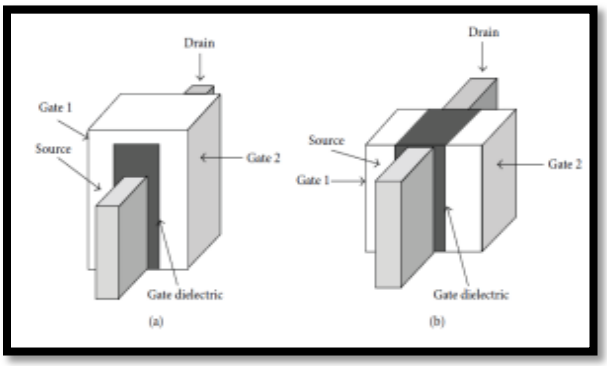

Fig 3.8: Structural comparison between (a) SG and (b) IGFINFET

This allows the back-gate propensity to be used to control the Vth of the front gate in a straight line. In any event, because to the requirement for two independent gate contacts, IG FinFETs result in a high zone punishment. Silicon-on-Insulator (SOI) FinFETs and Bulk FinFETs are the two most notable FinFET fabrication advancements. On top of the protective layer, the primary FinFETs were built. The spillage current is reduced because current cannot flow "underneath" the gate when the transistor is turned off. Later, elective solutions for avoiding spilled current from streaming in the bulk were presented, which included Bulk FinFET assembly.

IV.IMPLEMENTATION AND WORKING

The implementation and working of the process is given below in the form of a flow chart with several steps simultaneously as follows.

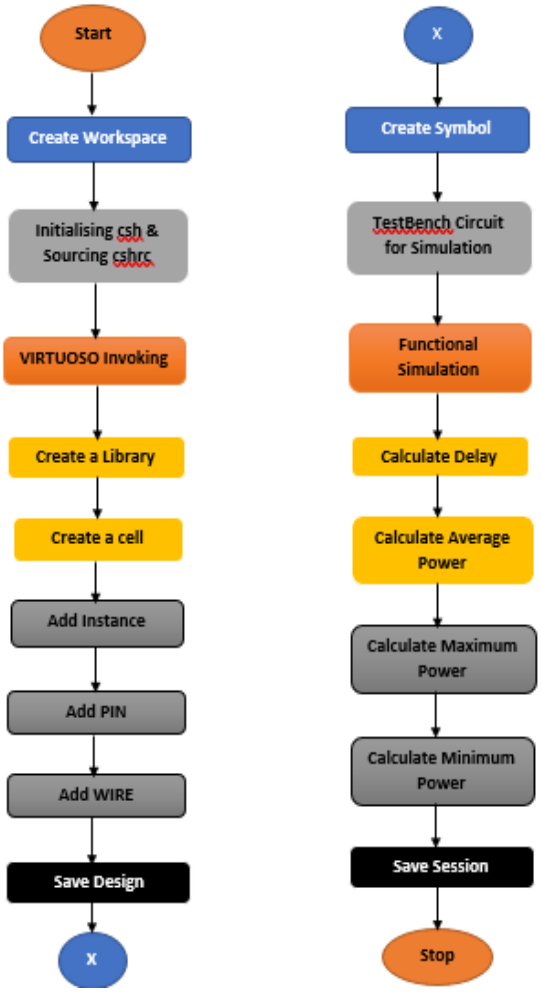

Fig 4.1: Flow Chart of Implementation & Working

V.RESULTS

Case 1: - NAND gate using CMOS 180nm Technology

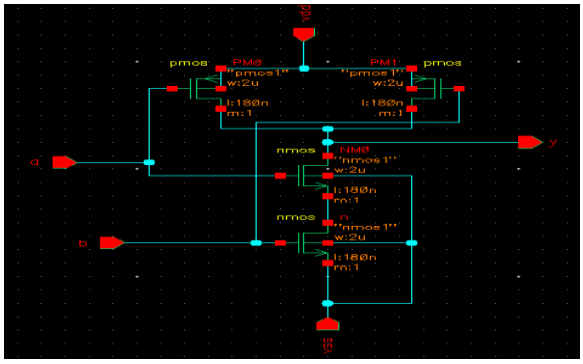

Fig 5.1.1: Circuit diagram of NAND gate using CMOS 180nm

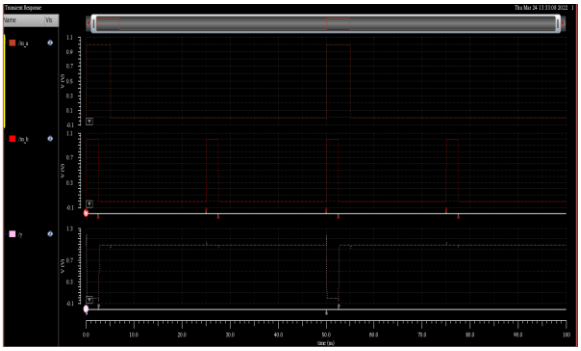

Fig5.1.2: Transient response of NAND gate in CMOS 180nm

delay(?wf1 v("/in_a" ?result "tran") ?value1 0.8 ?e...	22.9074p
average(getData(":pwr" ?result "tran"))	373.459n
ymax(getData(":pwr" ?result "tran"))	209.352u
ymin(getData(":pwr" ?result "tran"))	3.0781p

Fig 5.1.3: Results of NAND gate in CMOS 180nm

Case 2: - NAND gate using CMOS 90nm Technology

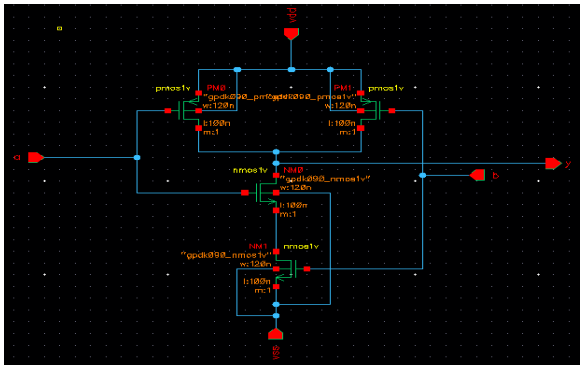

Fig 5.2.1: Circuit diagram of NAND gate using CMOS 90nm

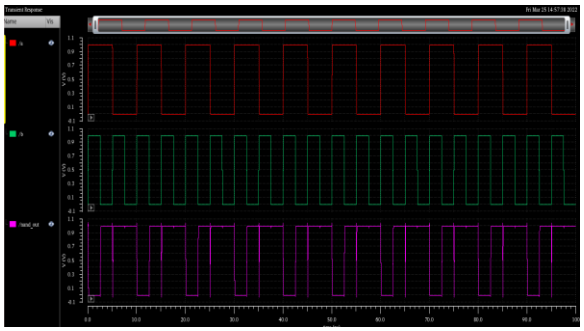

Fig 5.2.2: Transient response of NAND gate in CMOS 90nm

delay(?wf1 v("/a" ?result "tran") ?value1 0.8 ?edge1 "either" ?...	-8.96135p
average(getData(":pwr" ?result "tran"))	189.254n
ymax(getData(":pwr" ?result "tran"))	29.5809u
ymin(getData(":pwr" ?result "tran"))	259.19p

Fig 5.2.3: Results of NAND gate in CMOS 90nm

Case 3: - NAND gate using CMOS 45nm Technology

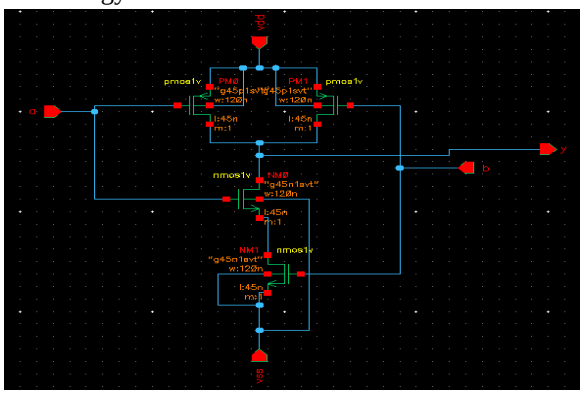

Fig5.3.1: Circuit diagram of NAND gate using CMOS 45nm

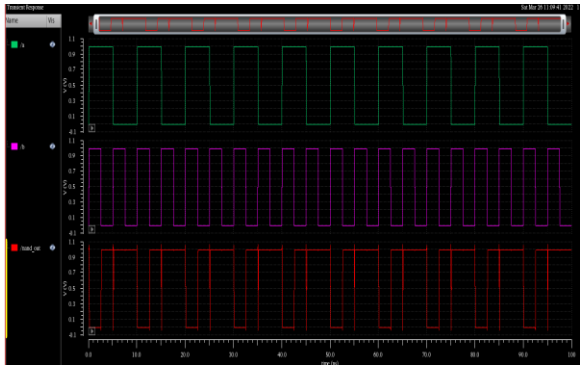

Fig 5.3.2: Transient response of NAND gate in CMOS 45nm

delay(?wf1 v("/a" ?result "tran") ?value1 0.8 ?ed...	-66.5683f
average(getData(":pwr" ?result "tran"))	74.708n
ymax(getData(":pwr" ?result "tran"))	21.7466u
ymin(getData(":pwr" ?result "tran"))	1.44136p

Fig 5.3.3: Results of NAND gate in CMOS 45nm

Case 4: - NAND gate using CMOS 18nm Technology

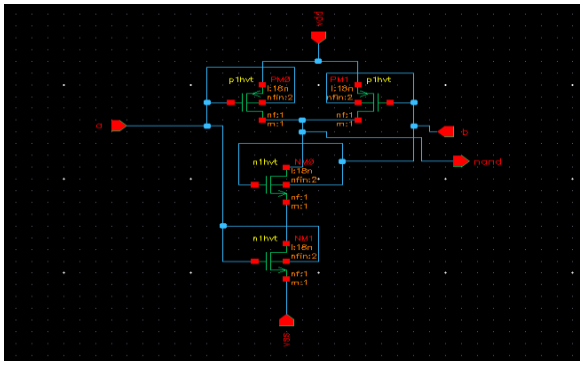

Fig 5.4.1: Circuit diagram of NAND gate using CMOS 18nm

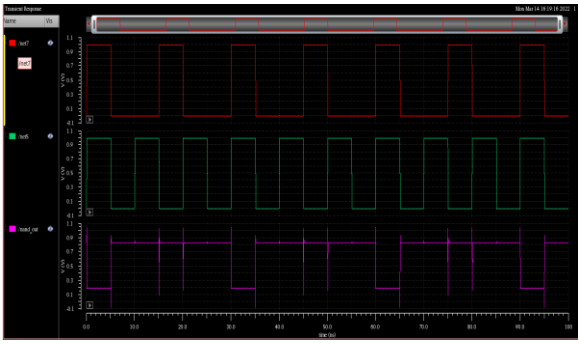

Fig 5.4.2: Transient response of NAND gate in CMOS 18nm

delay(?wf1 v("/net7" ?result "tran") ?value1 0.8 ?edge1 "either" ?nth1 1 ?td1 0.0 ?tol1 nil ?wf2 v("/nand_out" ?r...	-1.195p
average(getData(":pwr" ?result "tran"))	352.8u
ymax(getData(":pwr" ?result "tran"))	522.8u
ymin(getData(":pwr" ?result "tran"))	2.664u

Fig 5.4.3: Results of NAND gate in CMOS 18nm

Case 5: - D Flip-Flop using CMOS 180nm Technology

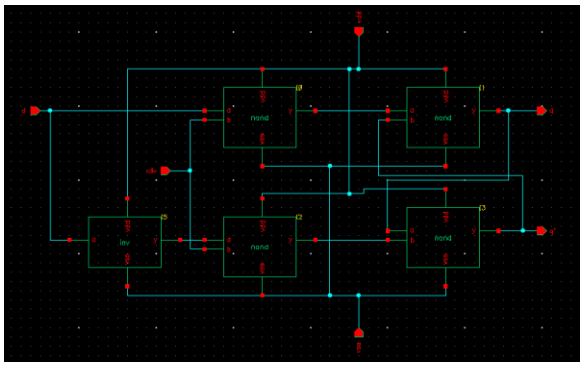

Fig 5.5.1: Circuit diagram of D Flip-Flop using CMOS 180nm

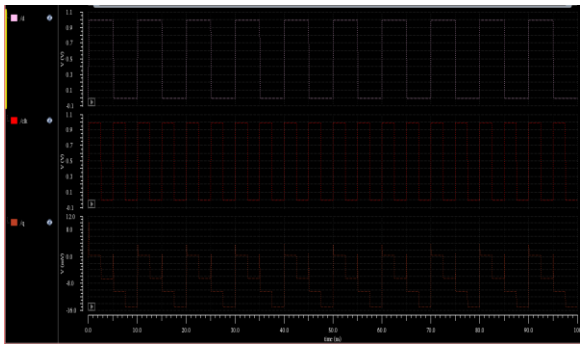

Fig 5.5.2: Transient response of D Flip-Flop in CMOS 180nm

average(getData(":pwr" ?result "tran"))	27.439n
ymax(getData(":pwr" ?result "tran"))	19.2057u
ymin(getData(":pwr" ?result "tran"))	0

Fig 5.5.3: Results of D Flip-Flop in CMOS 180nm

Case 6: - D Flip-Flop using CMOS 90nm Technology

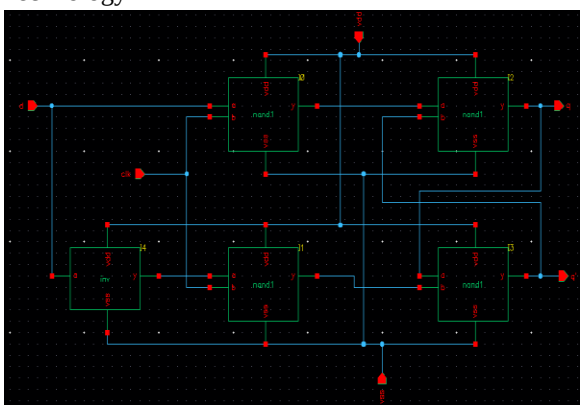

Fig 5.6.1: Circuit diagram of D Flip-Flop using CMOS 90nm

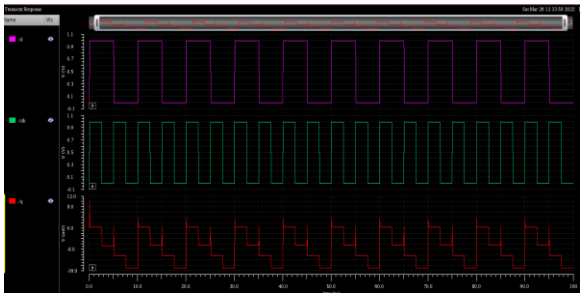

Fig 5.6.2: Transient response of D Flip-Flop in CMOS 90nm

delay(?wf1 v("/d" ?result "tran") ?value1 0.8 ?edge1 "either" ?nth...	18.1711p
average(getData(":pwr" ?result "tran"))	849.676n
ymax(getData(":pwr" ?result "tran"))	72.8967u
ymin(getData(":pwr" ?result "tran"))	30.1361n

Fig 5.6.3: Results of D Flip-Flop in CMOS 90nm

Case 7: - D Flip-Flop using CMOS 45nm Technology

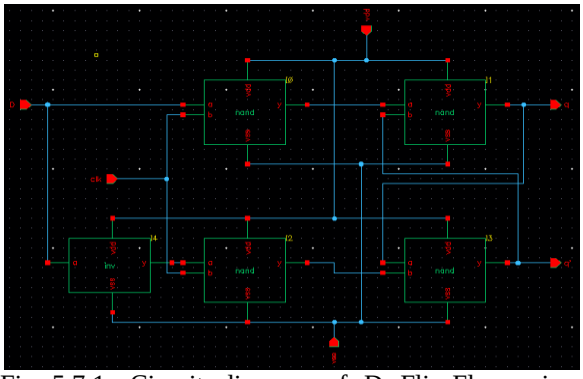

Fig 5.7.1: Circuit diagram of D Flip-Flop using CMOS 45nm

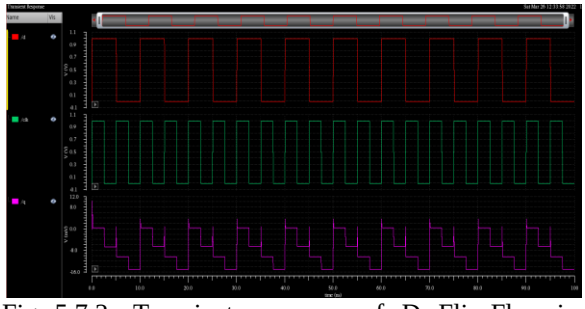

Fig 5.7.2: Transient response of D Flip-Flop in CMOS 45nm

delay(?wf1 v("/d" ?result "tran") ?value1 0.8 ?e...	21.2669p
average(getData(":pwr" ?result "tran"))	337.162n
ymax(getData(":pwr" ?result "tran"))	25.3562u
ymin(getData(":pwr" ?result "tran"))	25.6196p

Fig 5.7.3: Results of D Flip-Flop in CMOS 45nm

Case 8: - D Flip-Flop using CMOS 18nm Technology

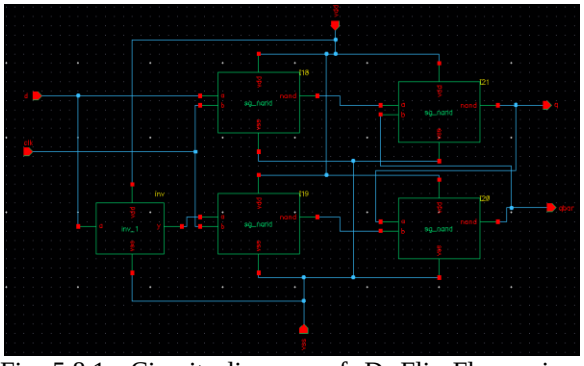

Fig 5.8.1: Circuit diagram of D Flip-Flop using CMOS 18nm

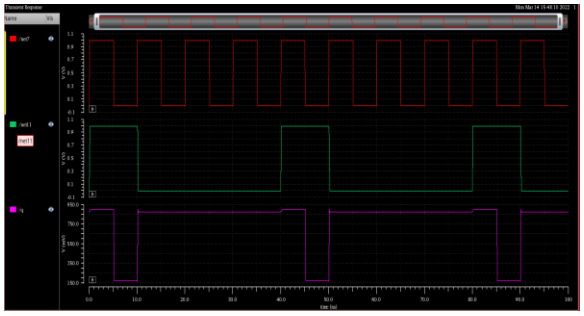

Fig 5.8.2: Transient response of D Flip-Flop in CMOS 18nm

delay(?wf1 v("/net7" ?result "tran") ?valu...	5.093n
average(getData(":pwr" ?result "tran"))	841.2u
ymax(getData(":pwr" ?result "tran"))	1.09m
ymin(getData(":pwr" ?result "tran"))	120.7u

Fig 5.8.3: Results of D Flip-Flop in CMOS 18nm

VI. DISCUSSIONS

Table1: Comparisons of results of NAND gate in different technologies

Parameters	CMOS			FINFET
	180nm	90nm	45nm	18nm
Delay(s)	22.9074p	-8.96135p	-66.5683f	-1.19503p
Average Power(w)	373.459n	189.254n	74.708n	352.771u
Ymax(power)	209.352u	29.5809u	21.7466u	522.844u
Ymin(power)	3.0781p	259.19p	1.44136p	2.66441u

The above table is the examination of results got

from the NAND gate in CMOS and FINFET in various advances.

We have considered four parameters like delay, average power, maximum power, minimum power and compared those parameters in different technologies. In CMOS, we have utilized 45nm, 90nm, 180nm advances and in FINFET we have utilized 18nm technology to plan NAND gate.

So, we can close from the above outcomes that CMOS 45nm technology is liked to plan the NAND gate.

Table2: Comparisons of results of D FLIP-FLOP in different technologies.

Parameters	CMOS			FINFET
Technology	**180nm**	**90nm**	**45nm**	**18nm**
Delay(s)	13.5497p	18.1711p	21.2669p	5.0931n
Average Power(w)	27.439n	849.676n	337.162n	841.181u
Ymax(power)	19.2057u	72.8967u	25.3562u	1.09003m
Ymin(power)	0	30.1361n	25.6196p	120.738u

The above table is the correlation of results got from the D-Flip Flop in CMOS and FINFET in various advancements.

We have considered four parameters like delay, average power, maximum power, minimum power and compared those parameters in different technologies. In CMOS, we have used 45nm, 90nm, 180nm technologies and in FINFET we have used 18nm technology to design D Flip Flop.

From the outcomes, delay, average power, maximum power, minimum power is gotten least in the CMOS 180nm technology when contrasted with different technologies. So, we can finish up from the above outcomes that CMOS 180nm innovation is liked to plan the D Flip Flop.

VII. CONCLUSION AND FUTURE SCOPE

CONCLUSION:

Thus, the NAND gate and D flip-flop are executed in various advancements like in CMOS 180nm, 90nm, 45nm innovations and FINFET 18nm innovation in the VirtuosoSchematic Editor. The useful way of behaving of the circuits are checked. The recreation of NAND entryway and D Flip-Flop in these CMOS 180nm, 90nm, 45nm innovations and FINFET 18nm advancements is performed utilizing Specter with Cadence device. After the recreations of the circuits, the got results are examined. The deferral, normal power, greatest power, least force of executed circuits is determined. The determined results are thought about. The innovation where the deferral and power are noticed less are recognized by breaking down the acquired outcome. The deferral andforce of NAND entryway are noticed less in CMOS 45nm innovation while in D Flip-Flop these are noticed less in CMOS 180nm innovation.

VIII.FUTURE SCOPE

- The evolution of IC computational capabilities has a significant impact according to how we create, process, communicate, and store data.
- The capability to decrease transistor size every few years is the driving force behind this phenomenal development.
- The optimization of the transistor fin will play a vital role during this evolution, as will subsequent reduction to lower scale.
- Scaling is a top priority for businesses since it minimises the size of computing hardware.
- More study is being done to see whether the FINFET can be scaled down to see if it improves efficiency.
- It's worth noting that a 14nm particle is about the same size as a virus.
- When it comes to scaling down a transistor, we have come a long way.

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