Design of Low Power and High Performance Ternary Content Addressable Memory(TCAM)

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***Abstract*— Ternary Content Addressable Memory (TCAM) based search engines play a significant role in network routers due to its faster and more precise searching operations. TCAM is one of the enhanced varieties of Content Addressable Memory (CAM). TCAM contains three logic states: 0, 1 and X. In TCAM, a search operation can be carried out in a single clock cycle. It is called a specific form of memory for this reason. A prominent feature of TCAM is its quick search functionality. The TCAM array operates in parallel in each site to compare the search and stored data. But the biggest drawback of TCAM is serious power dissipation. In this research, we presented a low power and high performance 8*8 TCAM implementation using the Lector technique to address this power dissipation.**

Keywords*— CAM, Leakage power, Lector technique, TCAM

I.INTRODUCTION

Memory plays a crucial role in today's computing systems from server design to embedded systems for use in automobiles.

Ternary content addressable memory produces the matching data after comparing input data in parallel with stored data (logic "0," "1," or "don't care"). Due to its predictable and fast searches that use parallel operation to check the stored data with the search words, TCAM finds uses in routers and some networking equipment.

In contrast to CAM, which searches the contents in the search lines and then obtains the matching address at the output, RAM requires an address to access memory-stored data. High-speed search operations are a feature of CAM. But since they operate at such fast speeds, CAMs use a huge amount of power and generate a lot of heat.

In the previous design, TCAM cell is designed with 14 transistors. 8*8 memory subsystem is designed by 64 TCAM cells and one AND gate as shown in Fig.1. when data bit is matches with search bit then match-line bit goes to high, otherwise low. In this Fig.1, the AND gate has 64-bit input which is match lines generated by individual TCAM cells. This 64-input AND gate is designed by using 3-stage 4-input AND gates, whose output becomes match-line word as shown in Fig.2. A key cause in power consumption is typically when the match lines are precharged to VDD and bringing them down to ground during a search operation due to a mismatch between stored data and search data.

To overcome this power consumption, Lector based low power and high performance Ternary Content Addressable Memory is designed.

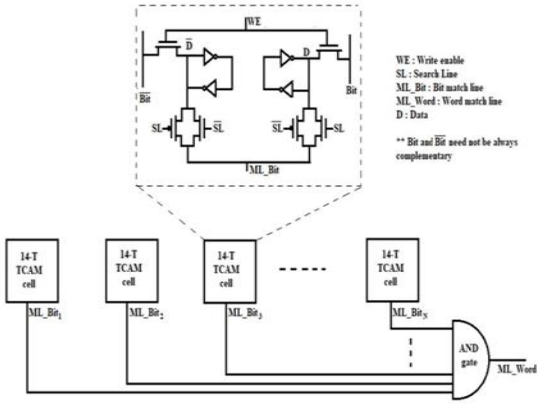

Fig.1: Existing TCAM Architecture

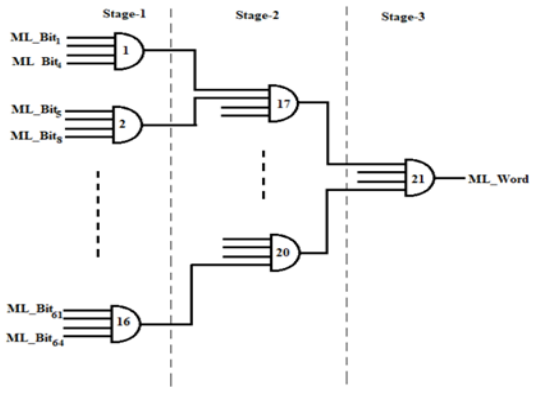

Fig.2: 64-input AND gate using 3-stage 4-input AND gates

II. PROPOSED ARCHITECTURE

Lector approach-based inverter is used instead of 2T-CMOS inverter because it controls the leakage power which is used in 14T-TCAM cell and also AND gate. In Lector approach, two leakage control transistors are placed in between pull-up and pull-down network whereby the source of one leakage control transistor (LCT) controls the gate terminal of the other. That's why there is no external circuitry is needed to control the leakage control transistors. "From the path supply to ground, a state with multiple transistors turned off is significantly less leaky than a state with just one transistor turned off". The inverter using Lector approach is shown as Fig.3.

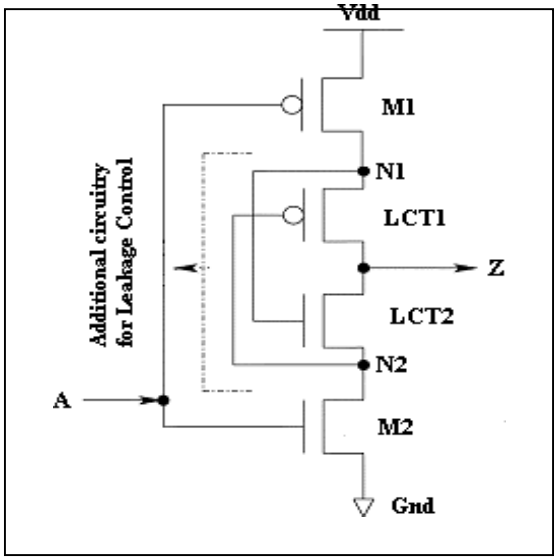

Fig.3: CMOS Inverter using Lector approach

One of the LCT is PMOS transistor which is placed under pull-up network and another LCT is NMOS transistor which is placed above the pull-down network. This is the additional circuitry for leakage control.

The node N2 voltage is 800 mV when Vdd = 1V and input A = 0. The voltage is insufficient to totally switch off LCT1, hence it cannot be done. As a result, conduction will be possible since the LCT1 resistance will be close to but somewhat lower than its OFF resistance. Even though it is not the same as the OFF resistance, LCT1's resistance increases the supply voltage's route to ground's resistance, which lowers sub-threshold leakage current and lowers leakage power. Similar to the previous example, when input A = 1, the node N1 voltage is 200 mV, causing LCT2 to function in a close to cutoff condition. In Table I, all potential input states for each transistor in the LECTOR inverter are listed.

TABLE 1: State Matrix for CMOS Inverter using Lector approach

Transistor Reference	Input(A)	
	0	1
M1	ON	OFF
M2	OFF	ON
LCT1	Near Cut-OFF region	ON
LCT2	ON	Near Cut-OFF region

The route resistance causes an increase in the gate's propagation latency as well. The LCT inverter's transistors are sized to minimize or maintain the propagation delay at its base case. The sleep transistors in the sleep-related approach must be able to isolate the power source and/or ground from the gate's other transistors. They must be made bigger to dissipate more dynamic power as a result. This cancels out any savings from the circuit being idle. The switching of sleep transistors requires extra circuitry, which consumes power in both the active and idle stages and is dependent on the input vector. Comparatively, LECTOR produces the necessary control signals inside the gate and is also vector independent.

Regardless of the amount of transistors in the pull-up and pull-down networks, the LECTOR approach adds two transistors to every line from Vdd to gnd. Forced stacks, however, have a full area overhead. With LCTs, the loading need is a constant and substantially less. In contrast, the loading requirements for forced stacks depend greatly on the number of transistors added. As a result, LECTOR suffers minimal performance decrease, and we circumvent the problem with forced stack approach.

The simulation waveforms can be seen in below Fig.4.

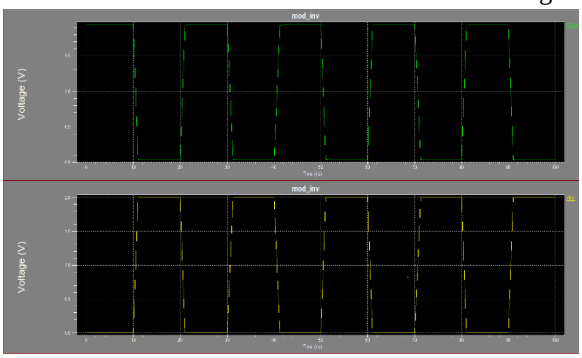

Fig.4: Simulation waveforms of Lector inverter

In the same manner, 4-input AND gate is also designed by using Lector technique as shown in Fig.5. In this AND gate, applying lector approach on inverter only.

With the help of these 4-input AND gates, 64-input AND gate is designed as shown in Fig.7.

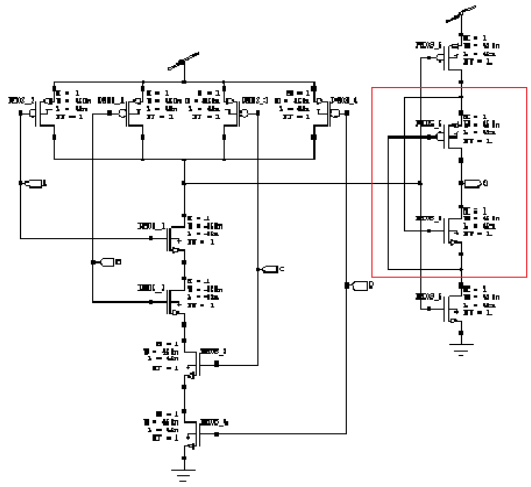

Fig.5: 4-Input AND gate using Lector Approach

The simulation waveforms for 4-input AND gate using Lector approach is shown as below Fig.6.

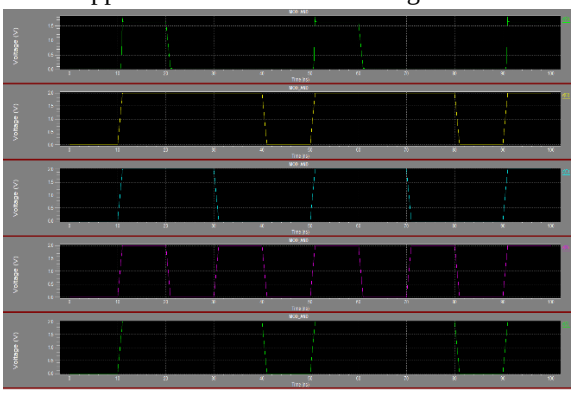

Fig 6: Simulation waveforms for 4-input AND gate

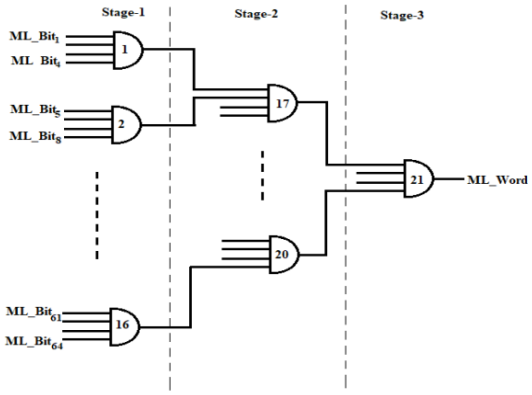

Fig.7: Modified 64-input AND gate using 3-stage 4-input AND gates

Modified TCAM architecture is designed by using inverter using Lector approach and AND gate using Lector approach. Replace normal CMOS inverter and AND gate with these Lector based CMOS inverter and AND gate. And then overall 8*8 TCAM architecture is designed and implemented as shown in Fig.8.

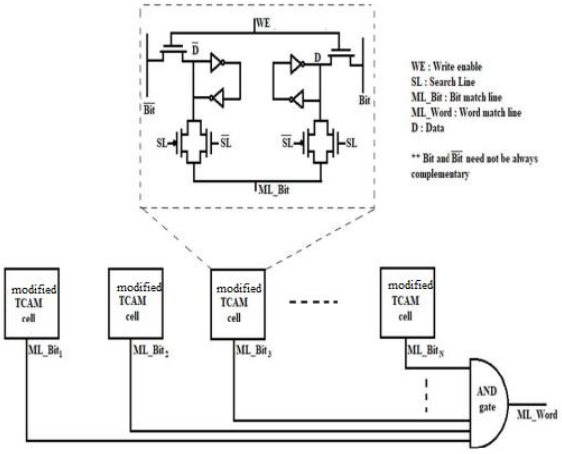

Fig.8: Proposed TCAM architecture

The simulation waveforms for Modified TCAM cell and proposed 8*8 TCAM architecture as shown in Fig.9 and Fig.10.

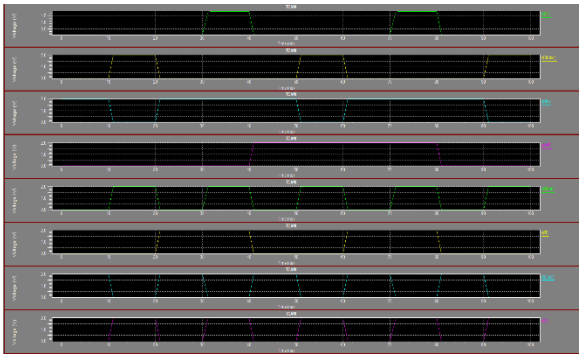

Fig.9: Simulation waveforms for Modified TCAM cell

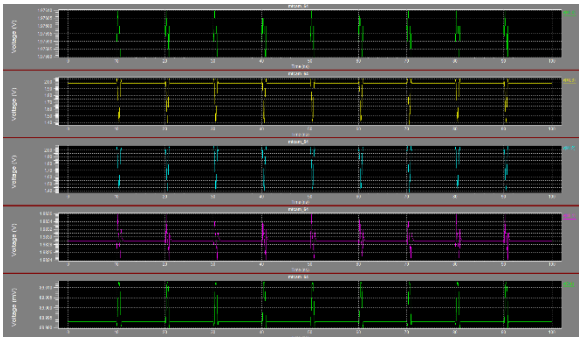

Fig.10: Simulation waveforms for Proposed 8*8 TCAM architecture

III. RESULTS

The power consumption and delay is measured using Tanner EDA 45nm technology. The results obtained through the lector technique for proposed TCAM architecture. The performance analysis is shown in Table 2.

TABLE 2: Performance Analysis

TCAM	POWER	DELAY
Existing	5.393 W	0.95024ns
Proposed	0.2766 W	0.68064ns

IV. CONCLUSION

The 8*8 TCAM architecture is designed by using modified inverter and AND gate in Tanner 45nm technology node. The modified inverter and AND gate is designed by using CMOS technology and also applying Lector approach. By adopting lector approach, power consumption is reduced by 95% and delay is reduced by 30%.

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