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Ultra-Low-Power and Area- Efficient Design of a Weighted Pseudorandom Test-Pattern Generator for BIST Architecture

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Abstract-A test pattern generator generates a pseudorandom test pattern that can be weighted to reduce the fault coverage in a built-in self-test. The objective of this paper is to propose a new weighted TPG for a scan-based BIST architecture. The motivation of this work is to generate efficient weighted patterns for enabling scan chains with reduced power consumption and area. Additionally, the pseudo-primary seed of TPG is maximized to obtain a considerable length in the weighted pseudorandom patterns. The maximum- length weighted patterns are executed by assigning separate weights to the specific scan chains using a weight-enabled clock.

Keywords: BIST, TPG, Genus

1. INTRODUCTION

Modern technology has focused on developing low-power systems for very-large-scale integration (VLSI) high-speed designs. As a result, several design strategies have been implemented to mitigate trade-offs between performance, power, and area. Instead, several approaches have concentrated on low-power dissipation during BIST normal-mode operations rather than test-mode operations. During the BIST test mode operation, the switching activity in the scan chains and test data compression using the appropriate TPG are crucial. Moreover, this testing should be achieved with high reliability and sensitivity in semiconductor designs. Figure 1 illustrates an example of a conventional pseudorandom TPG. The TPG linear function is accomplished according to the output feedback signal and the input seed bits. Its linear functionalities are used in many applications such as aircraft systems, cockpit systems, medical systems, audio and video systems, and power generation and distribution systems. A TPG consists of deterministic, exhaustive, pseudorandom, pseudorandom-weighted, and mixed-mode outputs. The pseudorandom-weighted output is used to achieve higher fault coverage in many BIST structures. The weighted pseudorandom TPG exhibits true randomness and repeatable patterns in all clock cycles. Typically, it requires one seed bit to produce one test pattern for n cycles of the scanning phase in the test-per-scan BIST, where n is the scan chain length. The latest study decreased the switching activity during scan shift cycles. Additionally, the TPG allows the automatic selection of weighted parameters to achieve its low power. The weighted pseudorandom TPG methods and their implementation in can effectively reduce the switching transitions. However, the methods included additional XOR transitions between the shift registers, it consumed more power and area. The concerned drawbacks are eliminated in the proposed design effectively.

The BIST requirements should mainly focus on the higher fault coverage and the lesser weighted switching activity with lower power and reduced area overhead. To achieve these requirements, two approaches can be utilized. One is to alter the circuit design of the weighted TPG. The other is to include additional hardware in the weighted TPG. Hence, in this paper, a new pseudorandom-weighted TPG is constructed using additional hardware. Additionally, higher fault coverage is achieved in terms of eliminating transition delay faults using test-point insertion. The test-points are inserted for every two NAND gate structures of the overall design area. The proposed technique involves swapping weighted test patterns to the scan chains using a phase shifter. The swapping of the weighted patterns considered for selecting the prior scan chains with lesser area is

compared with that of the other scan chains. The weighted patterns are hence used with all the scan chains of BIST architecture. This eliminates the faults at a specified output and improves the fault coverage's. The TPG also improves its rapid switching activity due to its selected weighted patterns and reduces its average scanning and capturing power consumption during BIST test-per-scan.

2. EXISTING METHODOLOGIES

The test patterns for BIST can be generated by MSIC-TPG using test per clock scheme or an architecture consisting of a Gray counter, Decoder and accumulator. The test vectors generated are applied to the multiplier circuit and faults are detected by comparing the response of the circuit with the expected response.

2.1 Pattern Generation

The pattern generation method for MSIC vectors uses econfigurable Johnson counter, seed vector and x-or operation. For every clock pulse, the reconfigurable Johnson counter generates the Johnson vector and the Linear feedback shift register generates a seed [9]. The Exclusive-or operations are done between Johnson counter and the seed vector in order to produce the test patterns. These produced vectors are shifted in to scan chains [9]. In the next clock pulse, the Johnson vectors will be circularly shifted and will bit-xor with seed. The resulted test patterns will be shifted in to the scan chains. The procedure is repeated until all the scan cells are loaded. Finally, the generated test vectors will be applied to the 4*4 multiplier circuit.

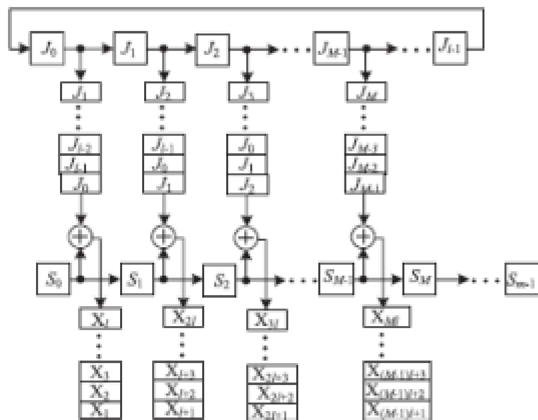

Figure 1.1: Test pattern Generation

2.2 Reconfigurable Johnson counter

The three different modes of operation for reconfigurable Johnson counter are initialization mode, circular shift mode and normal mode. Reconfigurable Johnson counter is constructed by using AND gate, a multiplexer and eight delay flip flops.

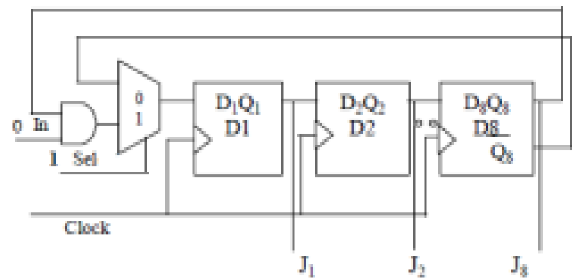

Figure 1.2: Initialization mode

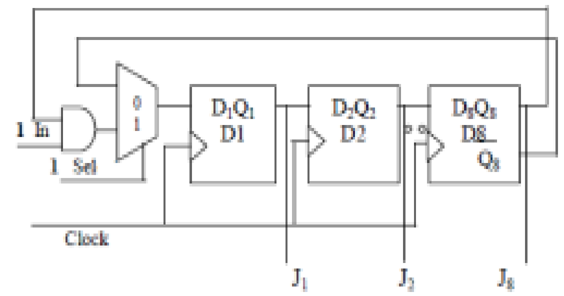

Figure 1.3: Circular shift mode

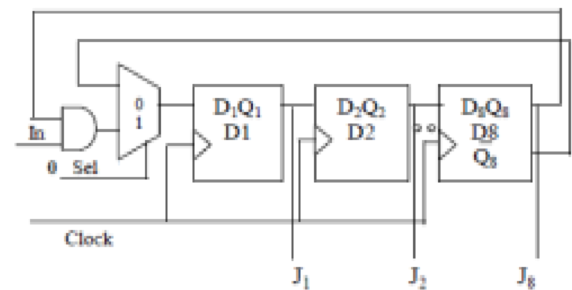

Figure 1.4: Normal mode

In initialization mode as shown in the fig 2, the reconfigurable Johnson counter will be initialized to all zero states by keeping 'sel' input of multiplexer at a value 1. In circular shift mode, the 'sel' input is made 1 and the input to the AND gate 'in' is made 1 by which the output Q8 is feedback as shown in the fig 3. To operate the reconfigurable Johnson counter in normal mode as shown in the fig 4, the 'sel' input of multiplexer is made 0 by which the inverted output of the last delay flip flop will be feedback.

2.3 TPG using test per clock

The outputs of the Johnson counter and seed generator are applied to the x-or gate to produce the test patterns. The clock and control circuit produces the clk1 and clk2 signals. The clk1 and clk2 are applied to the seed generator and Johnson counter respectively in order to produce the seed and Johnson vectors.

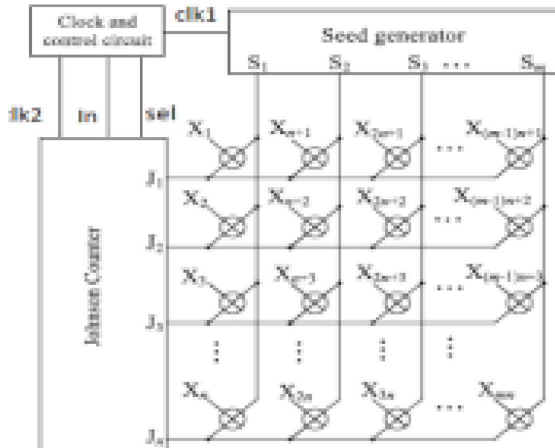

Figure 1.5: Pattern generation

The procedure for pattern generation is as follows
1. By applying clk1 to seed generator, the seed is produced.
2. A new Johnson vector is produced every time by clocking clk2.
3. By repeating 2, 2l Johnson vectors are generated.
4.For expected fault coverage, the steps 1-3 are repeated.

2.4 TPG using Gray counter
The test pattern generation using Gray counter, Decoder and accumulator architecture is shown in fig 1.6. The purpose of using gray counter is to prevent the unwanted signal transition at the input. As the patterns produced by the gray code counter has only single bit change between the subsequent test vectors, power optimization can be achieved. For every clock pulse, a 4- bit gray code is applied to the 3 to 8 decoder. The output of decoder is applied to the register B. The set and reset inputs are given to the registers in order to store the result. The outputs of two registers are given to a ripple carry adder and the final output test patterns are obtained from register A. The produced patterns are applied to the 4*4 multiplier circuit and the response obtained is compared with the forecasted result to verify the functioning of the circuit.

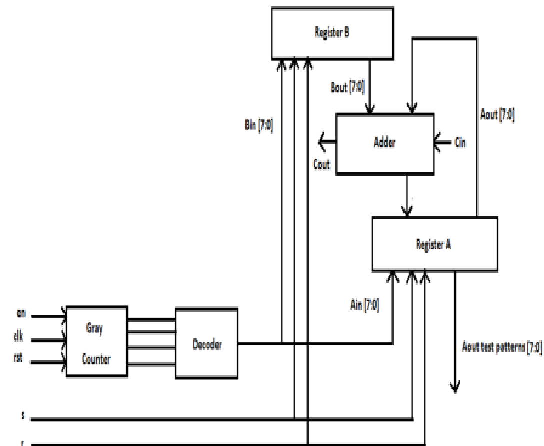

Figure 1.6: TPG using Gray counter

3. Proposed methodology
Compared with the existing methods, the proposed weighted TPG is designed with some advantages, including fewer switching transitions achieved using the specie weighted patterns and reduced power attained using fewer hardware components in the design. This reduces the hardware over-head and improves the fault coverage's in the BIST. The TPG method shown in Figure 1.7 is the proposed TPG, which includes the Galois operation and additional hardware for weighted pattern generation. The Galois operation in the proposed TPG is shown by the black dashed line and assumes constant pseudo-primary seeds (*A, X*) for simplification. However, the constant seed bits can be enlarged using the same subset of initial primary seeds. The seed subsets are used to achieve the maximum length in weighted patterns with less switching activity.
The additional hardware indicated by the blue line uses a smaller number of components for generating the weighted pseudorandom TPG output. In addition, the additional hardware design uses a weight- enabled clock, which enables specie weights through successive clock cycles. The particular weights are given to the respective scan chains through the weighted Mux. The weight generator clock selection effectively reduces the fault coverage in terms of the random-pattern resistant fault and the redundant faults in the BIST architecture. A 3-bit pseudorandom TPG is proposed according to the Galois scheme over a field of *GF (2m).* The test patterns are generated concurrently using the shift registers and Galois operation. The synchronous clock for the TPG leads

the bit sequences to be lost while it is incorporated for *m*-bits. Hence, the *m*-bit TPG is designed using asynchronous clocks in shift registers. The input vector bit (*X*) is multiplied continuously by the pseudo-primary seed bit (*A*) and added to the test vectors (*Z*). In addition, the state of the registers accommodates the multilevel parallelism in the TPGs. Consequently, the next *(i*C*1)*-th state after the *i*-th state is described in terms of the feedback loop structure.

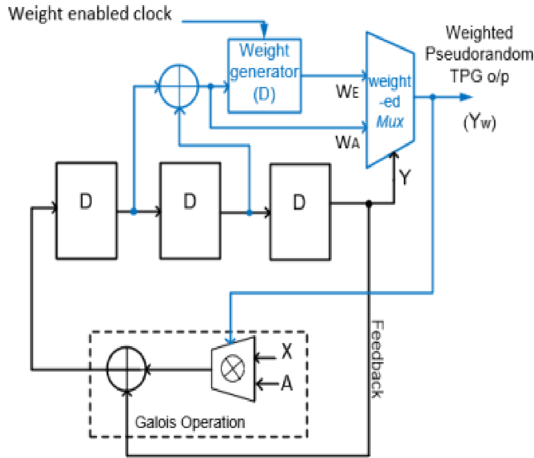

Figure 1.7: Proposed 3-bit weighted pseudorandom TPG

4. Simulation results & Comparison

The test pattern generation for BIST using different methodologies is coded in Verilog and implemented using Xilinx ISE 14.2 software. First, the weighted patterns WA generated with the probabilities of having '0' or '1' assigned to the certain scan chains occupy a smaller area. The output of the weighted Mux depends on the important feature of the pseudo randomness of the seed inputs. Consider a case in which Y0 will be swapped with Y1, Y2 until Yn, according to the value of the Galois operation (Z) in the proposed 3-bit TPG. Here, Y2 is Y, which is connected to the selection input of the Mux. This determines the weighted pattern. Hence, overall switching transitions in the scan chain primary inputs can be reduced by 25%.

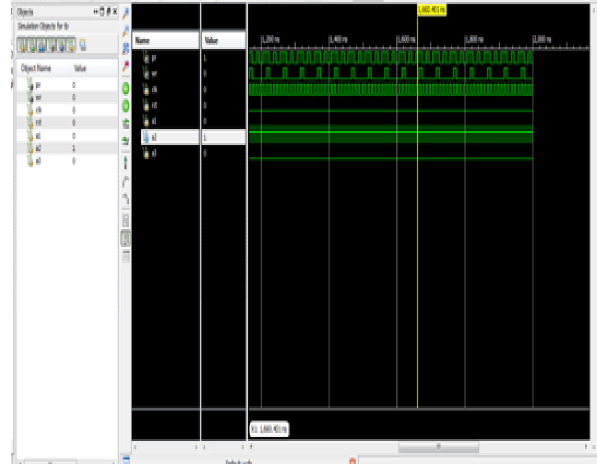

Figure 1.8: Proposed 3-bit weighted pseudorandom TPG

4.1 Cadence RTL Genus Tool

A standard cell design methodology makes use of standard cell library of a particular process technology and synthesizes the design. Synthesizing the design involves use of standard cells, constraint file, timing files of the technology used and produces a gate-level netlist made out of logic gates such as- AND, INV, Flip-Flop, OR etc. The gate-level netlist is obtained after running the synthesis. A gate-level netlist is a description of the circuit in terms of gates and connections between them. This gate-level netlist is again simulated using simulation software's to verify the correct functionality of the design. This sub-step is called post-synthesis gate- level simulation.

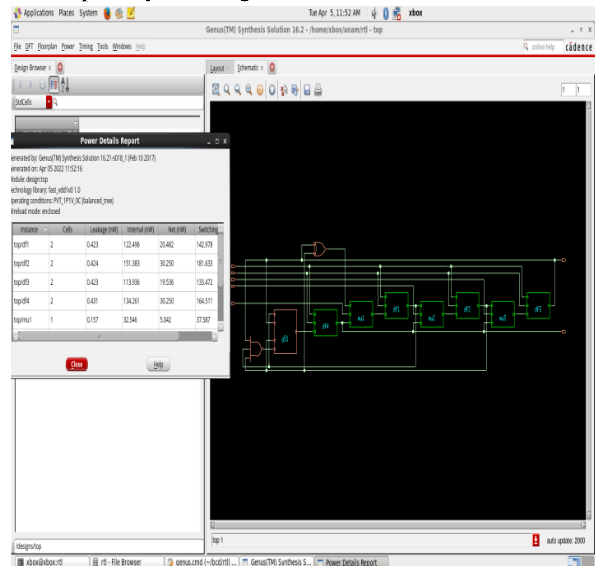

Figure 1.9: power report with synthesis results

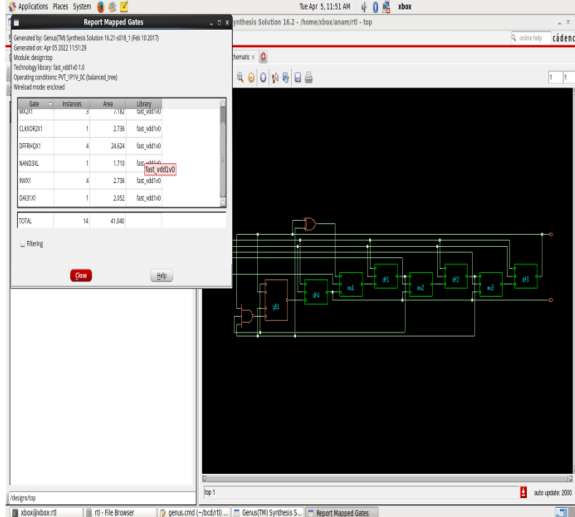

Figure 1.10: Area report with synthesis results

COMPARISONS

Related work	Circuit techniques		Objectives for scan chains test	Problem	Power reduction	Area-efficient
	Pseudorandom TPG	Weighted Pseudorandom TPG				
Jinyi et al. [5]	Galois adder and Galois multiplier for each tapping bit used	Not applicable for weighted patterns	No scan-in test done	Failed to produce weighted patterns	No	No
Barry et al. [17]	Galois adder and Galois multiplier for each tapping bit used		Alternative clock values of logic '0' and '1' used	Inefficient low-power operations for all scan chains	No	No
Xiang et al. [18]	Galois adder for each tapping bit used		The test enabled	More propagation delay and complicated design	Yes	No
Prasad et al. [16]	Multiplexer for each tapping bit and one XOR for convolution are used	Additional hardware components used		Higher switching transitions	Yes	Yes
Hwasoo et al. [19]	Galois adder for each bit used	Additional hardware components and XOR gates successive Galois adder are used	Chains of XOR gates are used with a D flip-flop estimator	Insufficient weighted patterns for larger pseudo-primary input	No	Yes
Proposed	One Galois adder, one Galois multiplier used for all tapping bits with an asynchronous clock	Additional hardware components including weight generator and weighted multiplexer are used	Weight-enabled clock used to enable the weights W_E, W_A using weight generator	Eliminated the problem of previous authors' work by using different valued weights. However, little propagation delay exists in the weight-enabled clock.	Yes	Yes

CONCLUSION

We have proposed a modified pseudo random architecture based on the development of VLSI architecture. In addition, according to the properties of pseudo random systems, based on different digital logic gates are proposed and designed. Moreover, an approximated VLSI structure computation method is designed and proposed. The simulation results are carried out from Xilinx 14.3 and synthesis results are extracted from Cadence Genus tool using 90nm technology.

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