Turbo Coder for LTE Implementation in VLSI Using Verilog HDL

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***Abstract*—Turbo codes are error correction codes that are widely used in communication systems. Turbo codes exhibits high error correction capability as compared with other error correction codes. This paper proposes a Very Large Scale Integration (VLSI) architecture for the implementation of Turbo decoder. Soft-in-soft out decoders, interleaver and Deinterleaver is used in the decoder side which employs Maximum-a-Posteriori (MAP) algorithm. The number of iterations required to decode the information bits being transmitted is reduced by the use of MAP algorithm. For the encoder part, this paper uses a system which contains two Recursive convolutional encoders along with pseudorandom interleaver in encoder side. The Turbo encoding and decoding is done using Octave, Xilinx Vivado, tools. The system is implemented and synthesized in Application Specific Integrated Circuit (ASIC). This paper presents the FPGA implementation simulation results for Turbo encoder and decoder structure for 3GPP-LTE standard.**

***Index Terms*—Turbo codes, Channel coding, Interleaver, SISO, Iterative decoder, MAP, Cadence, Xilinx Vivado.**

I. INTRODUCTION

Turbo coding is a very effective technique for correcting errors, which in recent years had a huge effect on channel coding. Turbo coding in digital communication is one of the most common and successful coding techniques for enhancing the bit error rate. Turbo encoder is to be an integrated module in the In-Vehicle Device embedded module by using the magnitude comparator. It is shown that proportional to chip size processing time also increased in the Turbo encoder parallel computing variant system. The usage of proposed logic resulted in efficient area and power usage. The Circuit complexity of proposed design Turbo encoder using magnitude comparator is little bit high [1]. Highly parallel decoders for convolutional turbo codes have been used by two parallel decoding architectures and a design approach of parallel inter leavers. A warm-up-free parallel sliding window architecture is proposed for long turbo codes to maximize the decoding speeds of parallel decoders. The warm-up-free PW architecture doubles the speed at a cost of hardware increase of 12% [2]. Turbo generally refers to iterative decoders intended for parallel concatenated convolutional codes as well as for serial concatenated convolutional codes. Implementation aspects like quantization issues and stopping rules used in conjunction with buffering for increasing throughput. Problem currently emerging, such as the analog decoding concept which allows the iterative process to be removed [3].

An arithmetic circuit which performs digital arithmetic operations has many applications in digital microprocessor, application specific circuits, etc. High speed ASIC implementation of a floating point arithmetic unit which can perform addition, subtraction, multiplication, division functions on 32-bit operands is used. Pre-normalization unit and post normalization units are also discussed along with exceptional handling [4]. Wireless communication standards such as 3GPP-LTE, WiMAX, DVB-SH and HSPA incorporates turbo code for its excellent performance. Turbo codes, capable of achieving close-to-Shannon capacity and amenable to hardware-efficient implementation, have been adopted by many wireless communication standards, including HSDPA and LTE. Turbo decoder uses original MAP algorithm instead of using the approximated Max log-MAP algorithm thereby it reduces the number iterations to decode the transmitted information bits [5]. A parallel concatenation of convolutional encoders via pseudo-random interleave for turbo coding the information

bits, which need to be transmitted. It generates sequences of systematic bits as well as non-interleaved and interleaved parity bits. The soft-demodulated values of transmitted bits are referred as a-priori probability values and are fed to constituent MAP decoders. Such MAP decoders are fundamentally based on algorithm that works on the principle of trellis graph, and it processes a-priority probabilities of systematic and parity bits to produce a-posteriori probability values of the transmitted information bits [6].

The extrinsic information is computed using a-posteriori probability values from the MAP decoder, interleaved/non-interleaved a-priori probability values, and interleaved/de-interleaved extrinsic information from another MAP decoder. Such extrinsic information values are shu²ed between these MAP decoders and are iteratively processed along with a-priori probability values to produce error-free a-posteriori probabilities of the transmitted bits [7]. Channel decoder is an integral part of wireless communication system and is responsible for reliable data communication. A channel decoder which employs turbo codes for error-correction delivers excellent bit-error-rate performance and it has made this code widely accepted by various wireless communication standards. Peak data-rates of 3G and 4G wireless communication standards which include turbo codes for error correction can be observed that the 3GPP-LTE (third generation partner- ship project - long term evolution) wireless standard has highest peak data-rate among 3G standards [8]. The inherent iterative process of decoding restricts turbo decoder to process data at higher data-rate. A great deal of work is going on the design of higher data-rate or throughput turbo decoders and their implementations have achieved throughputs up to 2.2 Gbps. However, wireless industry has already targeted milestone throughput beyond 3 Gbps for the next generation wireless communication standards [9].

An excellent theoretical justification on the near-optimal error-rate performance of turbo code. Interestingly, multiple types of turbo codes are reported in the literature such as serial-concatenation, self-concatenation and hybrid-parallel-&-serial-concatenation turbo codes. Additionally, various design aspects of turbo coding are comprehensively covered from Jet Propulsion Laboratory, specifically addressing turbo codes for deep-space communications [10]. The paper presents the implementation of SOVA decoder for different constraint lengths. Compared to a conventional SOVA decoder application, simulation results show power savings and area savings. The designers in developed a turbo decoder architecture in which utilizes both parallel SISO decoder tier and parallel trellis stage level. In the LTE-Advanced standard, the authors in paper present the design and implementation of a memory reduced Turbo decoder on the field programmable gate array (FPGA) [11].

Turbo codes are error correction codes that are widely used in communication systems. Turbo codes exhibits high error correction capability as compared with other error correction codes. A system which contains two Recursive convolutional encoders along with pseudorandom inter leaver in encoder side. The Turbo encoding and decoding is done using Octave, Xilinx Vivado, Cadence tools [12]. The system is implemented and synthesized in Application Specific Integrated Circuit (ASIC).Timing analysis has been done and file has been generated. Architecture processes soft-demodulated a-priori probability values in parallel using stack of multiple MAP decoders. Various contributions on this topic have been reported and are being adopted by latest wireless communication standards [13]. With the shrinking CMOS technology node in the semiconductor industry, such complex parallel-turbo decoder occupies nominal silicon area and consumes considerable amount of power. The communication through channel in wireless systems is more prone to errors than in wired systems, for the transmission of voice and data. So, the forward error correction coding must be used to reduce the probability of errors due to channel corruption of the information being transmitted. An efficient coding technique called turbo coding is preferred than more conventional coding systems, as it achieves a high level of performance [14]. Verilog models after translation, simulating Verilog-AMS models after the behavior-level conversion of SPICE parts, and simulating the mixed models with a Verilog- AMS simulator that supports referencing SPICE models. The approach of model translation and conversion has the disadvantages of translation overheads and a low translation compatibility from the SPICE model to the Verilog

model. The other approach has the disadvantage of no or low compatibility when referencing SPICE models [15].

In this paper a novel form of computation for Turbo decoder is proposed with a combination of clock gating and adaptable iteration in decoding to meet the LTE and LTE-advanced standards. The proposed work accomplished the power efficiency at maximum number of iterations by retaining the moderate data rate.

II. PROPOSED LOW-POWER TURBO DECODER

MAP algorithm is quite difficult to implement because of its design complexities. The major difference between the MAP and Max-Log-MAP algorithms is the computations of the values are in log domain and MAP algorithm will mainly perform the approximation. The approximated values are easy to implement. Approximations of MAP algorithm are reduced or avoided in Max-Log-MAP by applying the small correction in each steps to maximize the operation. This small modification leads to effective computations near to the MAP algorithm.

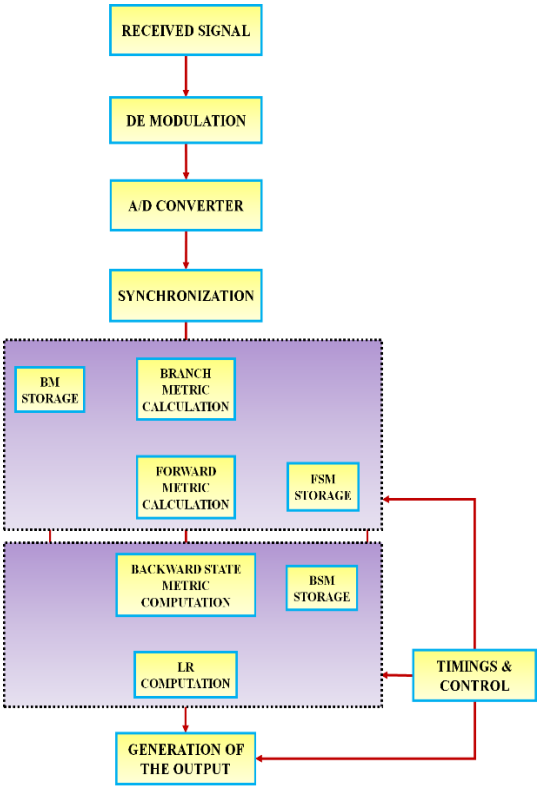

Figure 1. Turbo decoder computation flow

Turbo codes are most popular and are generally used in parallel concatenated to iterative decoding techniques. The standard structure of turbo decoder has interleaver, deinterleaver and two decoders. Branch Metric Unit (BMU) to calculate, Forward State Metric Unit (FSMU) to verify, Backward State Metric Unit (BSMU) to correlate Log Likelihood Ratio (LLR) for evaluation: are the four major segments in Log-MAP decoder. Calculation steps of Log-MAP decoder are illustrated as in Fig 3.3. The process of quantization is used to scale-up the received analog signal. The calculation is carried out in branch metric unit, this stage also has forward state metric unit along with the BMU.

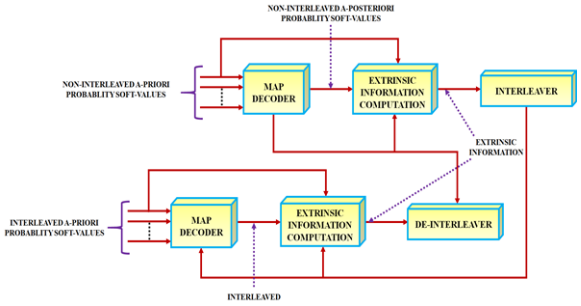

Figure 2. Turbo decoder

There is a trade-off between energy and bandwidth efficiency [4] while designing a channel code. The codes with bigger redundancy or lower rate can usually rectify maximum number of errors. The communication system is expected to communicate long distance with minimum transmit power. It uses the smaller antennas to withstand more interference to communicate at higher data rates. This leads to correct more number of errors. The code energy becomes more efficient from these properties. The low rate codes consume maximum bandwidth with high overheads. The high computational requirements develop the decoding complexities as the code length increases. In channel coding always process of encoding is easy and decoding in difficult. For every received noise power (N), bandwidth (W), channel type and signal power (S), the theoretical upper bound on the data rate is represented by R and only at this limit the transmitted data is error free. This limit is refers to Shannon capacity or channel capacity.

To decode the turbo codes most of the algorithms uses the divide-and-conquer method, because these codes are parallel concatenated codes. In turbo decoder, the

first decoder input is given by the output of the first encoder which is not scrambled where in the second decoder input is scrambled and this makes uncorrelated between two decoders. The two decoders will receive at maximum level by information exchange. The Convolution encoders with parallel concatenation are referred as pseudo-random technique. A parallel concatenation of convolutional encoders via pseudo-random interleaver for turbo coding the information bits, which need to be transmitted. It generates sequences of systematic bits as well as non-interleaved and interleaved parity bits.

A parallel concatenation of convolutional encoders via pseudo-random interleaver for turbo coding the information bits, which need to be transmitted. It generates sequences of systematic bits as well as non-interleaved and interleaved parity bits. On the other side, Fig. 3.2 shows a basic block diagram of turbo decoder which is an integration of constituent Soft-In Soft-Out (SISO) decoders with pseudo-random interleaver and de-interleaver. The soft-demodulated values of transmitted bits are referred as a-priori probability values and are fed to constituent SISO decoders, as shown in Fig.3.2 Such SISO [6] decoders are fundamentally based on algorithm that works on the principle of trellis graph and it processes a-priori probabilities of systematic and parity bits to produce a-posteriori probability values of the transmitted information bits. Thereafter, the extrinsic information is computed using a-posteriori probability values from the SISO [6] decoder, interleaved/non-interleaved a-priori probability values and interleaved/de-interleaved extrinsic information from another SISO decoder. Such extrinsic information values are taken between these SISO decoders and are iteratively processed along with a-priori probability values to produce error-free a-posteriori probabilities of the transmitted bits.

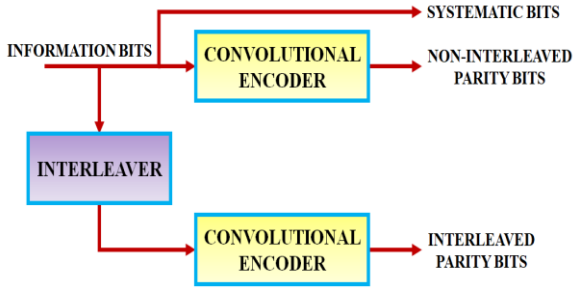

Figure 3. Turbo encoder

A. Clock Gating

To run multiple delayed cycles a control flag is developed to operate such components. Once the device stops execution, finally the combinational circuit linking registers are removed and the energy is saved due to the pipeline coordinates. The implementation of overall circuit requires additional circuit components to dissipate low power signals. Group of techniques are used to reduce the power dissipation in digital circuits are called as Dynamic Power Management (DPM) strategies [4]. A special type of circuits is used to disable the functionality when a circuit or portion of the circuit is not functioning at particular time duration to reduce the power consumption. A gate level circuit is used to achieve power reduction is called as ‘’gated clock” technique, which stops the clock supply to the sequential elements when output is same as input, as it is shown in Fig. 3.5 and activating the FF only when the input signal is different from the actual output value.

B. Adaptable Number of Iterations

The process of decoding will stop soon after the completion due to the adaptable number of iterations because iterations are not present. This technique reduces the time taken to decode after the decoding process gets over results in reduced decoding latency and achieves less power dissipation.

C. Blocking of Floating Inputs

The RAMs are used to read the data very quickly but the reduced access time expects the higher performance to go along with compose and read function. Consequently it should be stopped to minimize the scattering of state power. When floating inputs are occurred, AND or OR logic is utilized to restrict the entry of inputs by applying the command sign as 0.

III. IMPLEMENTATION

A. Architecture of Turbo Coder

Turbo encoder and decoder together comprises the Turbo coder architecture (shown in figure 1).Two identical Recursive convolutional encoders (RSC) and a pseudorandom inter leaver constitutes the turbo encoder (figure 2).LTE employs a 1/3 rate parallel concatenated turbo code. Each RSC works on two different data. Original data is provided to the first

encoder, while the second encoder receives the interleaved version of the input data. A specified algorithm is used to scramble the data bits and the method is called Interleaving.

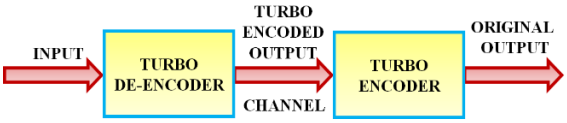

Figure 4. Turbo coder Block diagram

An appreciable impact on the performance of a decoder is seen with the interleaving algorithm when used. The RSC1 and RSC2 encoder outputs along with systematic input comprises the output of turbo encoder, that is, a 24 bit output is generated which is illustrated. This will be transmitted through the channel to the Turbo decoder. A standard turbo decoder block diagram is shown in Figure 3 that contains two modules of SISO decoders together with two pseudorandom interleaves and a pseudorandom de inter leaver.

The usually used method of turbo code decoding is carried out using the BCJR algorithm. The fundamental and basic idea behind the turbo decoding algorithm is the iteration between the two SISO part decoders which is illustrated in figure 3. It comprises a pair of decoders, those which work simultaneously in order to refine and upgrade the estimate of the original information bits. The first and second SISO decoder, respectively, decodes the convolutional code generated by the first or second CE.A turbo-iteration corresponds to one pass of the first component decoder which is followed by a pass of the second component decoder.

B. Interleaver and Deinterleaver

The interleaver is an important block in a channel coding of turbo codes. The interleaver or deinterleaver is also designed in parallel to meet the decoding specification of parallel turbo decoder. Contention of memory is a very common problem in interleaving and it resolved by adopting the contention free interleaver. In the proposed design, the block size is N,

$$(i) = A(i) mod NA(i) = fli + f2i2 \qquad (1)$$

Where, i=0, 1,2,…..,N-1

Where f1 is an odd number and f2 is an even number, 'i' is the index number of input data. yi and Π(i) is the index number after interleaving.

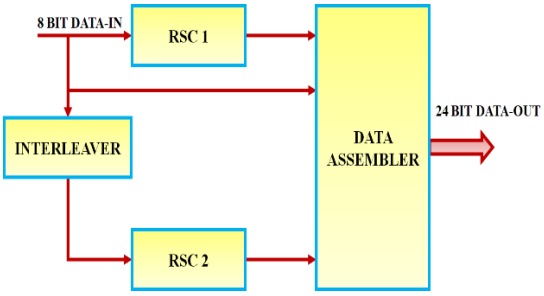

Figure 5. Turbo encoder Block Diagram

The generation of interleaving target address becomes difficult because the A (i) uses the real time multiplication operation, so the computation complexity increases as the index number I increases till N-1. The low complexity on recursion and the derivation is as follows.

From (1)

$$A(0) = 0, A(1) = f1 + f2$$
$$A(i + 1) - A(i) = f1 + f2 + 2i.f2$$
$$A(i + 2) - A(i + 1) = f1 + 3f2 + 2i.f2 \qquad (2)$$

Then,

$$A(i + 2) - 2A(i + 1) + A(i) = 2f2 \qquad (3)$$

Since A(1) is initial values as defined, the interleaving index is calculated by recursion from (2). From this method, no multiplication is required which reduces the computation complexity very effectively. The same address generator cannot be used in parallel design because the computation takes place simultaneously. Therefore, to solve this, parallel address generator is used.

C. SISO Decoder

The signal which is received at the input of a soft-in-soft out (SISO) decoder is the real (soft) value of that signal. An estimate of each input bit the decoder then generates an approximation for each data bit expressing the probability that the transmitted data bit is equal to one. The maximum a-posteriori (MAP) algorithm is used in the turbo-decoder under consideration in this paper for the SISO component decoder. The MAP algorithm never restricts the set of bit estimates to correspond strictly to a valid path through the trellis. Therefore, the results produced by a Viterbi decoder that recognizes the most likely true path through the trellis should differ from those generated by that.

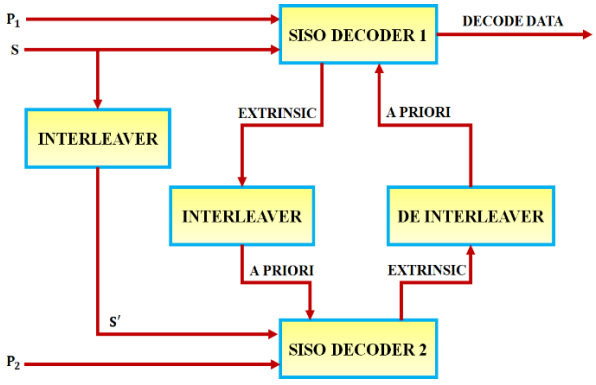

Figure 6. SISO decoder

The MAP algorithm minimizes the likelihood of bit error by using the entire sequence that was obtained to figure out the most likely bit at each trellis point. Consider a frame of *N* coded symbols consisting of *m* bits and the channel output received by the decoder as *y*. It is expressed in joint probabilities as:

$$P_r\left(d_i^{sym} = j|y\right) = \frac{P\left(d_i^{sym} = j, y\right)}{\sum_{k=0}^{2m-1}\left(P\left(d_i^{sym} = k, y\right)\right)} \quad (1)$$

The trellis form of the code allows the decomposition of computing the joint probabilities among the former and latter observations. The Forward recursion metric used in decomposing is shown in Equation 2. It provide the probabilities of state S instantly at i acquired from previous values from the channel. Backward recursion metric is also used to find the probabilities of the state calculated using the forthcoming values from channel and Branch metric.

$$P_r\left(d_i^{sym} = j|y\right) = \sum_{(S^t,S)/d_i^{sym}=j} \alpha_i\,(S')\gamma_i(S',S)\beta_{i+1}(S) \quad (2)$$

And the branch metric is given by

$$\gamma_i(S',S) = P(y_i|x_i).Pr^a\left(d_i^{sym} = d_i^{sym}(S',S)\right) \quad (3)$$

IV. RESULTS AND DISCUSSION

In this paper, the turbo encoder and decoder simulations are done using Verilog HDL. Vivado Design Suite is a Xilinx based software suite. It can be used to create and analyse HDL designs. Xilinx Vivado and Octave are used to simulate the recursive convolutional encoder and the Turbo encoder decoder. RTL is used to construct the net list. For logic synthesis and analysis in digital designs, the RTL compiler Ultra is utilised. The Encounter tool is used for physical design (floor layout, placement, and routing). The implementation tool takes a net list as input and optimises, places, and routes it.

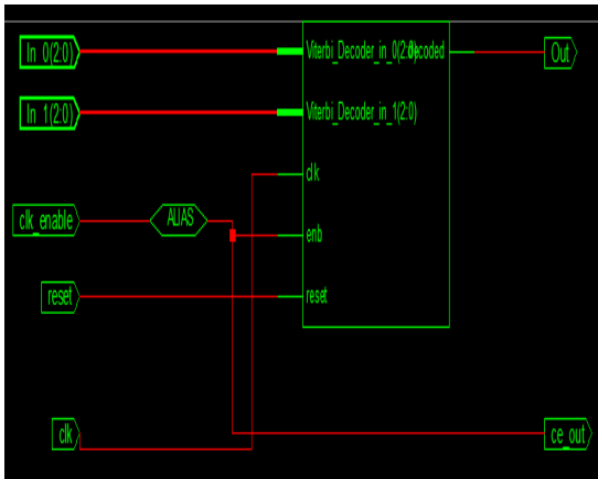

Figure 7. Top module of decoder

Turbo decoder is modelled using Verilog and the design is simulated on Modalism platform. The various sub units are called on the top module, which shows the implementation of Viterbi decoder. Here the cascaded Viterbi Decoder forms the turbo decoder of two inputs with variable data size.

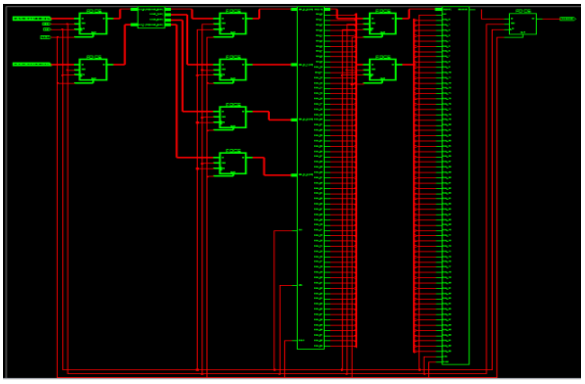

Figure 8. RTL schematic of turbo decoder

Enable signals en map are used for triggering MAP decoder which processes the soft-values to generate decoded a-posteriori LLR values. It is essential to monitor these LLR values processed by the MAP decoder which is implemented on FPGA board. Thereby, such values can be monitored using the multi-channelled logic analysers.

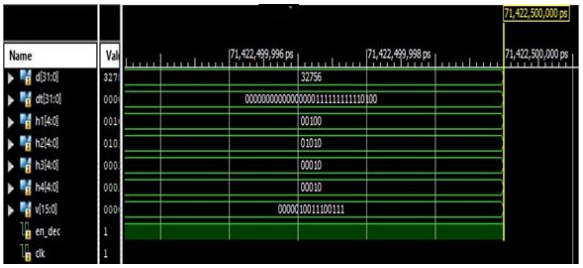

Figure 9. Simulation output

In this work, the main functional units of turbo decoder are analyzed. The significance of interleaver and types of interleaving blocks are demonstrated. The core of the turbo decoder finds many design and implementation issues are addressed with respect to VLSI chip integration.

V. CONCLUSION

The power consumption in 4G LTE wireless networks is illustrated. Along with this, the major sources of power dissipation in turbo decoder are discussed. Many possible power optimization techniques like contention free interleaver, memory cuts for parallel access, parallel architecture and SDR for iteration termination are proposed. The evaluation of the impact on power consumption and throughput due to optimizations at the architecture and algorithm level is proposed. In this work, the main functional units of turbo decoder are analyzed. The significance of interleaver and types of interleaving blocks are demonstrated. The core of the turbo decoder finds many design and implementation issues are addressed with respect to VLSI chip integration.

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