A 15 Level Multilevel Inverter Modelling and Simulation by using PDPWM Technique

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Abstract: **Incredible advances taking place in medium and high-powered applications of electric sector, different topologies of converters are flagging the way into it. Multi-Level Inverters (MLI) is one of the converters which deal with many applications by generating desired level of output voltages with various Pulse Width Modulation techniques. In this paper, a fifteen-level inverter has been discussed by using Sine wave Pulse width modulation technique along with Pulse Disposition (PD) modulation method to decrease harmonic content. Chosen switching patterns are given to MLI by designing suitable logic gate circuit. A detailed explanation on generating switching patterns by logic gates with binary coded representation, output voltage waveforms of inverters along with THD analysis are given in this paper with the help of MATLAB/SIMULINK.**

I.INTRODUCTION

In the present day generation, power electronic converters are playing a key role by converting into desired form in order to meet the different applications. Among all these, Multi Level Inverters (MLI) is drawing a serious attention in the fields of renewable energy penetration for the grid integration, Hybrid Electric vehicle systems, photo voltaic systems and the applications which deal with high voltage systems. These Multi Level Inverters are drawing a special attention because; one can generate high levels of output voltages by enhancing the circuit model and switching devices. Generation of high voltage levels is nearer to sinusoidal waveform which is having low distortions, low voltage stress and low switching losses. The system with low distortions can be useful and can be even fed to large rotational machines for required applications. Generally, Multi Level Inverters (MLI) is of different configurations
such are Diode clamped, flying capacitor MLI, cascaded H Bridge MLI, Modular Cascaded MLI, Hybrid MLI. Each type of configuration has its certain pros and cons along with its applications. Number of the switching devices like diodes, capacitors varies in each type of MLI though they are capable of producing many output voltage levels.
Out of all the basic three methods, Cascaded H Bridge can be designed with a smaller number of components and can generate high levels of output voltages by increasing number of voltage sources or capacitors and output can be obtained by different soft switching new techniques. Some of the PWM switching techniques are Single Pulse Width Modulation, Multiple Pulse Width Modulation, Sinusoidal pulse Width Modulation, modified pulse Width Modulation, phase displacement control, Advanced pulse Width Modulation techniques such as trapezoidal modulation, Staircase modulation, Stepped modulation, Harmonic injection modulation, delta modulation. In this paper, 15 level Multi Level Inverter is designed with the help of level shifting PWM process. Various methods such as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) methods are used in level shifting gating pulses. The switching patterns for 15 levels multilevel inverter are generated by Phase Disposition (PD) method and by designing logic gate circuitry.

II.CLASSIFICATION OF MULTILEVEL LEVEL INVERTER

Generally, there are 3 types of MLI. They are,
i. Neutral clamped (NPC) or Diode Clamped MLI.
ii. Flying capacitor (FC) MLI
iii. Cascaded H-Bridge (CHB) MLI.

Diode Clamped MLI

The diode-clamped inverter was also called the neutral-point clamped (NPC) inverter when it was first used in a three-level inverter in which the mid-

voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s. A three-level diode-clamped inverter is shown in Fig 1(a). In this circuit, the dc- bus voltage is split into three levels by two series-connected bulk capacitors, C1 and C2 . The middle point of the two capacitors 'n' can be defined as the neutral point. The output voltage Van has three states: Vdc/2 ,0 and -Vdc/2. For voltage level, Vdc/2 switches S1 and S2 need to be turned on; for -Vdc/2 , switches S1' and S2' need to be turned on; and for the 0 level, S2 and S2' need to be turned on. Fig. 1(b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage, Vdc the voltage across each capacitor is, Vdc/4 and each device voltage stress will be limited to one capacitor voltage level Vdc/4 through clamping diodes.

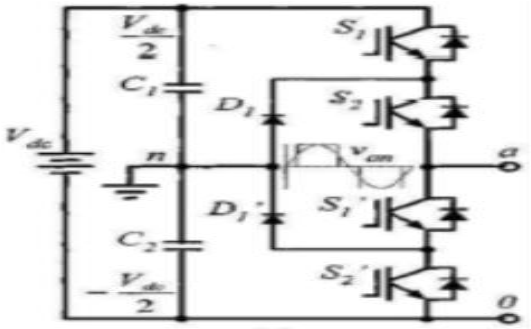


Fig1(a). Three-level Diode-clamped multilevel inverter circuit topology

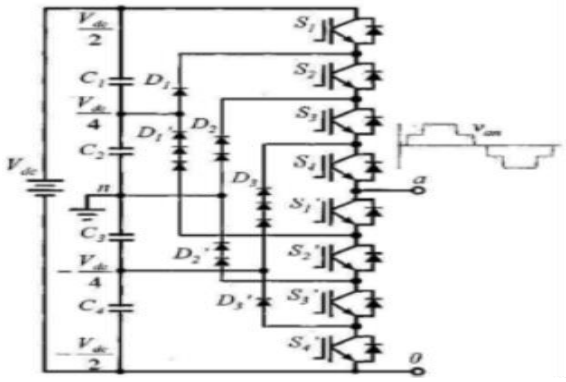


Fig1(b). Five-level Diode-clamped multilevel inverter circuit topology

Flying Capacitor MLI

The structure of this inverter is similar to that of the diode- clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Fig.2(a) & 2(b). shows the three-level and five-level capacitor clamped inverters respectively.

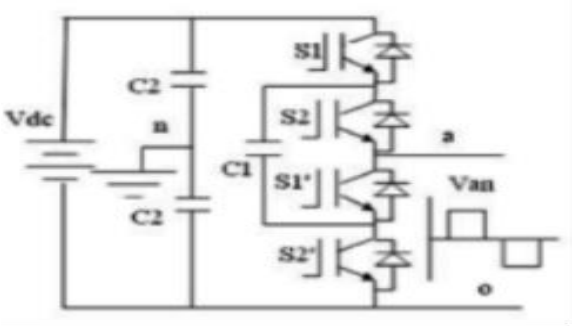


Fig2(a). Three-level Capacitor-clamped multilevel inverter circuit topology

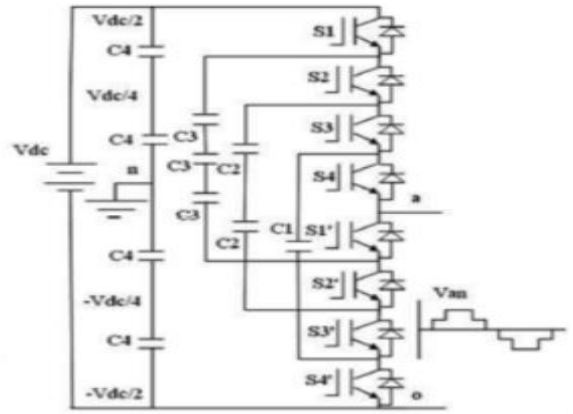


Fig2(b). Five-level Capacitor-clamped multilevel inverter circuit topology

Cascaded H-Bridge MLI

The most popular multilevel inverter topologies are diode clamped, flying capacitor and cascaded H-bridge multilevel inverter. The latter requires less number of power switching components, has higher efficiency and has simple circuit layout, all these aspects make it superior over the other topologies. Conventional single phase five level cascaded H-bridge multilevel inverter circuit with two H-bridge module is shown in Fig.2.5. The number of power switches required for a k levels inverter are $N = 2(k - 1)$. Each module of the H-bridge has its own DC input

voltage and consists of four power switching devices. Each module of the cascaded multilevel inverter can produce three levels of the output voltage which are +Vdc, 0 and −Vdc. The resulting phase voltage is synthesized by the addition of voltage generated by each H-bridge. As the demand for lower size & performance ratio of power converters increases, there is an increasing trend of reducing the numbers and size of power components in implementation of power converters. In cascaded H-bridge multilevel inverter implementation, reducing the numbers of main switching devices reduces the switching and conduction losses and increases the inverter efficiency.

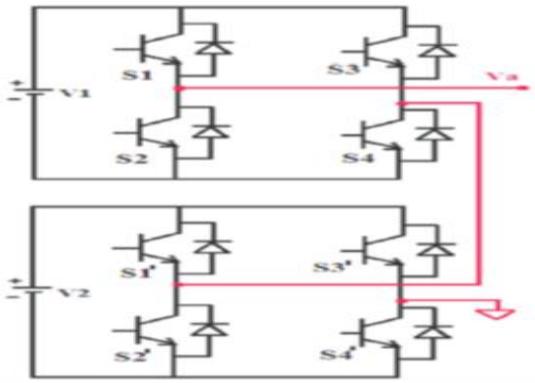


Fig 3. 5-level single phase cascaded H-bridge multilevel inverter

III.PROPOSED CIRCUIT

It is quite sure that in order to generate high levels of output voltage, one need to enhance number of voltage sources and switching devices along with the other associated components. The voltage sources can be replaced by batteries, super capacitors and PV cells. However, in recent trends, using of a smaller number of switching devices is focused much and also its associate components also serve the purpose due to its advantages. Most of the research papers also proposed different types of new configurations with the concept of reducing number of switches in the circuit. In the proposed 15 level Multi level inverter as shown in Fig.4, there are seven switches, three diodes and three voltage sources. One can have symmetric and asymmetric multi-level inverter type of design based on the voltage sources. If all the voltage sources in the circuit are equal, it can be referred to as symmetric MLI. If the voltages are different, it is said to be asymmetric configuration. In this circuit, asymmetric methodology is adopted such that it is maintained to have voltage source ratio in 1:2:4 which provide the flexibility for binary coded representation. Out of the available seven switches, four switches in right half of circuit is for polarization and acts as common H bridge for the generation of positive and negative cycles respectively. The remaining three switches are responsible for generating voltage levels. In order to generate enough gating signals, Multiple Carrier Pulse Width Modulation scheme (MCPWM) is adopted. In MCPWM, there are two types- level shifting method and phase shifting method. To generate 'L' levels of output voltage, it requires (L-1) number of carrier

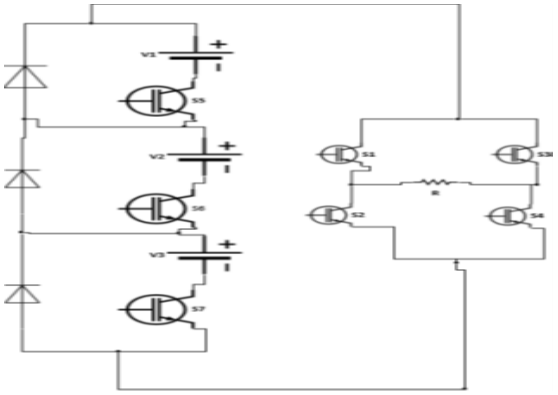


Fig 4. Proposed Multi level Inverter

signals. Similarly, to generate 15 levels, it needs 14 carrier signals consisting of seven positive pulses P7, P6, P5, P4, P3, P2, P1 and seven negative pulses N1, N2, N3, N4, N5, N6, and N7 which can be implemented in different fashions such as Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD) techniques. Among all these, Phase Disposition (PD) method is adopted in this proposed circuit as shown in Fig.5

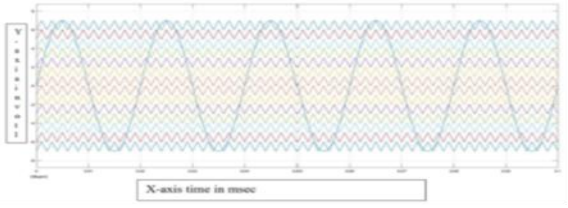


Fig 5. PD-PWM switching signals generated

Analysis of Logic Gates

Logical gate circuits play a very important role in decision making of systems and as well as controlling of systems. The logic gates operation mainly depends on two values in words "TRUE" or "FALSE" and in circuit model "0" or "1". The binary logic "1"

indicates ON state and binary logic "0" indicates OFF state. The basic logic gates which are used in constructing complex systems are AND, OR, NOT gates. In this proposed circuit, the desired switching pulses are done by these basic logic gates. For the generation of a greater number of required switching pulses, the basic logic gates are not sufficient so that for generation of a greater number of pulses, the circuit may even require different logic gates like EX-NOR, NOR, NAND Gates. The Required pulse sequence is generated with the comparison of reference sinusoidal wave (50 Hz) and carrier wave of frequency 1 KHz.

In order to get desired switching, binary coded representation was used in this paper as they provide flexibility in designing and for simple understanding. Based on the binary coded representation, the switching status for each switch is designed and they are represented in the logic sequence table, given below. In order to generate exact switching sequence to run the circuit, observe the basic logical gates and obtain suitable logic circuitry. For the switch generation of S5, seven pulses (P7⊕P6⊕P5⊕P4⊕P3⊕P2⊕P1) with the combination of Ex-OR are connected to one terminal of logic gate EX-NOR and similarly, 7 pulses N1⊕N2⊕N3⊕N4⊕N5⊕N6⊕N7 with the combination of Ex-OR are connected to second terminal of EX-NOR. This type of logic circuitry is designed based upon the careful examination of different available. Similarly, the remaining switching pulses for S6, S7 are also designed. The switching pattern for each switch is expressed with the help of following equations as given below.

S5=(((P1⊕P2⊕P3) ⊕P4⊕P5) ⊕P6⊕P7) ⊙ (((N1⊕N2⊕N3) ⊕N4⊕N5) ⊕N6⊕N7)

S7=P4+ N4

Time Divisons (secs)	Voltages	P7	P6	P5	P4	P3	P2	P1	N1	N2	N3	N4	N5	N6	N7	S5	S6	S7
0-0.00625	0V	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
0.00625-0.0125	+5V	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0.0125-0.001875	+10V	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
0.001875-0.0025	+15V	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
0.0025-0.003125	+20V	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1
0.003125-0.00375	+25V	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0.00375-0.004375	+30V	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0.004375-0.005	+35V	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0.005-0.005625	+35V	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0.005625-0.00625	+30V	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0.00625-0.006875	+25V	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0.006875-0.0075	+20V	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1
0.0075-0.00825	+15V	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
0.00825-0.00875	+10V	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
0.00875-0.009375	+5V	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0.009375-0.01	0V	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
0.01-0.01625	0V	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
0.01625-0.01125	-5V	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0
0.01125-0.011875	-10V	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0
0.011875-0.0125	-15V	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
0.0125-0.013125	-20V	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1
0.013125-0.01375	-25V	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
0.01375-0.014375	-30V	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
0.014375-0.015	-35V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0.015-0.015625	-35V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0.015625-0.01625	-30V	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
0.01625-0.016875	-25V	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
0.016875-0.0175	-20V	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1
0.0175-0.018125	-15V	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
0.018125-0.01875	-10V	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0
0.01875-0.019375	-5V	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0
0.019375-0.02	0V	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0

Table.1 Analysis of Logic gates

IV.SIMULATION CIRCUIT & RESULTS

Simulation Circuit for R-Load

In the proposed 15 level Multi level inverter as shown in Fig7(a), there are seven switches, three diodes and three voltage sources. One can have symmetric and asymmetric multi-level inverter type of design based on the voltage sources. If all the voltage sources in the circuit are equal, it can be referred to as symmetric MLI If the voltages are different, it is said to be asymmetric configuration. Out of the available seven switches, four switches in right half of circuit is for polarization and acts as common H bridge for the generation of positive and negative cycles respectively. The remaining three switches are responsible for generating voltage levels.

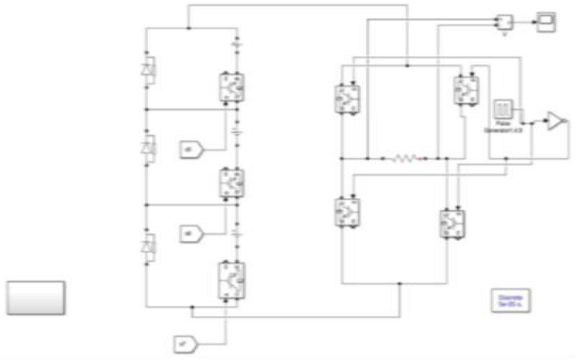


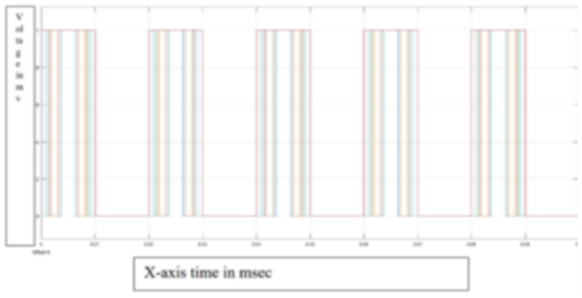
Fig 6(a). Simulation diagram of a 15 level ASCHBMLI with PD-PWM technique for R-Load

In order to generate enough gating signals, Multiple Carrier Pulse Width Modulation scheme (MCPWM) is adopted. In MCPWM, there are two types- level shifting method and phase shifting method. To generate 'L' levels of output voltage, it requires (L-1) number of carrier signals. Similarly, to generate 15 levels, it needs 14 carrier signals consisting of seven

positive pulses P7, P6, P5, P4, P3, P2, P1 and seven negative pulses N1, N2, N3, N4, N5, N6, and N7 which can be implemented in different fashions such as Phase Disposition (PD). The 15 level Multi Level Inverter is designed and simulated with the help of MATLAB as shown in the Fig 7(a).

Pulse Patterns

In order to generate exact switching sequence to run the circuit, observe the basic logical gates and obtain suitable logic circuitry. For the switch generation of S5, seven pulses (P7⊕P6⊕P5⊕P4⊕P3⊕P2⊕P1) with the combination of AND are connected. similarly, 7 pulses N1⊕N2⊕N3⊕N4⊕N5⊕N6⊕N7 with the combination of Ex-OR are connected to second. The required fourteen gating pulses consisting of positive and negative pulses are obtained as shown in the Fig 6(b)



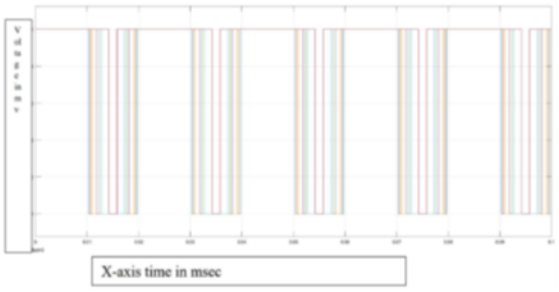


Fig 6(b). Positive and Negative Pulse patterns for R-Load

Simulation Results for R-Load

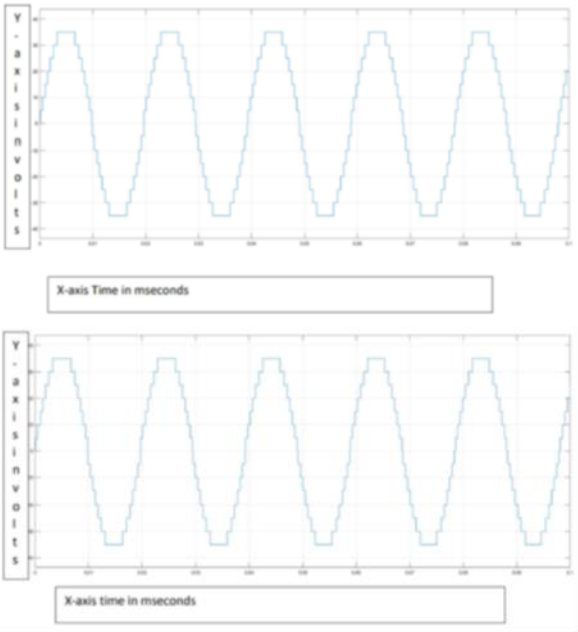


Fig 6(c). Output voltage for 15 level Inverter for R load.

Simulation Circuit for RL-Load

In the proposed 15 level Multi level inverter as shown in Fig 7(a) there are seven switches, three diodes and three voltage sources. One can have symmetric and asymmetric multi-level inverter type of design based on the voltage sources. If all the voltage sources in the circuit are equal, it can be referred to as symmetric MLI If the voltages are different, it is said to be asymmetric configuration. If all the voltage sources in the circuit are equal, it can be referred to as symmetric MLI If the voltages are different, it is said to be asymmetric configuration. It consists of one Sine Wave, Repeating Sequences are 14, Relational operators are14.for the switches ON -OFF we are using the logical operators (NOT, AND gates).

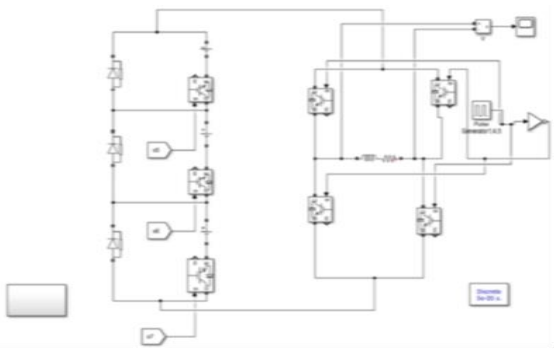


Fig 7(a). Simulation diagram of a 15 level ASCHBMLI with PD-PWM technique for RL-Load.

In order to generate exact switching sequence to run the circuit, observe the basic logical gates and obtain suitable logic circuitry. For the switch generation of S5, seven pulses (P7⊕P6⊕P5⊕P4⊕P3⊕P2⊕P1) with the combination of AND are connected. similarly, 7 pulses N1⊕N2⊕N3⊕N4⊕N5⊕N6⊕N7 with the combination of Ex-OR are connected to second. The required fourteen gating pulses consisting of positive and negative pulses are obtained as shown in the Fig. 7(b)

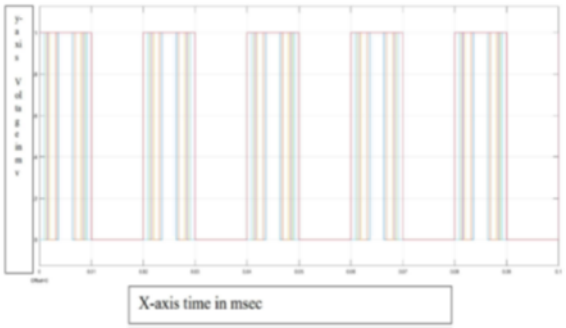


Fig 7(b). Positive and Negative Pulse patterns for RL-Load

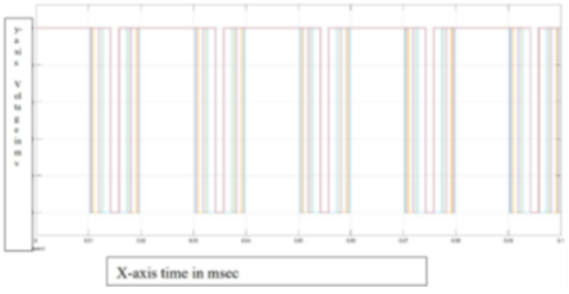


Fig 7(c). Output voltage for 15 level Inverter for RL load.

THD Analysis of Low & High Switching for ASCHMLI

THD analysis is performed for both R and RL loads are shown in the Fig. 8(a) & 8(b)

Fig 8(a) THD Analysis for R-Load

Fig 8(b) THD Analysis for RL-Load

V.ANALYSIS OF SIMULATION RESULTS

The simulation was implemented in MATLAB-Simulink version R2016a.This section presents the results of the simulation output waveform comprising of 15 level was produced. PDPWM technique is used for further improve the reliability of multilevel inverter. Based on the logic gates operation gate pulses are generated, the required fourteen gating pulses consisting of positive and negative pulse are obtained as shown in fig. 6(b) for R-Load and fig 7(b) RL-Load. The 15 Level output voltage was peak magnitude of 35 volts with a step voltage of 5 volts for R-Load and for RL-Load. The load parameters are R=10 Ohms, L=1mH for R & RL loads. More over the THD (Total harmonic Distortion) in the load output voltage waveform is 7.30 % for R-Load and 7.20 % for RL-Load. Without using PDPWM technique the THD value is 8.16 %. Hence it is concluded that PDPWM technique gives the less THD than conventional control.

VI.CONCLUSION

A symmetrical Cascaded H bridge Multilevel inverter (SCHBMLI) and Asymmetrical Cascaded H Bridge Multilevel Inverter (ASCHBMLI) has been analyzed in this report. Generally, in a 15-level number of bridges is7, Number of sources are 7 and switches present are 28. But our work carried out on the asymmetric cascaded H-Bridge multilevel inverter uses3 sources, 1 bridge and no of switches are 7.by using PD-PWM

technique The THD analysis for the proposed 15 level MLI is performed and presented. It can be noted that Harmonic content increases with R load 7.30% THD than RL load 7.20% THD with Phase Disposition PWM technique. Implementation of Multicarrier PWM concept to higher Multi level Inverters ensure the high efficiency with less distortions.

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