Low-Power Timing-Error Control Using a Timing Error Tolerant Circuit Technique

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Abstract- Real-Time operating conditions of digital integrated circuits play a key role in state-of-the-art systems. The overhead resulting from margining for worst case conditions is now a major energy contributor. In this paper a timing error tolerant circuit technique for low- power timing- error control is proposed. Controlling the transparent window of the clock enables the critical path to detect and correct the timing error-induced irregular data transition that occurs after the clock's rising edge. The timing error is directly corrected by a small amount of logic. It also introduces a time borrowing strategy, which corrects for future errors. The time-borrowing technique can be used at any site that has a quick flip-flop setup time. The timing error occurs in two stages sequentially, the arranged CLK in the second stage keeps a transparent window open long enough to allow regular data to be saved without modifying the system CLK.

Keywords: Timing-Error, flip-flop setup time, data transition, CLK, time-borrowing technique

1 INTRODUCTION

The lightweight in situ error detection and correction technique uses a soft-edge flip-flop combined with in-latch transition detection and a set-dominant error latch to detect data path transitions after the clock edge. Inherent error correction is achieved through time borrowing in soft-edge flip-flops. The technique is implemented in an ARM Cortex M0 microcontroller system in 40-nm CMOS, rendering the microcontroller "timing error aware." Post-fabrication sorting of ICs according to their (measured) performance (binning) is a typical low key solution, but comes with a high test cost scaling with production volume. However, the throughput decrease and energy per operation increase should be taken into account [1]. By modifying a clock in a flip-flop, the proposed system can recover a timing error without the loss of time in the clock-based system. Furthermore, due to the compact mechanism, this system has low hardware overhead in comparison with existing timing-error-tolerant systems that can recover the error instantly. The maximum allowable frequency (MAF) is used to evaluate the performance of this system and other timing-error-tolerant systems that can detect and correct the error instantly [2]. However, it is not able to prevent the timing violation in the successive critical path (SCP) and critical feedback path (CFP) structures. Furthermore, this technique is more effective in terms of the performance improvement. The DFFC technique is not able to prevent timing violation in problematic path structures [3]. The scheme combines ideas from error correction codes with the self-checking capability of MVM. Field-programmable gate array evaluation shows that the proposed scheme can significantly reduce the overheads compared to the protection of each MVM on its own. Therefore, the proposed technique can be used to reduce the cost of providing fault tolerance in practical implementations [4].To ensure an error free design, timing constraints are usually set based upon the longest path delay from static timing analysis (STA). The entire design flow uses Synopsys Electronic Design Automation (EDA) tools and customized scripts, which can be adapted for other designs [5]. Alpha particles and atmospheric neutrons induce single-event upsets, affecting memory cells, latches, and flip-flops. However, as the whole situation is getting worse, solutions that protect the entire design are mandatory. Solutions for detecting the error in logic functions already exist, but there are only few solutions allowing the correction, leading to a lot of hardware overhead in no processor design. A novel technique that includes several hardware architectures and an algorithm for their implementations, which reduces the cost of rollback in any kinds of circuit [6]. Inspired by the Markov random field (MRF) theory, a two-stage voting system is implemented in CDMR, including a first stage optimal MRF structure and a second-stage high-performance merging .The output error rate of the proposed method is still the lowest among all

designs [7].The power consumption of SFQ circuits can be reduced by the lowering critical currents of the Josephson junctions (JJs), or the bias voltage. Moreover, if a small error rate (for example 10−6) is acceptable, further improvement in energy efficiency would be expected at significantly higher clock frequencies than would be the case if the SFQ circuit must exhibit error-free operation. Moreover, because of the dynamic behavior of JJs under reduced voltage, the effects of bias current fluctuation are more complicated in LV-RSFQ circuits [8]. In place of the well-studied synchronous NoCs, the event-driven asynchronous ones have emerged as promising replacement thanks to their strong timing robustness especially when implemented in quasi-delay-insensitive (QDI) circuits. Recovery from router data-path faults usually requires adaptive routing support from the routing layer, which is left as the future work [9]. A snapshot of the data path's activity just before the launch of the next clock to determine if a timing error will occur. A novel EDaC technique that is inherently robust to false errors and thus avoids the overhead associated with extra hold constraints. Furthermore, the wide detection scope guarantees robust error detection over a wide supply and frequency range and aids to prevent over tuning under varying activity patterns [10].

In this paper, a timing-error-tolerant technique is proposed that, via a simple process, may rapidly resolve a timing error. Controlling the clock's transparent window allows the critical path to detect and fix the timing error-induced irregular data transition that occurs after the rising edge of the clock. A small amount of logics directly corrects the timing error.

2 RECENT WORKS

Chung-Hsun Huang *et al* [2020] [11] have discussed an error-detection-and-correction-free voltage scaling technique based on spatial–temporal error spreading and voltage dithering (ESVD) for video processing data paths. By leveraging the persistence of vision and the tendency of the human eye to mix pixels in close proximity, the suggested ESVD alleviates the reduction in visual quality caused by timing errors due to the lower supply voltage without explicit detection and correction. This ESVD reclaims voltage margins and improves energy efficiency while retaining QoE without any TED or TEC.

Cheng-Yao Hong *et al* [2020] [12] have proposed a variation-resilient microprocessor architecture with a two-level timing error detection and correction (EDAC) system. The proposed EDAC system first performs circuit-level error correction through time borrowing when a timing error occurs and subsequently employs a system-level error correction scheme if the timing error is relatively large and cannot be resolved within a cycle. The proposed EDAC system was designed and implemented on an ARM Cortex-M0 microprocessor using a 28-nm CMOS process. Increases the implementation effort and overhead and severely limits the feasibility of latch-based EDAC systems.

François Rivest *et al* [2020] [13] described a new timing error cost function for binary time series prediction. The ability to make predictions is central to the artificial intelligence problem. While machine learning algorithms have difficulty in learning to predict events with hundreds of time step dependencies, animals can learn event timing within tens of trials across a broad spectrum of time scales. This paper focuses on binary time series that can be predicted within some temporal precision. Then, suggested the squared timing error (STE) that uses DTW on the event space and applies SSE on the timing error instead of at each time step. The results in real-world binary time series show that the STE algorithm generally outperforms all the other cost functions considered.

Ali Khakpour *et al* [2021] [14] have proposed a timing errors and especially the timing skew mismatch errors are one of the main errors that cause substantial degradation in the resolution of high-speed Time-Interleaved analog-to-digital converters (TIADCs). These errors cannot be completely corrected using blind methods such as ANC, BSS etc., because of the correlation between the desired signal and the noise as both are sampled from the same input signal. In this paper, a new algorithm using oversampling is suggested to guarantee independence between the signal and the noise. The compensation structure is a typical Adaptive Noise Cancelling (ANC) block which uses special cost function gained from the oversampling concept. Low computational complexity and fast convergence speed are the main advantages of this algorithm.

Kuo Liu *et al* [2022] [15] have presented a challenging issue to predict the thermal-induced time-varying error for the movement axis of the

computer numerical control (CNC) machine tool. Subsequently, it is a challenge to predict the machining accuracy for a certain work piece when the machine tool and numerical control (NC) program are determined. The framework of time-varying error prediction and compensation for the CNC machine tool's movement axis was proposed based on the digital twin concept, which includes the physical entity layer, data transmission layer, function execution layer and application service layer.

3 PROPOSED WORK

Drastic device shrinking, increased complexity, power consumption reduction, and increasing operating speed that accompany the technological evolution to nanometer technologies have reduced the reliability of submicrometer ICs. A significant problem is related to soft errors induced by alpha particles and by neutrons created by the interaction of cosmic rays with the earth atmosphere. A more recent technique approximates parts of logical functions identified as more vulnerable to soft errors and uses the results to mask an error. Thus, it makes a trade-off between fault coverage and area overhead. Recently, a solution that combines error detection and error masking where also proposed. Although this solution is claimed to have better performance in terms of error correction than TMR, it affects negatively the clock frequency and has a greater hardware overhead than DMR. Figure 1 presents the block diagram of the proposed work.

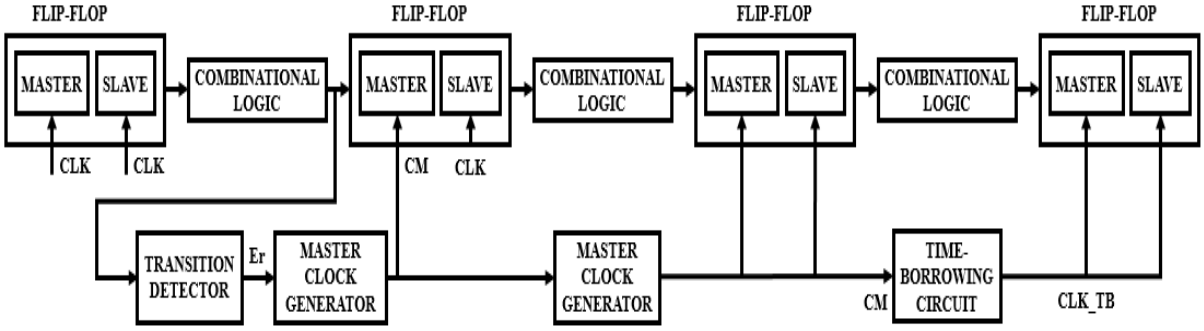


Figure1 Block diagram for proposed system

In this paper, a timing-error-tolerant technique is proposed that, via a simple process, may rapidly resolve a timing error. Controlling the clock's transparent window allows the critical path to detect and fix the timing error-induced irregular data transition that occurs after the rising edge of the clock. A small amount of logics directly corrects the timing error. Additionally, it introduce time borrowing strategy, which corrects for further errors. Any site with a quick flip-flop setup time can use the time-borrowing technique. The arranged CLK in the second stage keeps a transparent window open for long enough to allow regular data to be saved without modifying the system CLK if the timing error happens in two stages sequentially.

3.1 Flip Flop

A Flip Flop is a memory element that can hold one bit of information. It is also known as a Bistable Multivibrator because it has two stable states: 0 and 1. A flip-flop is a binary bit storage device with two states; one of its two states represents "1" and the other represents "0." This type of data storage is used to save states, and the corresponding circuit is known as "sequential logic". In electronics, flip-flops and latches are circuits that have two stable states that can store state information a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will output its state (often along with its logical complement too).

3.2 Master Slave Flip Flop

A master-slave flip flop is made by connecting two JK flip flops in a series configuration in which one acts as the master and another as a slave. The two inputs of slave are connected with the output of the master flip flop. Furthermore, the master flip flop inputs are fed back by the output of the slave flip flop.

3.2.1 Master Slave FF Working

Whenever the CLK pulse goes to high which means 1, then the slave can be separated; the inputs like J & K may change the condition of the system. The slave FF can be is detached until the CLK pulse goes to low which means to 0.

3.2.1.1 Timing Diagram

When both the CLK pulse & o/p of the master is high, then it remains high until the CLK is low due to the state is stored. At the present, the master's o/p turn into low as the CLK pulse turn into high once

more & remains become low till the CLK turn into high once more. Therefore toggling takes place for a CLK cycle.

3.3 Combinational Logic Circuits

Combinational logic circuits are those that contain various types of logic gates. A combinational logic circuit is simply a circuit that combines different types of logic gates. The combinational circuit's output is determined by the current combination of inputs, regardless of the previous input. The basic components of a combinational logic circuit are input variables, logic gates, and output variables.

3.4 Time Borrowing Circuit

Time borrowing is a technique that allows a longer path to borrow time from the next path of subsequent logic. Time borrowing typically has an impact on the setup because it slows the data arrival time, resulting in a longer data arrival time. The time borrowed by the latch from the next stage in the pipeline is then subtracted from the time of the next path.

3.4.1 Time Borowing Limitations

Time borrowing optimization, which occurs in the Fitter (Finalize) stage, cannot occur for the following registers. If any such registers are on the critical timing path, you can possibly report better performance by enabling Dynamic time borrowing mode, which reports time borrowing for all borrow-capable registers.

3.5 Master Clock Generator

A Master Clock Generator is the device that sends the clock signal to the synchronisation device(s). The master clock generator is an extremely stable oscillator that supplies external clocks to digital devices equipped with clock input terminals. It take one or more precise timing reference signals as inputs, then convert and distribute those timing references to other devices to improve their accuracy. Master clock systems are used in a variety of applications and industries, including: Aerospace. Defense.

3.6 Transition Detector

In flip flops, a transition detector is used to achieve edge triggering in the circuit. It simply converts the rising edge of the clock signal to a very narrow pulse.

It consists of a delay gate and the clock signal itself, which is inverted after passing through a NAND gate. The advantage of edge triggering is that it eliminates the problems associated with zero and one catching in pulse triggered flipflops (e.g. master slave flip flops).

4 RESULTS AND DISCUSSION

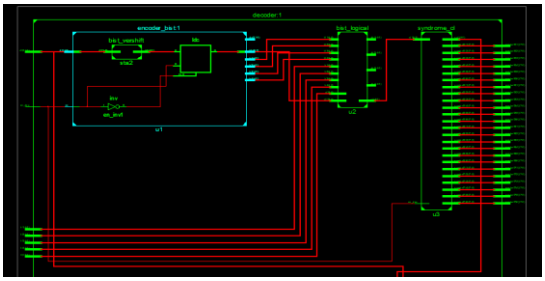


Figure 2 Timing Error Tolerant Circuit

Figure 2 represents the timing error tolerant circuit a timing-error-tolerant aggressive design method to design the individual components of the NoC (such as switches, links, and network interfaces), so that the communication subsubsystem can be clocked at a much higher frequency than a traditional conservative design (up to 1.5× increase in frequency). The NoC is designed to tolerate timing errors that arise from overclocking without substantially affecting the latency for communication.

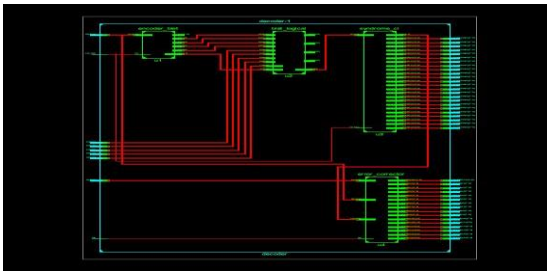
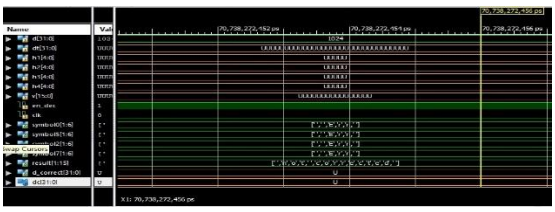


Figure 3 Schematic of Time Borrow Circuit

Figure 3 signifies that time borrow circuit is a longer path takes to borrow the time from the next path of subsequent logic. Time borrowing typically affects the setup since time borrowing is slowing the data arrival time i.e. data arrival time is more. It does not affect the hold time because in hold time data arrival time is more.



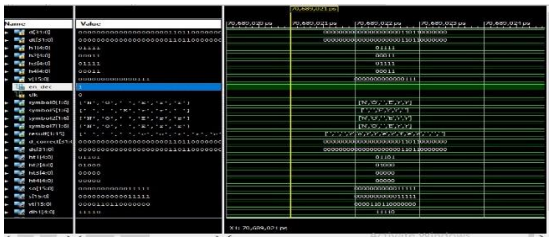


Figure 4 Simulation Results

5 CONCLUSION

This paper suggested a timing error-tolerant method that can correct a timing error immediately with a compact circuit structure. An effective method to detect and correct timing errors using a timing error-tolerant circuit, and time borrowing is used in tolerant circuit's technique. Controlling the transparent window of the clock enables the critical path to detect and correct the timing error-induced irregular data transition that occurs after the clock's rising edge. The timing error is directly corrected by a small amount of logic. It also introduces a time borrowing strategy, which corrects for future errors. The time-borrowing technique can be used at any site that has a quick flip-flop setup time. If the timing error occurs in two stages sequentially, the arranged CLK in the second stage keeps a transparent window open long enough to allow regular data to be saved without modifying the system CLK. The timing error is corrected directly through a minimum number of logics. This paper succeeded in evaluating the system's effectiveness and quickly fixing a timing error in a clock-based system.

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