Implementation of Polar Codes Using Verilog HDL for 5G Applications

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Abstract:-**This paper proposes Very Large Scale Integration (VLSI) architecture for the implementation of Polar decoder. Soft-in-soft out decoders, interleavers and deinterleavers is used in the decoder side which employs Maximum-a- Posteriori (MAP) algorithm. The number of iterations required to decode the information bits being transmitted is reduced by the use of MAP algorithm. For the encoder part, this project uses a system which contains two Recursive convolutional encoders along with pseudorandom interleaver in encoder side. Beyond-5G systems are expected to operate at Terabit/s data rates. Today's most advanced polar code implementations currently deliver only around 5Gbps. Therefore, Turbo codes and LDPC codes that played key enablers in 3G and 4G systems are already unproven for many new 5G applications. Polar code is believed as prominent breakthrough in 5G. It guarantees apical performance for 5G scenarios and hence it is considered as a promising candidate for the 5G New Radio. This work accentuates on the suitability of polar codes for the 5G scenarios.**

Key words:-Polar codes, MAP, VLSI

I. INTRODUCTION

Polar codes were introduced by Erdal Arıkan in 2008. They are the first family of error-correcting codes that attain the capacity of binary-input memoryless and symmetric channels with efficient encoding, decoding, and construction algorithms. Since their introduction, polar codes have been generalized and shown to be capacity achieving in numerous other communications settings.

The original construction of polar codes relies on the recursive application of an invertible linear transformation, which, when combined with a successive-cancellation decoder, effectively splits the original binary-input memoryless and symmetric communication channel into a number of bit subchannels. Increasing the recursion depth causes these bit subchannels to converge either to noiseless or purely noisy channels. Virtually error-free transmission can be achieved by sending the data over noiseless subchannels. While related code constructions had been suggested before (e.g., N. Stolte, I. Dumer and K. Shabunov), Arıkan's work was the first to prove the polarization phenomenon and thus prove that polar codes are capacity achieving.

Unfortunately, the subchannels converge to these limiting cases relatively slowly, meaning that the error-correcting performance of Arıkan's polar codes improves more slowly with the blocklength than other widely-used codes, such as Turbo and LDPC codes. However, polar codes have been shown to provide excellent error-correcting performance with low decoding complexity for practical blocklengths when combined with more advanced decoding algorithms. These favorable traits have led to polar codes being used in the 5G wireless standard, which is a testament to their outstanding performance.

In this Best Readings, we summarize several papers on the theoretical foundations of polarization theory, the construction and decoding of practical polar codes, as well as some generalized polar codes, which can help to overcome limitations of classical Arıkan polar codes. We also focus on practical implementation issues because, despite the simple structure of the encoding and decoding algorithms of polar codes, their practical implementation poses numerous challenges. Polar codes [1] are constructed from the generator matrix $G \otimes M$ 2 with G2 = [1 1 0 1] , where $\otimes M$ denotes the Mth Kronecker power. It has been shown in [1], that the synthesized channels seen by individual bits approach two extremes, either a noiseless channel or a pure-noise channel, as the block length N = 2M grows large. The fraction of noiseless

channels is close to the channel capacity. Therefore, the noiseless channels, termed unfrozen bit channels, are selected for transmitting message bits while the other channels, termed frozen bit channels, are set to fixed values known by both encoder and decoder. Therefore, polar codes are the first family of codes that achieve the capacity of symmetric binary-input discrete memoryless channels under a lowcomplexity successive cancellation (SC) decoding algorithm as the block length N approaches infinity. However, the performance of polar codes at short to moderate block lengths is disappointing under the SC decoding algorithm. Later, a successive cancellation list (SCL) decoding algorithm for polar codes was proposed [2], which approaches the performance of the maximum-likelihood (ML) decoder as the list size L is large. However, the performance levels of polar codes are still inferior to those of low-density parity-check (LDPC) codes even under the ML decoder. To strengthen polar codes, a serial concatenation of a cyclic redundancy check (CRC) code and a polar code, termed the CRC-aided polar code, was found to be effective to improve the performance under the SCL decoding algorithm [2]. The performance levels of CRC-aided polar codes under the SCL decoding algorithm are better than those of LDPC and turbo codes [2], [3]. As the SCL decoder is capable to achieve the ML performance, it is important to study the block error rate (BLER) of polar codes under the ML decoder. However, in the literature, there are no analytical results regarding the ML performance of polar codes. The BLERs of polar codes rely on simulations that are time-consuming. A possible way to analyze the BLER performance of a coding scheme is to use the BLER upper bound which is a function of the weight enumerating function (WEF) as that used to analyze turbo codes [4]. However, if the code size is large, obtaining the exact WEF of a polar code with the heuristic method is prohibitively complex. Approximations of WEFs of polar codes are proposed in [5], [6] based on the probabilistic weight distribution (PWD) [7]. In this paper, we propose to randomize the polar code using interleavers between the inter-3 mediate stages of the polar code encoder. Codes constructed on the basis of this idea are called interleaved polar (i-polar) codes. The ensemble of i-polar codes is formed by considering all possible interleavers. The regular polar code is just one realization of the ensemble of i-polar codes. Based on the concept of uniform interleaver, i.e., all interleavers are selected uniformly at random from all possible permutations, the average WEF of a code selected at random from the ensemble of i-polar codes can be evaluated. The concept of uniform interleaver has also been used in the analysis of turbo codes [4]. Note that the WEF analysis in this paper is not an approximation to the WEF of a polar code, but is an exact WEF averaged over the ensemble of i-polar codes. Based on the average WEF, a BLER upper bound, termed simple bound [8], can be used to evaluate the BLER performance averaged over the ensemble of codes. Simulation results show that the BLER upper bounds can well predict the ML performance levels of i-polar codes at high SNRs. Also, we will show by simulations that a specific realization of i-polar codes outperforms a regular polar code under the SCL decoder of the same list size. We also propose a concatenated coding scheme that employs P identical high rate codes as the outer code and Q identical i-polar codes as the inner code with an interleaver in between. CRC codes are the most popular outer codes employed in the concatenation of polar codes.

We propose as an alternative to use systematic regular repeat-accumulate (RRA) codes or irregular repeataccumulate (IRA) codes [9] as the outer component code. The average WEF of the concatenated code is derived based on the uniform interleaver assumption. Simulation results show that the BLER upper bounds can well predict the BLER performance levels of the concatenated codes. One advantage of the proposed concatenated code is that, for $Q > 1$, the code can be decoded using Q SCL decoders working in parallel which can significantly reduce the decoding latency when Q is large. Analytical and simulation results both show that the performance of the proposed concatenated code with $P = Q = 2$ is better than that of the CRC-aided i-polar code with $P = Q = 1$ of the same length and code rate at high SNRs. Therefore, the proposed coding scheme is suitable for ultra-reliable low-latency communications (URLLC) [10]. Polar codes are error-correcting codes, which are able to achieve the capacity of binary-input memory less symmetric (BMS) channels. This means that one can transmit at the highest possible rate over that class of channels. In addition, the encoding and decoding operations can be performed with low complexity, thanks to recursive techniques.

II ARCHITECTURE OF POLAR CODER

Polar encoder and decoder together comprises the Polar coder architecture shown in Figure 1

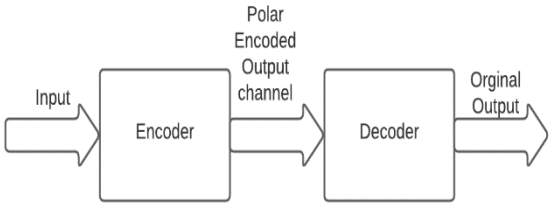


Figure 1-POLAR CODER BLOCK DIAGRAM

Two identical Recursive convolutional encoders (RSC) and a pseudorandom interleaver constitutes the polar encoder.LTE employs a 1/3 rate parallel concatenated polar code. Each RSC works on two different data. Original data is provided to the first encoder, while the second encoder receives the interleaved version of the input data. A specified algorithm is used to scramble the data bits and the method is called Interleaving. An appreciable impact on the performance of a decoder is seen with the interleaving algorithm when used. The RSC1 and RSC2 encoder outputs along with systematic input comprises the output of polar encoder, that is, a 24-bit output is generated which is illustrated in figure 2. This will be transmitted through the channel to the Polar decoder.

A standard polar decoder block diagram is shown in Figure 3that contains two modules of SISO decoders together with two pseudorandom interleavers and a pseudorandom de-interleaver. The usually used method of polar code decoding is carried out using the BCJR algorithm. The fundamental and basic idea behind the polar decoding algorithm is the iteration between the two SISO part decoders which is illustrated in figure 3.4.

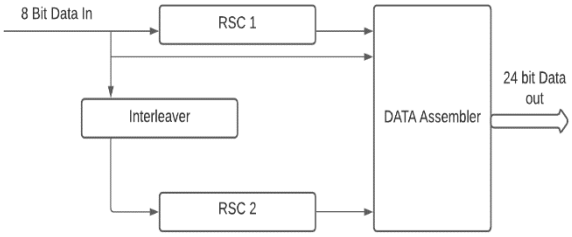


Figure 2POLAR ENCODER BLOCK DIAGRAM

It comprises a pair of decoders, those which work simultaneously in order to refine and upgrade the estimate of the original information bits. The first and second SISO decoder, respectively, decodes the convolutional code generated by the first or second CE. A polar-iteration corresponds to one pass of the first component decoder which is followed by a pass of the second component decoder.

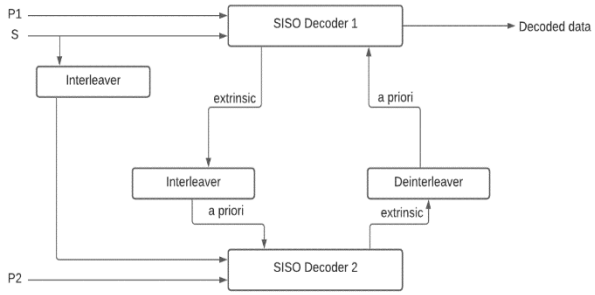
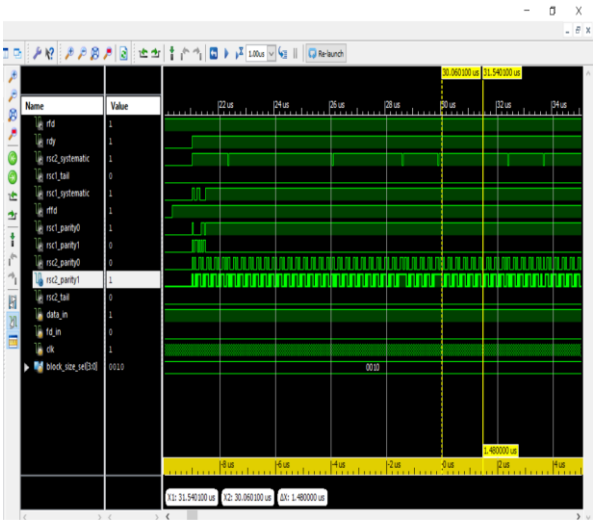


Figure 3. Polar Decoder Block diagram

III RESULTS AND DISCUSSIONS

For Encoder

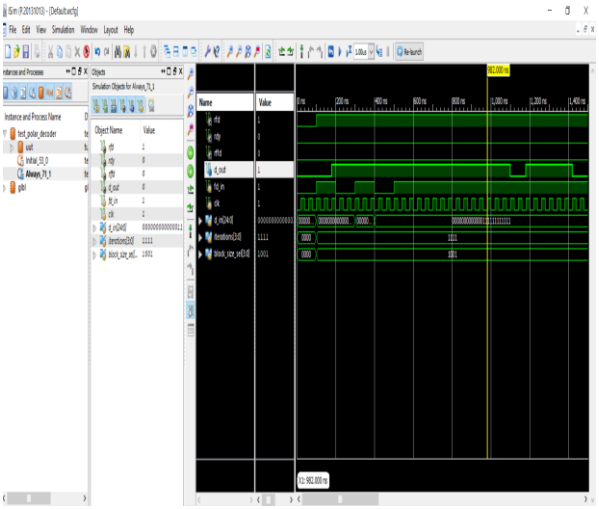
Here the data_in 1010011 and fd_in 1010100 is transmitted for every 100µ seconds and the block size is 0010



We can observe the block size 0010 and data_in 1 and d_in 0 is transmitted and the transition occurred at posedge of clock.

For Decoder

Here the block size is 1001 and fd_in 10101 and d_in 11111 is transmitted for the given iterations for every 100µ seconds.



IV CONCLUSION

The polar encoder and decoder designs are done using Verilog HDL and simulation has done in Xilinx ISE13.2. The RTL and Technology schematics have observed in XILINX. Synthesis repost has shown the details of our proposed design. This example highlights one of the polar coding schemes (CRC-Aided Polar) specified by 3GPP for New Radio control channel information (DCI, UCI) and broadcast channel (BCH). It shows the use of components for all stages of the processing (encoding, rate-matching, rate-recovery and decoding) and uses them in a link with QPSK over an AWGN channel. Highlighted performance results for different code rates and message lengths show agreement to published trends, within parametric and simulation assumption.

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