Impact of Power Minimisation Techniques for Testing Low-Power VLSI Circuit

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Abstract: Power consumption in chips has grown as a side effect of technological progress. In the absence of targeted countermeasures, test-time power usage and fluctuations would be much higher. To guarantee the high quality of the final product, VLSI testing comprises the whole range of testing techniques and infrastructures that are built into a system-on-chip. The study focuses on the Impact of Power Minimisation Techniques for Testing Low Power VLSI Circuits. The study also focuses on Methods for Power Minimization in Modern VLSI Circuits. In addition, the study highlights strategies and challenges for low-power VLSI designs. Methods for testing sometimes include failure modeling and test development to ensure each device receives enough test patterns. Furthermore, the study examines Leakage Power Reduction in CMOS VLSI Circuits. Lastly, Power Minimisation Techniques for Testing Low Power VLSI Circuits are the main focus of the study.

Keywords: Low-Power VLSI Circuits, Power Minimisation Techniques

1. INTRODUCTION

VLSI, or very large-scale integration, is the technique by which an IC is created by placing millions or billions of MOS transistors on a single chip. Early examples of very large-scale integration (VLSI) appeared in the 1970s, with the widespread use of MOS (Metal Oxide Semiconductor) chips. This made it possible to make complex semiconductor and communication technologies (Ansari, 2019). Process technologies in the field of complementary metal-oxide semiconductors (CMOS) work hard to keep up with Moore's law, which states that the computing capability of a chip doubles about every 18 months. Despite the many positive outcomes associated with rising levels of integration, public opinion towards inappropriate conduct is shifting. CMOS integrated circuits, the most common manufacturing process for realizing very large-scale integrated circuits (VLSI; those with more than 105 transistors), have their design and testing flow introduced here (Nicolisi, 2000).

The specification, implementation, and manufacturing phases make up the design flow of VLSI circuits. The functionality of the VLSI circuit is described during the specification stage. Specifications are written in HDLs like VHDL and Verilog, and they can be done at several levels of abstraction in either the behavioral domain or the structural domain (Saritha, 2022).

For instance, in the behavioral domain, logic is represented by Boolean algebra expressions, and in the structural domain via the interconnection of logic gates. By using a higher degree of abstraction, we can reach the register-transfer level. The register-transfer level (RTL) of the VLSI design cycle characterizes an integrated circuit (IC) as sequential logic, consisting of registers and functional units that calculate the future state depending on the present state of the memory. The abstract functioning of a system is best described at the algorithmic level, the highest degree of specification (Garg, 2018).

Methods for Power Minimization in Modern VLSI Circuits

According to Yan, (2018) more systems on a chip mean more transistors, which means more power is being dissipated by the devices. Longer battery life, particularly in portable devices, and greater dependability are two hallmarks of low-power design. There are four distinct categories of power consumption in VLSI devices: dynamic, static, leakage, and static power consumption. Time-tested methods include clock gating, power gating, varying the frequency or amount of power supplied, and adjusting the threshold at which a device is considered to be functional. However, several cutting-edge methods, including dynamic power reduction, leaky power reduction, reverse biasing, and others, have also been implemented.

Low Power Design

Maiti, (2020) analyzed that the biggest obstacle to portability is battery life. There is a greater need than ever before for improved functionality and longer run times. More than two-thirds of the world's

population thinks that increased standby time should be a main mobile phone feature. Concerns about the environment, battery life, digital noise immunity, packaging cost, and cooling cost all play a role in the importance of power in SOC.

Table 1: Power Reduction Techniques

Traditional Techniques	Dynamic Power Reduction	Leakage Power Reduction	Other Power Reduction Technique
Clock gating	Clock gating	Minimize usage of V_T cells	Minimize oxide devices
Variable frequency	Variable frequency	Back biasing	Power efficient circuit
Variable voltage supply	Variable voltage supply	Reduce oxide thickness	
Variable device threshold	Variable island	Use FET	

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Traditional Low-Power Techniques

Clock Gating

According to Hills, (2019) this method is widely utilized because of its effectiveness in lowering the heat generated by dynamic processes. When a clock gating method is used, additional logic gates are added to the circuit to shave down the clock tree. Some circuitry that could cause a flip-flop to be toggled due to parity is disabled by the clock. In latch-based clock gating, the enabled signal is held away from the clock's active edge using a level-sensitive latch until the entire clock pulse has been created. The latch-free clock gating design makes use of the AND and OR gates. The gate clock may create several clock pulses or end prematurely if the enabled signal becomes passive between clock pulses.

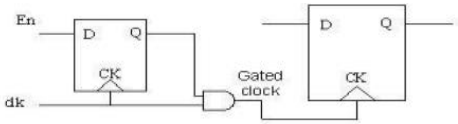

Figure 1: Latched based clock gating

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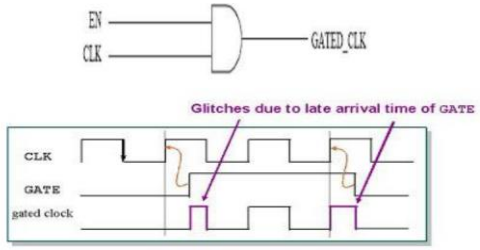

Figure 2: Latch free clock gating

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Variable Frequency

Cao, (2018) stated that a VFD, or variable frequency drive, is a changeable frequency device. It regulates AC motor speed and torque in electromechanical drive systems. This has been accomplished by altering the power supply to the motors. This input may be a frequency or voltage. Since motors account for roughly 25% of industrial electrical energy consumption, VFDs are widely utilized in everything from household appliances to compressors. Many motor applications that rely on AC line power may reduce their energy consumption by switching to variable speed operation with the help of a variable frequency drive (VFD). Power reduction and improved control performance are two of the most prominent advantages of variable frequency drives (VFD).

Variable Voltage Supply

Piguet, (2018) pointed out that in contrast to fixed voltage power supplies, which provide the same dc voltage at all outputs, a standard variable voltage supplier consists of a three-terminal positive voltage regulator.

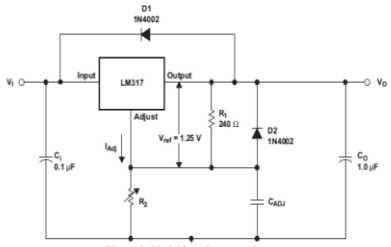

Figure 3: Variable voltage regulators

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Variable Device Threshold

Ascione, (2019) analyzed that the substrate bias is regulated to maintain a constant threshold voltage. Device simulation has been used to examine the properties of changing threshold voltage. The threshold voltage may be lowered to enhance the driving current and mitigate the deterioration caused by the series connection. Figure 4 shows how increasing the body-biased voltage raises the threshold voltage of both devices and lowers the sub-threshold value in standby mode.

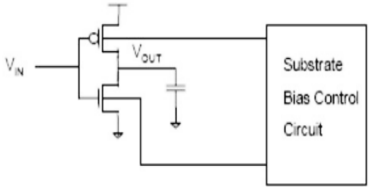

Figure 4: Variable Threshold

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Dynamic Power Reduction

Many, (2018) pointed out that there are three primary categories of power consumption in CMOS: static power, dynamic power, and leakage current. The equation for the power in motion is:

P=ACV2 F

Kheiri, (2018) pointed out that the energy used to charge and discharge a capacitor is known as its dynamic power consumption. Most opportunities to reduce power dissipation can be managed at the design stage. Unused components are powered off by a mix of software and hardware mechanisms. To successfully decrease the leakage current, it is best to do so at the circuit and process levels.

Clock Gating

According to Tahersima, (2019) primarily, it finds use in sequential circuits where a lowering in dynamic power consumption is desired. Clock gating's core idea is to minimize the need for the clock signals that flip flops need to switch. Clock gating eliminates or prevents extra clock switching of the adders during clock cycles. In extreme cases, clock buffering might waste as much as 50% of the dynamic power being used. This is because clock buffers are used more often in a system due to the faster toggle rate and because they reduce clock latency.

Power Efficient Technique

Mirhoseini, (2020) analyzed that reducing power loss is one way to improve energy efficiency. If the savings from using less energy are enough to cover the increased expenses associated with switching to more efficient equipment, then customers will come out ahead. Renewable energy and energy efficiency are the cornerstones of a reliable and long-lasting power grid. The power may be analyzed at the circuit and gate levels. There are several approaches for low power.

Adiabatic Circuits

Amano, (2018) pointed out that an adiabatic circuit does not lose energy but rather recycles it. This is accomplished by putting limits on the form and duration of the signal's transition energy. There is no need to include diodes in the design of adiabatic circuits due to their invisibility from a thermodynamic perspective.

Logic Design of Low Power

According to Graser, (2018) power dissipation accounts for around 10% of the overall power usage in a static CMOS circuit. Power dissipation is not an issue in dynamic circuits since there is no direct dc supply to the ground; but, in domino-logic circuits, there is a direct channel from the supply voltage to the ground, which may lead to a short circuit.

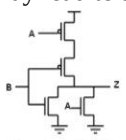

Figure 5: Static NOR

Z can only be pulled up id A=B=0V

Z can be pulled down by either A=1 or B=1 (or both)

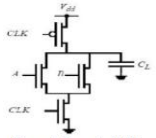

Figure 6: Dynamic NOR

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Leakage Power Reduction

Marchetti, (2019) pointed out that minimizing power loss due to leakage has become a significant challenge for on-chip devices. The leakage current and power dissipation both increase when the threshold voltage current decreases. Underthreshold leakage current is defined as the drain-to-source current of a transistor in the weak inversion region. Leakage current below the threshold and its dependence on device settings.

Table 2: Subthreshold Leakage Current

PARAMETERS	DEPENDENCE
Temperature (T)	Exponential increase
Transistor length (L)	Inversely proportional
Transistor width (W)	Directly proportional
Input voltage (V_{gs})	Exponential increase
Transistor threshold voltage (V_{th})	Increase by the order of magnitude with 100mv decrease

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Use of Low Vt Cell and High Vt Cell

Chen, (2018) analyzed that multiple Vt devices are utilized to reduce power consumption without sacrificing performance. To minimize leakage

current, high Vt is applied to gates whereas low Vt devices are employed for building high-speed circuit paths. Because it does not need a shift in SOC architecture, the multiple threshold approach has been given considerable thought. Instead, it relies on the designer's astute use of low Vt cells. As can be seen in fig.7, high Vt cells have high timing but low leakage current, whereas low Vt cells have high timing but low leakage current. Because of their superior timing capabilities, high Vt cells are deployed in less-urgent settings, whereas those with inferior Vt are deployed in mission-critical environments.

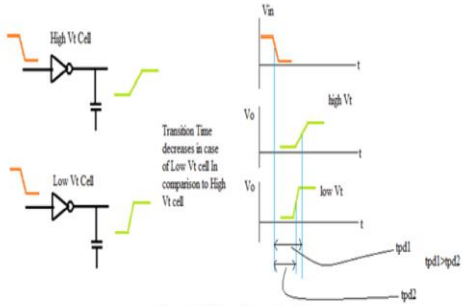

Figure 7: High and Low V_t cell

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Back Biasing

According to Bajaj, (2020) the biased voltage is generated using this technique. Whether the amplifier is solid-state or tube-based, this technique is utilized to conveniently provide a negative biased supply for the power stage. Substrate biasing is a synonym for back biasing. Increases in transistor threshold are achieved by applying a bias to the substrate, a method made possible by technological advancements. Leakage is reduced as a result. The body of the transistor is biased to a voltage greater than Vdd in PMOS. The NMOS configuration uses a body bias voltage that is less than Vss for the transistor.

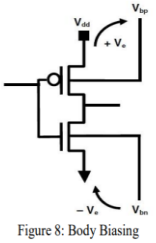
Figure 8: Body Biasing

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2.STRATEGIES & METHODOLOGIES FOR LOW POWER VLSI DESIGNS

According to Kalavathi Devi, (2021) to maximize their usefulness, low-power components and low-power design approaches should be used together. Smaller, more battery-operated components with higher performance requirements mean that power consumption must be drastically cut. For VLSI designers, area, performance, and affordability used to be top priorities. We were secondarily concerned about power. Due to the rapid development of portable computing devices and wireless communication systems, which need fast processing and sophisticated features with minimal power consumption, energy consumption has become a pressing issue. Different applications have different reasons for wanting to cut power usage. With micro-powered battery-operated portable applications like mobile phones, it is important to balance the need for a long battery life with the constraints imposed by their small size and cheap cost of packaging. Suguna, (2018) the objective for high-performance portable computers like laptops should be to lower the electronics' share of the system's overall power dissipation to below 50 percent. When it comes to high-performance, non-battery-operated systems like workstations, reducing power consumption has one overall goal: reducing system cost without compromising long-term device reliability. Recent developments in process technology have elevated the significance of power in the design of such high-performance systems. At manufacturing nodes below 100 nm technology, the power management has become more difficult due to both switching activity and leakage power consumption. Tang, (2020) pointed out that over the last decade, several methods have been developed in response to the increasingly stringent demands of the high-performance sector to reduce power consumption. Clock gating to limit dynamic power consumption and multiple voltage thresholds (multi-Vt) to limit leakage current are two well-known and supported low-power design techniques.

Power Dissipation Basics

Goel, (2020) pointed out that dynamic power, short-circuit power, and static power are the three forms of power dissipation in a circuit. Power lost during the charging and discharging of capacitors makes up the bulk of the dynamic power, also called switching power.

$$Pdyn = CL\ Vdd2\ \alpha\ f$$

According to Venkateswarlu, (2019) where CL is the load capacitance, which varies with fan-out, wire length, and transistor size; Vdd is the supply voltage, which drops at each new process node; describes the average frequency with which the wires switch; and f is the clock frequency, which increases as the number of process nodes increases. The switching threshold voltage (Vt), the transistor size, and the supply voltage all affect the static power or leakage power. Leakage consumes at least 30% of overall power, and that number rises as process nodes become smaller. The leakage power dissipation is augmented by crowbar currents produced by turning on both PMOS and NMOS devices at once. Meinerzhagen, (2018) pointed out that most methods for minimizing the size of a circuit ignore gate leakage while concentrating on minimizing the consequences of subthreshold leakage. For this purpose, an MTCMOS system has been developed to decrease leakage current below the threshold during sleep.

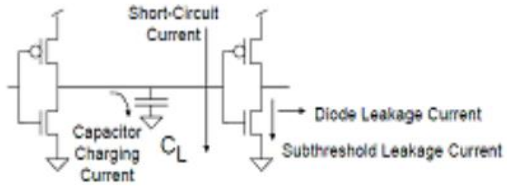

Figure 2, Power Dissipation in CMOS [4]

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Low Power Design Space

Voltage

According to Aghaei, (2019) the most efficient strategy for lowering power usage is lowering the voltage, which has a quadratic connection to power. By halving the supply voltage, power usage drops by a factor of four without the need for any additional circuitry or technology. Unfortunately, when Vdd gets closer to the threshold voltage Vt of the device, delays dramatically rise, and there is a speed penalty for reducing the supply voltage. Saritha, (2018) stated that changing the threshold voltage of the devices is one method to lower the supply voltage without sacrificing throughput. Vt scaling enables the supply voltage to be reduced without performance degradation. The need to regulate the rise in subthreshold leakage current and provide sufficient noise margins restricts how low Vt can go.

Physical Capacitance

Lue, (2019) analyzed that depending linearly on the physical capacitance being swapped, dynamic power consumption is determined. Therefore, limiting capacitances provides another method for reducing power consumption, while running at low voltages. Reducing capacitances requires utilizing less logic, smaller devices, and fewer and shorter connections. The optimization of capacitances is not as free as that of voltage; for instance, shrinking device sizes decrease the physical capacitance, but it also shrinks the current drive to the transistor, slowing down the circuit in operation.

Switching Activity

Shanmuganathan, (2019) pointed out that the frequency of data arrivals, or Folk, and the number of transitions, or E(SW), are the two components of switching activity. By optimizing the design of the algorithm, the logic topology, and the logic level, E(SW) may be lowered, using less power overall. Switch capacitance Csw=C is the result of adding the data activity E(SW) to the physical capacitance C. A CMOS circuit has a power consumption that is proportional to the quotient of its average capacitance charge, or E(SW), over the course of each data period or 1/Fclk.

The Role of Technology Selection

Macko, (2018) stated that one of the most important parts of managing electricity is choosing the right technology. Each technological improvement is supposed to boost functionality, density, and efficiency. Applying constant-electric-field scaling is the norm while creating new generations of technology. As the oxide thickness is increased, the applied voltage must be decreased to maintain the same electric field, and vice versa. With each incremental advancement in technology, this method may cut power use by half. However, the threshold voltage must likewise scale down as the voltage decreases if the technique is to achieve its performance goals. The leakage power and the subthreshold current both rise as a result of this scaling. As a result of this limitation, process engineers have begun to use a more generalized type of scaling for processes of 65 nm or less, instead of the previously employed constant-field scaling. Sharifi, (2018) pointed out that due to the impossibility of simultaneously optimizing a technology's performance and leakage, there are often two variations for any technology. The first

type is optimized for speed, while the second prioritizes efficiency. Both kinds are distinct from one another in the oxide thickness, supply voltage, and threshold voltage. Low-leakage designs, which need the thicker gate oxide technology type, require higher operating voltages. Considerations such as the requirement for a smaller geometry and a low-leakage variation must be made when selecting a technology to maximize the power for a certain design.

Figure 3: Technology selection for [9] effective power management

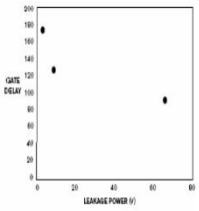

Figure4: Trade off between leakage and Power

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Circuit-Design Techniques

According to Touil, (2020) once a technology has been chosen, the next step is to concentrate on efficient design methods. The first step is to choose the right logic gate from the collection of standard cells. For each gate in a conventional cell library, we employ the smallest transistors possible to create numerous variants that vary in drive intensity, gate size, delay, voltage threshold, and power usage. Designers of cells often create and define gates that can work at voltages up to 30% lower than the power-supply voltage, since this is the primary parameter for regulating active power. When the voltage from the power source is reduced, the current flows more slowly. Naseri, (2018) pointed out that however if the design is not straining the limits of a certain technology, the sluggishness may be tolerated. An increase in the threshold voltage decreases the leakage current in the component. Logic gates may be designed with several thresholds voltage devices, such as the regular high and low threshold voltage devices, to limit the amount of power they leak.

Low Power management in Physical Design

Tao, (2018) pointed out that despite the inclusion of many corners, modes, and power states, as well as manufacturing unpredictability, physical design tools were able to efficiently implement the architecture, from the placement of unique cells to the routing and optimization across power domains. Creating multiple voltage islands (domains) is a typical practice in physical design for reducing power consumption by allowing various blocks to use different supply voltages or be turned off altogether for different modes of operation. The clock is a major variable power consumer. Energy efficiency may be increased by the use of low-power clock tree synthesis (CTS) techniques such as reducing the total capacitance and limiting switching activity. Khursheed, (2019) analyzed that attaining peak power performance from CTS requires a method that can synthesize the clocks for several corners and modes concurrently in the face of design and manufacturing uncertainties as well as multi-voltage flows. Power gating, which involves briefly shutting off the circuit, is an efficient method for minimizing leakage power. This period of inactivity, often known as "low power mode" or "inactive mode" is necessary to save energy. Turning circuit elements back on to "active mode" is what is done when they are needed again in the circuit in operation. The blocks may be turned off in two ways: software and hardware. This task is often handled by a specialized power management controller these days.

Table-3 Trade off associated with power management techniques.

Power Reduction Technique	Power Benefit	Timing Penalty	Area Penalty	Methodology Impact			
				Architecture	Design	Verification	Implementation
Multi Vt optimization	Medium	Little	Little	Low	Low	None	Low
Clock Gating	Medium	Little	Little	Low	Low	None	Low
Multi supply voltage	Large	Some	Little	High	Medium	Low	Medium
Power Shut off	Huge	Some	Some	High	High	High	High
Dynamic and adaptive voltage frequency scaling	Large	Some	Some	High	High	High	High
Substrate Biasing	Large	Some	Some	Medium	None	None	High

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Many industries are driving the demand for low-power technologies. The design must be optimized not just for Performance and Area, but also for power, which is a major hassle given the already difficult design problem.

Leakage Power Reduction in CMOS VLSI Circuits

According to Nandyala, (2016) growing energy requirements are a major roadblock to the improvement of digital integrated circuits. Power density has increased significantly because of higher clock rates, more thorough functional integration, and more compact manufacturing geometries. Increasing the number of transistors on a device and

increasing its functionality are both benefits of scaling. Performance may be improved as a result of scaling up operations' pace and frequency. Threshold voltages need to be reduced when voltages scale down with geometries for the new technology to provide its performance advantages. Although, leakage current increases at an exponential rate as threshold voltages drop. In the presence of less gate oxide, the leakage current through the gate has grown.

Power dissipation factors

Kumar, (2018) stated that CMOS devices can lose power due to two different types of power consumption issues: leakage power and dynamic power. Different types of dynamic power include switching power and short-circuit power. Any time a pull-up or pull-down network is turning on and off, short circuit power is being consumed, while switching power is being used anytime transistors are in active mode. Leakage power is inconsequential compared to dynamic power for larger u values; but, when u=0.13u and lower, leakage power is the dominant cause of energy consumption. The quantity of dynamic power lost is a square root of the input voltage. Lower supply and threshold voltages for MOS transistors are a result of the development of deep submicron technologies. As a result, there is a lesser loss of dynamic power.

According to Lorenzo, (2017) when no data is being transferred and the transistor is in a steady state, the power dissipated by the transistor owing to leakage currents is called static power dissipation. Power leakage occurs in proportion to gate length and oxide thickness. The threshold voltage and other factors affect it dramatically. However, in this instance, the benefits of reducing supply voltages and threshold voltages for MOS transistors, which serve to minimize dynamic power dissipation, become drawbacks. Static power dissipation rises according to the subthreshold leakage current.

Firdous, (2017) analyzed that leakage current in a transistor originates mostly from reverse-biased PN junction leakage and sub-threshold leakage. The leakage from the PN junction under reverse bias is negligible in comparison to the leakage from the subthreshold region. In the subthreshold region, also known as the weak-inversion zone, current flows between the source and drain of a MOSFET when the gate-to-source voltage is less than the threshold voltage. The term "subthreshold leakage" or "subthreshold drain current" describes this kind of current.

$$I_{sub} = I_{so}\exp\left(\frac{V_{gs}-V_{th}}{V_T}\right)\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (1)$$

$$I_{s0} = \mu_0 C_{ox}\frac{W_{eff}}{L_{eff}} V^2 e^{1.8} \quad (2)$$

Source: https://www.researchgate.net/publication/298706154_Leakage_Power_Reduction_in_CMOS_VLSI_Circuits/link/56a60d2308aeca0fddcb0db2/download

According to Thamaraimanalan, (2020) cox is the oxide capacitance per unit area, Jeff is the effective channel width, and Leff is the effective channel length; where 0 is the zero-bias electron mobility, n is the subthreshold slope coefficient, Vgs and Vds are the gate-to-source and drain-to-source voltages, VT is the thermal voltage, Vth is the threshold voltage, and VT = 0 is the threshold voltage. As Vth rises, the subthreshold current Isub drops precipitously because of the exponential relationship between the two.

Leakage current reduction

According to Vanapalli, (2016), there is an increase in the subthreshold leakage current when the threshold voltage decreases. One of the problems with scaling technologies is the rapid increase in subthreshold leakage power due to the drop in Vt. The ability to detect and implement strategies for minimizing this source of wasted energy is of paramount importance in such a setup. The increased need for electricity poses a problem for the advancement of digital integrated circuits.

Leela Rani, (2016) pointed out that for high-performance, low-power digital CMOS circuits, leakage current is a major issue. The scaling of threshold voltages necessary to assure optimal performance in active mode when supply voltages are scaled is the root cause of the exponential rise in the leakage component of the total chip power. To lessen the impact of standby leakage in digital circuits, several different design approaches have been suggested. Using power-gating has shown to be an effective solution to the growing issue of leakage power in nanoscale CMOS technology at the expense of just a little hit to performance. The battery-powered gadgets may be in one of two states: standby (idle) or active (working). These two channels allow us to classify the many types of power leakage we see. Leakage may be minimized when the device is in sleep mode with the use of

techniques like power gating and super-cutoff CMOS. During its non-use times, the circuit may be disconnected from its power supply using these ways. During the active mode or run time, leakage current may be decreased using strategies like forced stacking and sleepy stack.

Verma, (2016) analyzed that due to CMOS's ongoing miniaturization, leakage is rapidly approaching the level of dynamic switching power. Several methods have been suggested for minimizing leakage power, including operating at lower voltages (both dual-Vth and multi-Vth), selecting the best standby input vectors, stacking transistors, and applying a body bias.

Moradinezhad Maryan, (2021) stated that several thresholds may be used to address the leakage problem in low-voltage high-performance CMOS circuits. The dual-Vth assignment is an efficient strategy for decreasing leakage power. Using this technique, both a low Vth and a high Vth variant of each standard cell library cell are available. While gates with a high Vth are slower, their subthreshold leakage is drastically decreased compared to those with a low Vth. Integrated circuit manufacturers are now facing significant challenges related to power production, distribution, and dissipation. In most cases, high-complexity digital systems can no longer be designed using circuit design methodologies that just prioritize increasing circuit speed without also taking power into account.

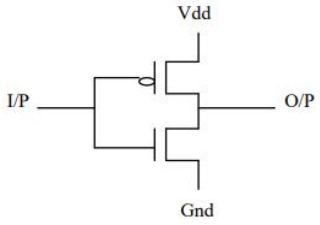

Fig 1: Base Case

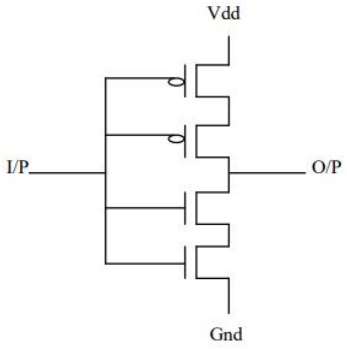

Fig 2: Forced Stack

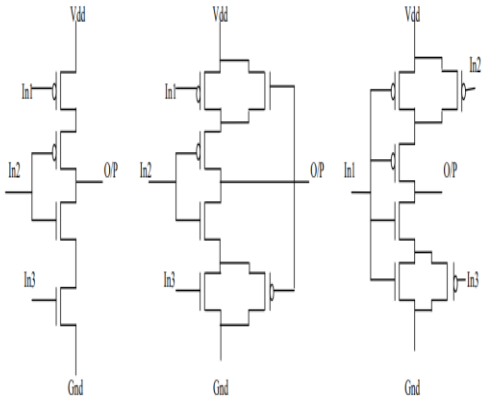

Fig 3: Sleep Transistor Fig 4: Sleepy Keeper Fig 5: Sleepy Stack

Source: https://www.researchgate.net/publication/298706154_Leakage_Power_Reduction_in_CMOS_VLSI_Circuits/link/56a60d2308aeca0fddcb0db2/download

According to Chun, (2016) stacking the transistors is another method for lowering leakage power. When two or more transistors are switched off at once, the stacking effect reduces the subthreshold leakage current. As may be seen in Figure 2, its internal organization is as follows. The stack method makes advantage of a stack effect by dividing a standard transistor in half. With the forced stack method, significant reductions in leakage power are possible while the logic state is preserved. Subthreshold leakage current is reduced due to generated reverse bias between the two transistors when they are switched off simultaneously. The forced stack inverter bypasses the high Vth (threshold) transistor.

Dadoria, (2016) analyzed that circuit optimization yields low power consumption and high performance. The performance of a circuit may be optimized by assigning a threshold voltage (Vt) and gate size at the same time. The sleep transistor method may be useful in lowering leakage power, but it irreversibly loses the transistor's state. Image 3 depicts this. When a transistor network is in a destructive state, sleep transistors are used to disconnect it from the power source or ground. Such methods are also referred to as gated Vdd and gated GND (note that a gated clock is generally used for dynamic power reduction). When the logic circuits are not being used, the sleep transistors are disabled. The sleep transistor technology drastically lowers leakage power in sleep mode by separating the logic networks using sleep transistors. When a sleep transistor is needed, a high threshold voltage is employed. Changing the threshold voltage may

decrease the amount of power used dynamically as well as leakage.

According to Garg, (2018) the sleepy keeper solution employs the usual sleep transistors in combination with two additional transistors to accomplish state saving while the system is in sleep mode. The sleepy keeper method may also use dual threshold voltages to limit leakage current below the device's threshold. Because it is common knowledge that NMOS transistors are inefficient at passing Vdd, they are usually put in the pull-down network in a conventional CMOS layout. However, since PMOS transistors are inefficient at passing GND, they are often used at the pull-up network. Figure 4 depicts the Sleepy keeper method, which differs from the conventional pull-up sleep transistor by having a single NMOS transistor connected in parallel with VDD. Since the sleep transistor is turned off during sleep mode, this NMOS transistor is the sole powering source for the pull-up circuit. In a similar vein, the sleepy keeper technique employs a PMOS transistor coupled to GND and the previously determined value of '0' to keep the output value at '0' during sleep.

Muchakayala, (2016) stated that the sleepy stack method is a hybrid of the stack and sleep methodologies. Similar to the stack method, the sleeping stack technique halves the size of the transistors already in use. Next, sleep transistors are added in parallel to one of the subdivided transistors. We can see its internal structure in Figure 5. Each network's stacking transistor and sleep transistor are engineered to operate in parallel. Specifically, the width of the sleep transistors has shrunk. Altering the transistor's width as it sleeps might result in more delays, power, and space trade-offs. Sleepy stack's sleep transistor activity is identical to that of the sleep transistor approach. Active mode triggers the sleep transistors to switch on, while sleep mode causes them to turn off. The precise logic state is preserved while very low leakage power consumption is attained because of the sleepy stack construction. The major problem of the sleeping stack method is the substantial space it adds.

Power Minimisation Techniques for Testing Low-Power VLSI Circuits

According to Saritha, (2022) Moore’s predictions about the miniaturization, complexity, and speed of integrated circuits (ICs) are being rapidly realized in today's VLSI designs. Because of the prevalence of portable, wireless, and battery-operated devices and equipment such as laptops, multimedia devices, and mobile phones, the power management has become an increasingly important consideration for product designers and quality assurance engineers. In the modern design process, testing has become a crucial step. DFT solutions must include originality and unconventional approaches. The most crucial metrics to monitor during testing are fault coverage, test count, test duration, test length, and area covered by DFT. Modern chips are designed with power dissipation, node switching, and test compression in mind. A further issue with modern high-density, high-power ICs in the deep sub-micron range is that they cause a significant drain on battery life in portable and battery-operated devices. It takes into account both typical operation and test conditions when calculating power consumption.

According to Karthick, (2017), a higher percentage of the power supply is used by the circuit under test during the testing phase. The dissipation of test power also has an impact on test throughput and the manufacturing yield. Many of the nodes in the CUT (Circuit Under Test) will flip states when the test pattern is applied. Additionally, there is a negligible amount of overlap between the two test vectors. The amount of heat produced by a CMOS circuit increases as the number of switching nodes increases. Many negative outcomes occur as a result of power dissipation, including higher test costs, worse reliability and performance, higher packaging costs, and higher costs overall. Consequently, finding ways to lessen circuit power usage during testing is an important field of study.

Lorenzo, (2017) stated that as early as the 1990s, designers were considering testability as an integral part of the development process. Prior DFT methods prioritized other metrics such as fault coverage or test application time or test duration or test quality. Most of the test cases cannot be covered by the ATPGs (Automatic Test Pattern Generators) of today, hence they only generate a small number of test patterns. There is a high rate of internal node switching caused by this test pattern. To cut down on testing time, parallel testing was used. As a result, the CUT's power dissipation is improved even more. While the DFT element utilized in an IC is idle during normal mode operation, it is active and dissipates power during the test mode. In addition to contributing to power dissipation while the CUT is in test mode, DFT also takes up a lot of room in the design. This has led to the development of power-conscious testing by designers.

VLSI Design Flow

Vanapalli, (2016) pointed out that the process technologies in the field of complementary metal-oxide semiconductors (CMOS) work hard to stay up with Moore's law, which states that the computing capability of a chip doubles about every 18 months. There are many upsides to further integration, but the public's view of problematic behavior is shifting. CMOS integrated circuits, the most common manufacturing technique for implementing very large-scale integrated circuits (VLSI) with more than 105 transistors, are introduced, along with its associated design and test procedure.

Ansari, (2019) analyzed that figure 1.1 shows the specification, implementation, and manufacturing phases of a VLSI circuit design pipeline. The purpose of the VLSI circuit is defined at this point. Specifications of the hardware are written in hardware description languages (HDLs) like VHDL and Verilog, with each HDL corresponding to a different degree of abstraction and a different design domain (either the behavioral or structural domain). The logic level of abstraction in the behavioral domain is often described using Boolean algebra expressions or the interconnection of logic gates. Register transfer is the next degree of abstraction up from the lowest level of abstraction. At the register-transfer level (RTL) of the very large-scale integration (VLSI) design cycle, an abstracted version of an integrated circuit is created; at this level, the next state is calculated using registers and functional units in conjunction with the current memory state. The abstract behavior of a system is described by a set of tasks that make up the definition of a system at the algorithmic level.

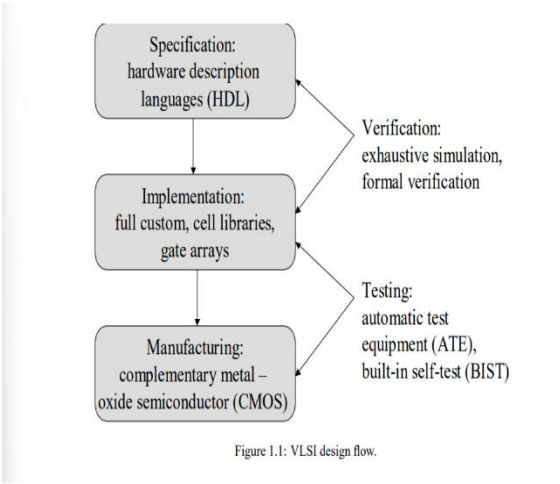

Figure 1.1: VLSI design flow.

Source:
https://eprints.soton.ac.uk/254107/1/nicola00.pdf

New Test Application Strategy for Full Scan Sequential Circuits

According to Garg, (2018) to demonstrate why a different approach to test application is necessary for power reduction, an overview of testing scan sequential circuits is provided. Input component xi and pseudo input component (current state component) yi are concatenated together to form the test vector Vi = xi@yi, which is then applied to a scan sequential circuit. Each test vector's current state component, yi, is advanced by one clock cycle, from t0 to tm1, when m scan cells are used. For the duration of the clock period t=0 t=m1, the non-scan cells in sequential circuits with partial scan do not lose their usefulness. In the next clock cycle time, the whole test vector Vi = xi@yi is applied to the under-test circuit. The scan cycle consists of m+1 clock cycles from t0 to time, during which the current state is moved into the test vector and the whole test vector is applied to the circuit under test. During the ensuing m clock cycles of the next scan cycle, the test answer y 0 I is shifted out and the current state component of the subsequent test vector Vj = x j@y j is pushed in. The values of the primary inputs are unimportant until tm when the whole test vector is applied. In other words, the test's efficacy is unaffected if the principal inputs are switched between clock cycles t0 and tm1.

The Applicability of the New Test Application Strategy to Partial Scan Sequential Circuits

Hussain, (2016) stated that after introducing the new BPIC test application technique for full scan sequential circuits, this section provides two detailed examples showing how the same approach may be utilized for partial scan sequential circuits. Scan cell ordering is explained and why it should be used in conjunction with the recommended test application method.

Extention of the New BPIC Test Application Strategy to Scan BIST Methodology

According to Xiang, (2016) for both full and partial scan sequential circuits, this BPIC test application approach has so far been accomplished utilizing external automated test equipment ATE. In brief, the best timing for the main input phase transition is represented by the letter k. Neither traditional full-scan nor partial-scan sequential circuits nor external ATE is required to implement the proposed BPIC test application approach. Below, we'll go through the few tweaks that should be performed while using the scan BIST method. In this way, much as in full- and half-scan sequential circuits, the primary inputs

may be changed out at the optimum time for doing so. More interference will be introduced, but the space overhead normally associated with the scan BIST method will be reduced since the ATE will remember the major input component of each test vector.

3. FINDINGS AD DISCUSSION

According to Jiang, (2018) while examining Methods for Power Minimization in Modern VLSI Circuits it was found that radix-2 non-restoring binary divider circuit implementation on FPGAs exhibiting varying technical features demonstrates the impact of technology factors on design power consumption. There is a clear tendency for the design's dynamic and static power consumption to decrease with technological advancements and increase, respectively. The design's overall effectiveness is affected by the stage of its practical execution. The speed, size, and power consumption of a design might vary depending on its location and routing aims. Parallelism, pipelining, RNS, LNS, etc., are all examples of alternative design architectures that might help reduce the system's power usage. The temporal limitations of the design may be loosened by the use of parallelism, but the system's power consumption cannot. The length of the design critical path may be shortened by using the pipelining approach. The power requirements of a system may be lowered using the pipelining approach, depending on the design's technical factors.

Chen, (2017) analyzed that to focus on the strategies and challenges for low-power VLSI design it was found that many industries are driving the demand for low-power technologies. Unfortunately, optimizing a design for power consumption with performance and area adds another layer to an already challenging design challenge. In conclusion, the many issues and major challenges associated with low-power designs are related to the following trends: a 30% drop in capacitors per node, a 2X increase in electrical nodes, a 14% increase in die size (thanks to Moore's Law), a 15% drop in supply voltage, and a 2X increase in frequency. Active power will grow by a factor of around 2.7 times to deal with these problems. Vt will be scaled to suit frequency requirements, leading to excessive leakage power. An approach to circuit design and low voltage technology that aims for a supply voltage of roughly 1V and operates with decreased thresholds. Wu, (2016) pointed out a method of managing power consumption that dynamically adjusts supply voltage and processing speed in response to a measurement of current demand. Power-efficient connections combine cutting-edge innovation and a more sedate approach to swing and movement. The creation of methods and instruments for logic synthesis, behavioral synthesis, and layout optimization that take power consumption into account. Some applications may benefit from lower power consumption if faster processing times are sacrificed in favor of power-saving methods that recycle the signal energy utilizing the adiabatic switching concepts.

Liu, (2018) analyzed that scaling down the technology has increased leakage current, as was discovered in an investigation of Leakage Power Reduction in CMOS VLSI Circuits. These days, leaky power is more common than dynamic power. For high-performance, low-power digital CMOS devices, leakage current is one of the biggest concerns. The proposed designs have a small leakage current and minimal latency, and they outperform the state-of-the-art methods in terms of both area efficiency and performance. Methodology put forward The most power-efficient method is variable body biasing with bypass since it provides greater maximum current than the basic case (the inverter) and the least leakage current.

According to Oh, (2017), the correlation between subsequent states when switching in test vectors and switching out test answers can be improved by adjusting the primary inputs to complete the fewest possible transitions. This was discovered while focusing on Power Minimisation Techniques for Testing Low Power VLSI Circuits. For each test vector, we provide a novel, test-set-specific approach to determining the optimal BPIC time. Results from a simulated annealing-based study of the design space reveal that combining the proposed method with the previously disclosed scan cell and test vector ordering significantly reduces power consumption during test application in small to medium-sized full-scan sequential circuits. Extensive testing findings with both compact and non-compact test sets reveal that compact test sets waste as much power during test application as non-compact test sets do, but require significantly less time to apply and compute. According to Garello, (2018) the unique BPIC test application strategy may also be utilized to reduce energy utilization in sequential circuits that only scan a portion of the

time. With the recommended test application strategy, power consumption may be minimized with no penalty to other test parameters such as test area, performance, efficiency, time spent applying the strategy, or data set size. It was shown that the partial scan has additional benefits beyond the often cited ones of decreased test area overhead and application time, including lower power consumption during test application and lower computer time required for design space exploration.

4. CONCLUSION AND RECOMMENDATION

Integrated circuits increasingly rely on meeting power dissipation criteria as a prerequisite for design completion. Since the beginning of a design project, it has been on the designer's mind. Design-for-low-power methods of the past, such as clock gating, are insufficient now. As a result, designers are being pushed to drastically alter their methods of working to accommodate more invasive power management strategies. These complex power profiles are now used in the design process, which results in the utilization of multi-voltage domains, power domain shutdown, and multi-threshold cells. To make technology libraries, voltage-specific cell characterization, as well as the visibility of power and ground pins in the logical domain, are additional time-consuming tasks. Intelligent planning is more important than ever before when testing cutting-edge low-power devices due to the many obstacles and compromises that must be considered. In addition, preparatory work should begin right away. There is no shortage of power-aware DFT methods, but they all come with their price tags and prerequisites. The primary goal of the planning is to determine when to run the design's tests and which DFT methods will be sufficient while still limiting power consumption.

The need for testing improved low-power devices is increasing the complexity of designs and forcing them to be tightly optimized for power consumption. There has been a shift in the design process toward low-power design. All EDA tools need to be made power-aware and have uniform support for users' power intent; it is no longer considered as easy, confined incremental adjustments like gating the clocks. One of the major goals in optimizing the low-power design flow, which naturally involves DFT synthesis, is to improve power analysis and estimate in terms of accuracy and speed and to connect it at various phases of the flow where the design is being improved. This will provide the necessary predictability, which will assist avoid very expensive design revisions.

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