FPGA Based PWM Techniques for Controlling Voltage Source Inverter

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***Abstract*— A built-in self-repair analyzer with the best repair rate for redundant memory arrays is used in this project. The prevailing methods made use of a stack and a finite-state machine for depth first search. The circuit's design enables use of the parallel prefix method, and it may be set up in a variety of ways to satisfy space and test time needs. The number of content addressable memory entries used to hold the defect addresses makes up the majority of the infrastructure overall, and it only increases quadratically as the number of repair elements increases. In the BIST architecture, the linear feedback shift register is utilised to count the subsequent state and also necessitates high transitions. To locate the defect address to store in mustrepair analyzer, the content addressable memory is used. The suggested approaches make use of pre computation content addressable memory and bit swapping linear feedback shift registers to minimise transition and power consumption, respectively, as well as to shorten the time delay in the analyzer that needs repair. Even in the worst situation, only one test is needed. It selectively stores fault addresses by carrying out the must-repair analysis during the test, and uses the saved fault addresses for the final analysis to provide a solution. Additionally, the architecture has been expanded to accommodate several word-focused memory types.**

***Index Terms*—PWM, FPGA, ASIC, AISCPWM**

I. INTRODUCTION

Nearly all embedded systems today include pulse width modulation (PWM) as a fundamental component. It is commonly used as a control method in most electronic appliances. These methods have been the subject of in-depth investigation during the past few years [2]. Various approaches exist depending on the system's architecture and requirements. According to N.A. Rahim and Z. Islam [2,] the PWM method is dependent on the application type, power consumption, semiconductor devices, performance, and cost requirements. According to E. Koutroulis, A. Dollas, and K. Kalaitzakis in [1], one of the most significant applications of PWM is in power electronics applications for managing power converters (DC/DC, DC/AC, etc.). One type of power converter that makes extensive use of the PWM principle is the PWM inverter. Due to their improved performance, PWM inverters are currently quite common in industrial applications. This popularity is the result of developments in semiconductor electronics and design technologies. To create a supply of variable voltage and frequency, many different PWM methods are employed. Optimal PWM and carrier PWM are two forms of PWM approaches, according to N.A. Rahim and Z. Islam in [2]. The best PWM involves a lot of computation, which necessitates additional hardware and raises the cost [2]. In order to produce the necessary PWM signal, carrier PWM approaches need a carrier signal that has been modulated with a modulator signal.

PWM TECHNIQUES

There are two main types of PWM techniques: an analog and a digital one. In an analog PWM, the carrier signal is used and the modulating signal is used. The two signals are compared using a comparator and the result is the PWM output that is desired. There are four types of analog PWM (a) sinusoidal PWM (b) modified PWM (c) single PWM (d) multiple PWM (7). [2] According to [4] and [7], the drawbacks of these analog PWM methods are that they are susceptible to noise and change with the voltage and temperature. They also suffer from component variation. They are also less flexible than digital methods. [2] Digital PWM Generators are the most suitable form for designing. They are highly flexible and less susceptible to environmental noise. They are

easy to construct and very fast to implement. The majority of the digital PWM Generator uses counter and comparators-based circuits.

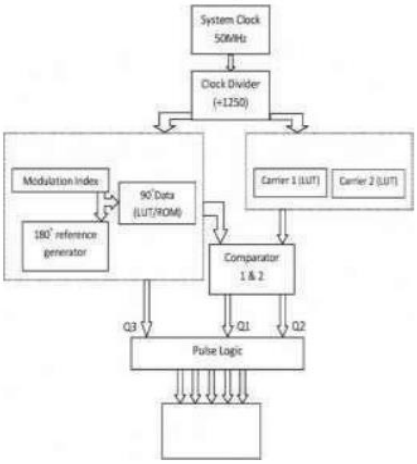


Fig. 1: 1 PWM Generation Method

ADVANTAGES OF FPGA BASED DESIGN

The most favoured method of building a PWM generator for power converter applications is with a field programmable gate array (FPGA). Essentially, they are connections between several logic pieces. When a design is implemented on an FPGA, it is done so in a way that it can be easily adjusted in the future if necessary. Just the connections between these logic blocks need to be altered. This FPGA's capacity to be reprogrammed makes it appropriate to use it in your design [1]. We can quickly execute designs utilising FPGA as well. Therefore, creating digital PWM generators using FPGA is the best option. Additionally, FPGA-based digital control systems seem to be less expensive to install, making them economically advantageous for modest designs [1]. Thatswhy FPGA based PWM Generator technique is discussed in this project.

PWM Techniques

PWM is one of the most widely used signal processing techniques in power conversion applications. PWM involves the generation of switched voltage pulses for different output frequency and voltages using a typical modulator. The average voltage produced by the modulator is equal to or less than the reference voltage during each period of PWM operation. For a relatively short period of time, the reference voltages are reflected in the fundamental of PWM (Grahame and Thomas, 2003). The advantages of PWM techniques include: Output voltage control can be easily achieved without complex circuits. Lower order harmonics are eliminated or minimized in the output along with voltage control. Higher order harmonics are easy to filter. PWM is considered a high frequency processing operation in a power conversion technique for optimization of a particular performance criterion such as: Minimizing THD Reducing distribution harmonic power Reducing heat losses etc. PWM operation reproduces the waveform of a synthesized wave. PWM pulses have a variable width and a constant amplitude. Michael (1998) observed that, the harmonics in the output waveform of the converter are usually selected as the performance criterion, and it is generally desired to reduce them in most applications. The frequency of the PWM should be maximised to minimize the harmonics effect on the motor performance. However, the frequency is limited by the resolution and switching device capabilities.

2. DIGITAL IMPLEMENTATION OF PWM METHODS

The growth of digital implementation of the PWM algorithms have revolutionized the field of inverter control considerably, and contributed to enhance the quality of power through effective suppression of undesired orders of harmonics. There are various PWM schemes which offer the desired control performances. It starts with a naturally sampled PWM, followed by a regularly sampled approach. According to Chin et al (1984) the traditional PWM switching strategy incorporates the natural sampling technique where a fixed triangular carrier waveform is matched to a sinusoidal reference waveform with variable magnitude and frequencies, and the coincidence point determine the pulse width. In the traditional PWM schemes, the harmonic power of a power waveform is usually concentrated in the high frequency 6 range due to the high switching nature of the power converter.

These high frequency harmonics can have adverse effects such as acoustic noise, harmonic heating in the electric machine and radio interference. An efficient switching technique of the PWM can improve the quality of a VSI by reducing the THD and increasing the fundamental voltage, as described by Houldsworth and Grant (1984). The researchers have concentrated more on improving the PWM switching strategies of VSI rather than changing the circuit topologies as per

Van Der et al (1988) and Ali Yazdian Varjani et al (1998). Depending upon the application requirements, PWM methods of different concepts and performance objectives are developed. Such continued changes of PWM schemes demands a programmable platform for PWM signal generation as per Green and Boys (1982). Generating PWM signals requires a high sampling rate in order to achieve a wide bandwidth performance. Digital platforms offer improvements over their analog counterparts. They are immune to noise and are less susceptible to voltage and temperature changes. According to Monmasson and Chapuis (2002) most computation resources of the processor are used for generating PWM signals. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for complex circuitry and rapid prototyping make it the preferred choice for prototyping an Application Specific Integrated Circuit (ASIC). Several attempts have been noticed with the motivation of perfect imitation of natural sampled SPWM in a digital platform. Khaled et al (1989) used a16-bit microprocessor (MC68000) system to generate pulse width modulation (PWM) voltage waveforms for a three phase VSI. The features such as quarter wave symmetry, 1200 phase differences etc. are exploited for conserve the processor time.

A flexible, inexpensive laboratory setup that can be configured for exploring a number of power converter topologies, 7 controlled in both open loop and closed loop has been presented by Brekken and Mohan (2006). In addition to driving passive loads, the setup can be used to demonstrate DC motor torque, speed, and position control, as well as variable speed three-phase AC motor control. Angel (2003) et al presented an FPGA based digital control for a Power Factor Correction (PFC) flyback AC/DC converter.

3. FUNCTION OF PROPOSED SYSTEM

The generation of PWM patterns through modulation involves amplitude to width transformation. That is, the suitable carrier-based PWM method programs, a "per carrier cycle average output voltage" equal to the reference voltage. In the traditional unipolar sinusoidal PWM (SPWM), a triangular carrier and a sinusoidal reference are compared for generating the gating pulses. In the SPWM switching strategies, fundamental enhancement demands an increase in pulse width in the regions around the center of the reference wave.

The relationship between reference output voltage and voltage gain is linear until reference voltage magnitude is greater than the limit of modulator linearity and the condition is known as over modulation. There is no straightforward PWM algorithm that keeps voltage gain linear until full utilization of the dc input for single phase inverter system. Transition from PWM operation to square wave mode operation was one of the unresolved issues that limited the performance of the AC drive systems. Modulated regular sampled SPWM Scheme called amplitude modulated inverted Sine carrier PWM is proposed to provide SPWM single mode operation. AISCPWM (Amplitude Modulated Sine Carrier PWM) offers linear gain characteristics compared to conventional SPWM without complex calculations and significant device losses.

Amplitude Modulated Inverted Sine Carrier PWM Method

This makes use of a novel Amplitude Modulated Inverted Sine Carrier (AMISC) function which has the conventional sine wave as a reference signal whereas the carrier is amplitude modulated inverted sine signal as shown in Figure 5.1. The carrier is a high frequency inverted sine, which is (amplitude) modulated by a sinusoidal modulating signal of reference frequency.

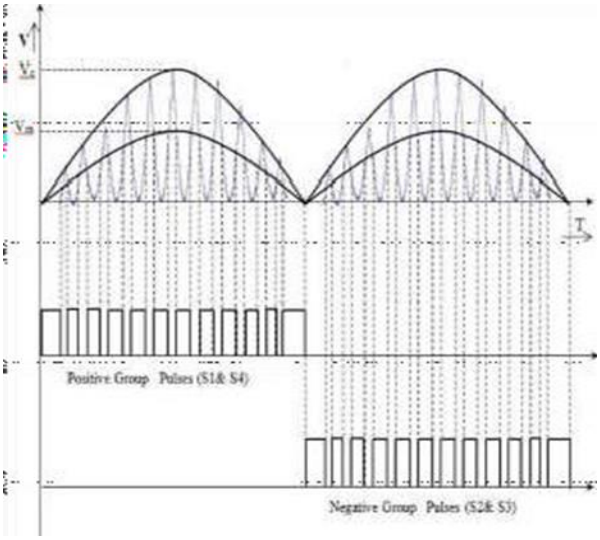
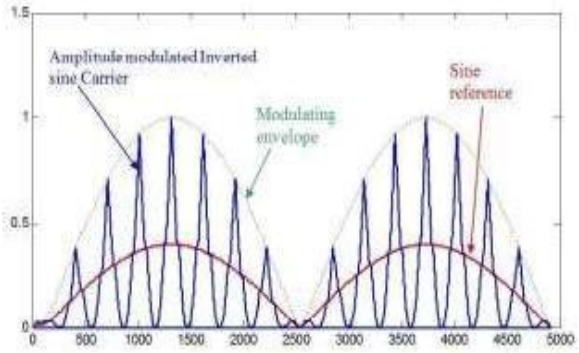


Figure 3.1 Concept of AMISC Function

Modified regular sampled SPWM scheme named Amplitude Modulated Inverted Sine Carrier (AMISC)



PWM has been developed to give single mode operation of SPWM inverter. This PWM scheme combines the advantages both ISCPWM and AMTCPWM

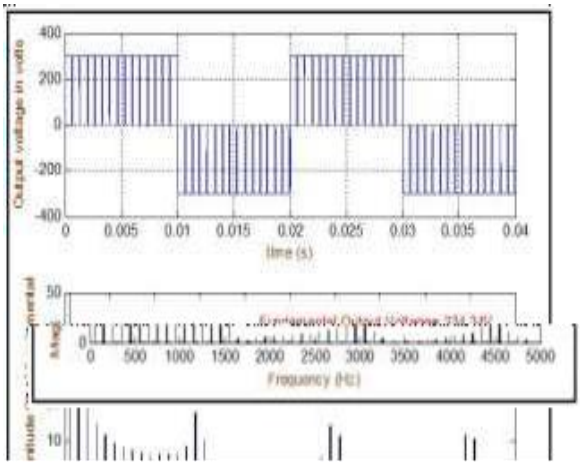


Figure 3.2 AMISC-PWM Pulse Pattern

4. PROPOSED DIGITAL IMPLEMENTATION AMIC-PWM METHOD

A digital architecture has been developed to implement the AMISCPWM technique as shown in figure. The architecture consists of Sine Data Manipulation (SDM) Unit, Reference Wave Scaling (RWS) Unit, Amplitude Modulated Sine Inverted Carrier Generation (AMSICG) Unit and Comparing and Pulse Separation (CPS) Unit. In this novel architecture, the modules are performing parallel. The Functionality of the units like SDM, RWS and CPS are similar to the ISC-PWM architecture and it has been discussed detail in the previous chapter.

The Amplitude Modulated Inverted Sine Carrier generation Unit (AMISCGU) is designed using the VHDL as in appendix A2.3. This unit comprises the sine generation, sine inversion and peak correction.

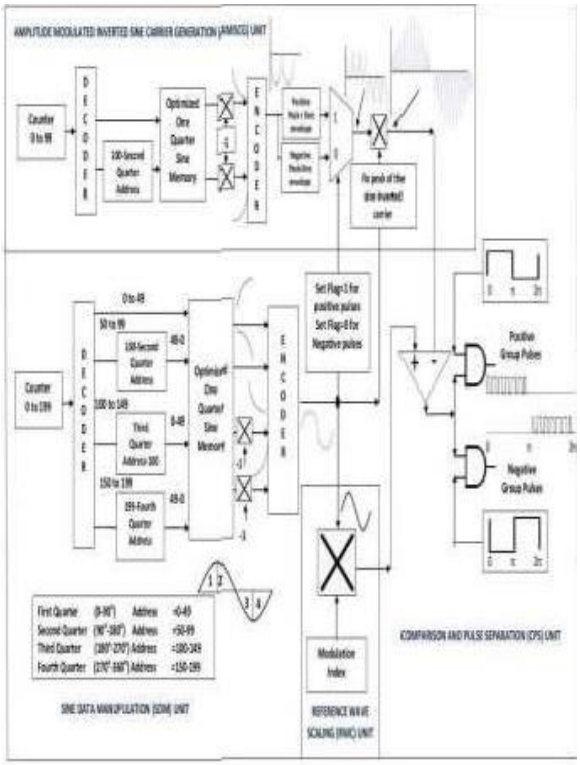


Figure 3.3. Proposed AMISC Architecture system

5. SIMULATION RESULTS AND DISCUSSION

FUNCTIONAL SIMULATION

The functional simulation of the designed AMISC-PWM architecture has been carried out using the Modelsim software. Using the Xilinx ISE tool, the functional verification of the design has beendone.

The gating pulses generated by the VHDL design for the positive and negative group switching devices of inverter have been analyzed in the Modelsim software. The gating pulses generated for the modulation indexes of 0.4 and 0.8 are shown in Figure 4.1 and Figure 4.2 respectively

The user-specified synthesis constraints like timing, power and area of the AMISC-PWM design have been verified using the Xilinx ISE software tool to optimize and implement the RTL design into equivalent unit-delay primitive blocks (flip-flops, logic gates, etc.). The RTL schematic view of the design and Logic implemented area has been verified virtually as shown in the figure 4.3 and 4.4 respectively. The graphs are shown below.

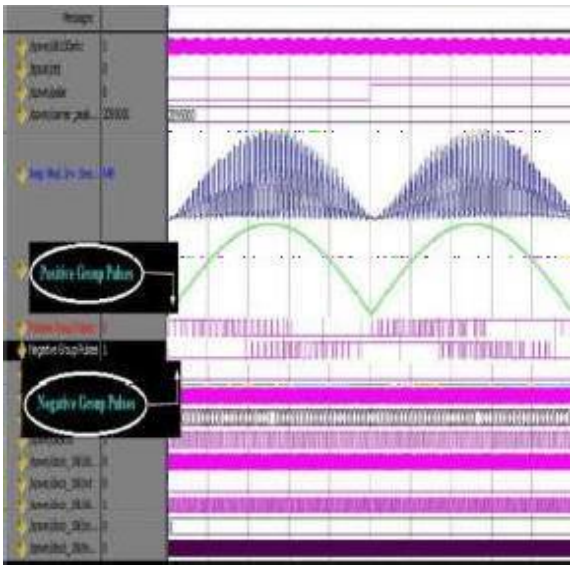


Figure 4.1 Modelsim output pulses for Ma = 0.4

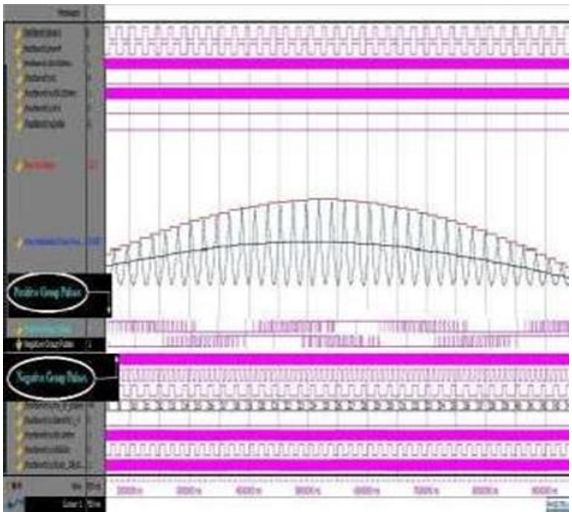


Figure 4.2 Modelsim output pulses for Ma = 0.8

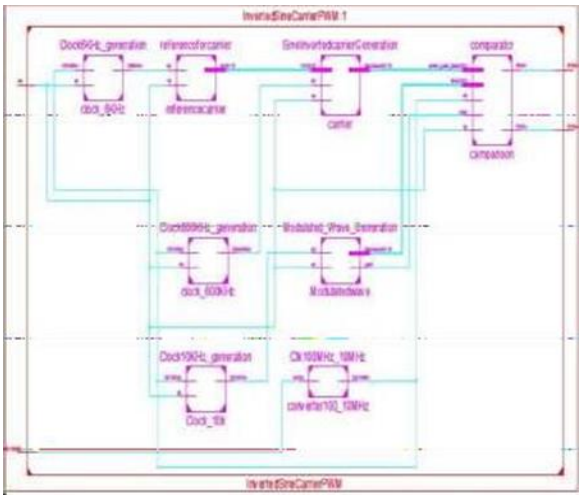


Figure 4.3 RTL Schematic View ofAMISC-PWM Design

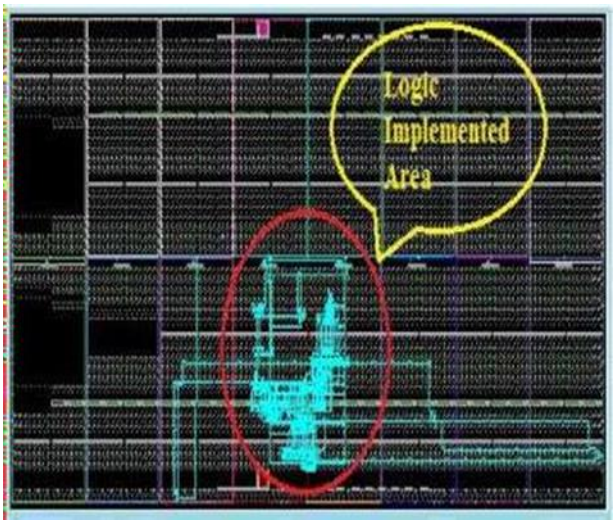


Figure 4.4 Logic implemented area for the AMISC-PWM Design

6. CONCLUSION

The major expectation from any PWM strategy is the voltage linearity, harmonic distortion, and maximum obtainable output voltage. The proposed architecture of novel AMISCPWM has produced a high output voltage and low THD. The architecture developed for generating the novel carrier function provides a high degree of flexibility in the digital implementation. The FPGA based AMISCPWM architecture is capable of producing the pulses with high resolution and better reliability due to its parallel computational nature. This PWM strategy has exhibited a better hardware realization with a single phase VSI. The comparative analysis between the other modern PWM strategies showed that the proposed novel PWM strategy is suitable for the system which needs a high output voltage.

FUTURE WORK

ASIC level design can be done for the PWM strategies to develop the dedicated PWM generation chips. It will be interesting to explore the options of implementing PWM strategies in closed loop drive systems

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