Ultra Low Power Voltage Deviate-Domino LogicCircuits with Low Noise Tolerance System

E.Lenin[1], V.Suresh[2], Dr.K.Somu[3]
[1]PG Student, Department of ECE, Maha Barathi Engineering College
[2]Assistant Professor, Department of ECE, Maha Barathi Engineering College
[3]Associate Professor, Department of ECE, Maha Barathi Engineering College

***Abstract*—A new noise-tolerant dynamic CMOS circuit approach is suggested with improved domino CMOS logic behaviour. Domino logic circuits are frequently chosen in high-performance designs due to their advantages of high speed and low area overhead. But in integrated circuits, the power used by clocking gradually becomes a determining factor. For this reason, the main goal of this research is to examine the performance of a voltage deviate-domino circuit using the Prescient Innovation Model (PIM) control method to compare the effectiveness of various domino techniques in terms of delay, power, and their outputs, such as the figure of merit on the spice model when using an EDA tool on a 0.18-micron CMOS process technology Utilising spice model EDA, the proposed PIM voltage deviate domino logic is created. The performance of proposed voltage deviate domino circuit is validated through simulation. The simulation results demonstrate the reduction improvement in the noise immunity, power consumption, delay and similar noise of results has to be demonstrated power reduction and speed change in voltage variation-Domino Circuit Registry file associated with the regular Registry file.**

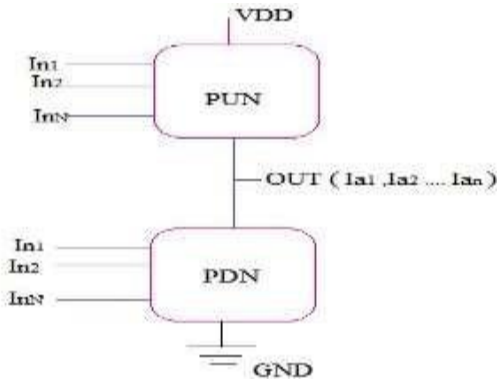
I. INTRODUCTION

Computer systems are becoming more compact, quicker, and less expensive as technology advances. Scaling of Very Large-Scale Integration (VLSI) technology has made this possible as the device density index rises and the operating frequency becomes simpler. As a result, electricity consumption has risen to the point where it is no longer affordable or reliable. Additionally, challenges with design reliability such soft mistakes, signal integrity, and process unpredictability are brought on by continual scaling to Nanosystems. Additionally, difficulties with power usage and toughness deteriorate over time. This has complicated the construction of computer systems and prevented the development of an unknown block in the future. Power usage and design reliability must be taken into account at every stage of the design, according to Pioneer Computing Systems researchers. The selection of logic type is crucial for any circuit-level design since it has a direct impact on power usage, performance, and durability.

Future computing demands cannot be fully satisfied by domino logic and static complementary metal-oxide semiconductor (CMOS). Static logic and dynamic logic are the two fundamental CMOS circuit architectures. Although static CMOS is more resilient and energy-efficient, it performs poorly with complex and important designs.

II. OVERVIEW OF LOGIC STYLES

In 1963, Frank Wanlas made the initial proposal for the complementary metal-oxide-semiconductor. Due to its low power consumption (virtually no power) when the gate input does not change, this is the design of the logical digital semiconductor sector for a variety of applications. A strong one can be driven by PMOS field-effect transistors, which are positive channel metal oxide semiconductors, and a strong zero can be driven by NMOS field-effect transistors, which are negative channel metal oxide semiconductor.



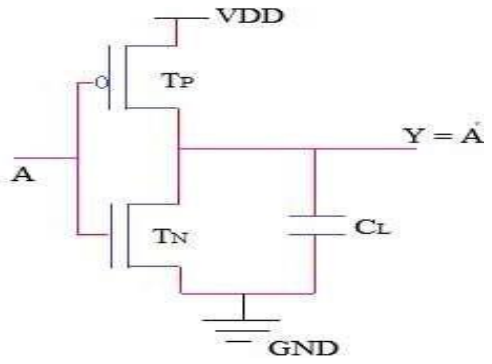


Figure 1.1 Circuit diagram of Static CMOS Logic

Different Static Logic Styles

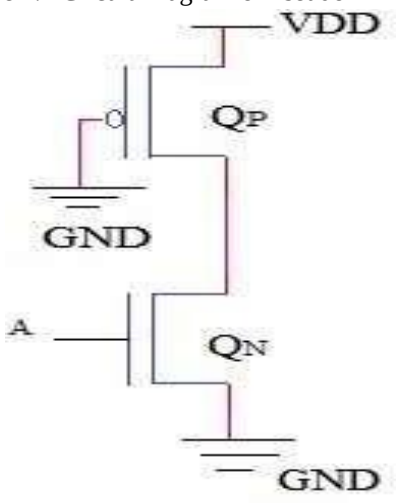
The static CMOS logic styles are classified into three categories

i. Pseudo NMOS
ii. Pass transistor logic
iii. Differential/Complementary Pass Transistor Logic

Pseudo NMOS

A CMOS inverter that has been changed. In this case, the input voltage just drives QN. The grounded gate of QP serves as an active load for QN. The load is referred to as the "Pseudo NMOS Load" and is shown in Figure.1.2. A driver transistor QN and a load transistor QP make up this inverter circuit, another type of NMOS logic. As a result, the name is "Pseudo NMOS."

Figure 1.2 Circuit Diagram of Pseudo NMOS Load



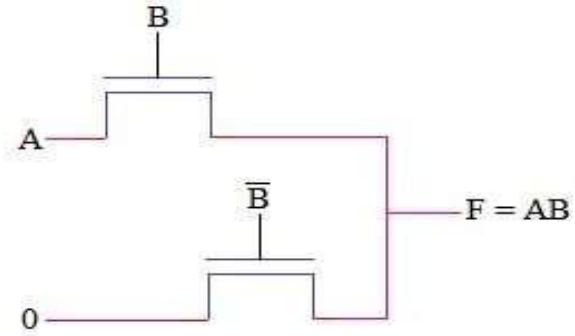


Figure.1.3 Circuit Diagram of Pass Transistor Logic

III.LITERATURE SURVEY

Dynamic circuits, such as domino logic circuits, are widely used in highperformance microprocessors for static CMOS circuits where high speed is not possible. Their high speed is due to reduced input capacitance, small switching thresholds and circuitimplementation that usually with fewer logic levels. Due to efficiency, the use of wide and complex logic gates. But the penalty to be paid for speed improvement is the increased power dissipation, mainly due to the necessary clocking and increased noise sensitivity. Therefore, this imposes design challenges for dynamic circuits. In addition, as technology continues to scale, it is necessary to lowerthe supply voltage to reduce dynamic power in deep sub-micron systems and avoid reliability issues. A detailed survey of the different CMOS logic is provided in this section.

STATIC CMOS LOGIC

Massimo Alioto and colleagues (2010), As a function of circuit-level factors, the impacts of delay process modifications on static and dynamic CMOS logic gates are carefully examined. This work's key addition is a thorough examination of the circuit parameters, including the number of stacked transistors, their size, load capacitance, and the circuit topology's influence on delay variation. To do this, straightforward models are created for both intradie and interdie variations, and the primary sources of variability are determined for each.

Keote et al. (2018) provide a design and implementation of 2*2 array and 4*4 array multipliers using proposed Two-Phase Clocked Adiabatic Static CMOS logic (2PASCL) circuit. Naoto Kikuchi et al. (2010) propose a unique gate drive circuit, which can fully utilise the Keote et al. (2018). Adiabatic energy recovery is the foundation of the suggested 2PASCL circuit, which uses less power. Two sinusoidal power clocks that are 1800 phase-shifted apart are used in the

proposed 2PASCL. The measurement results of the 2*2 array proposed 2PASCL multiplier show power reductions of 80.16% and 97.67% in comparison to reported 2PASCL and conventional CMOS logic, and the measurement results of the 4*4 array proposed 2PASCL multiplier show power reductions of 32.88% and 82.02%. Performance of the Vertical Field Effect of the Screen Grid The lowest input vector for the impact of gate leakage, total leakage current, and increasing the NMOS transistor of the stacked transistor on the Transistor (SG-VJFET) is discussed by Nikhil Saxena et al. (2013). Two common gate driver ICs, capacitors, and diodes are used in the proposed circuit to enable quick switching without a significant power loss and to enable high frequency and any duty cycle operation.

IV. VOLTAGE DEVIATE-DOMINO CIRCUITS FOR LOW POWER HIGH-SPEED APPLICATIONS USING PRESCIENT INNOVATION MODEL

In VLSI circuit excessive-velocity records verbal exchange, propagation postpone and coffee energy utilization are arguments of desire for CMOS implementation in unique domino good judgment. In conventional domino circuits essentially paintings with noninverting good judgment however on this non-inverting logic have some big issues together with high leakage electricity and excessive propagation postpone.So nevertheless the efficiency improvement of domino good judgment is quite difficult as it requires more inverters for implementation. So static CMOS based domino good judgment circuits want each inverting and non-inverting common sense to conquer this problem. Besides static CMOS logic is slower than dynamic good judgment and knows the massive region overhead, and large dispersion of quick-circuit strength.

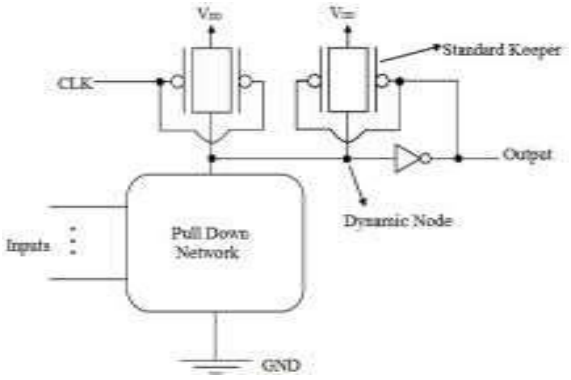


Figure 3.1.Standard Footless Domino Configuration

The configuration of standard Footless Domino configuration is shown in Figure 3.1.This approach reduces circuit performance over energy loss, which requires certain areas to be implemented using static CMOS, which may delay it.

The block diagram of voltage deviate-domino circuit Implementation is proven. 3.2. As compared with normal domino circuits the proposed VDDC is reduced the overall strength usage as it disconnects the output from the pull-down network. In fact the n-bit inverter is shown in determine 3.Three. Whilst the N-transistor is attached the pull-down transistor (M2) is connected throughout the output terminal of the inverter. Therefore, the enter of the voltage deviates domino circuit is still full voltage swing and additionally get low energy potential, as compared to conventional domino circuits with decrease voltage

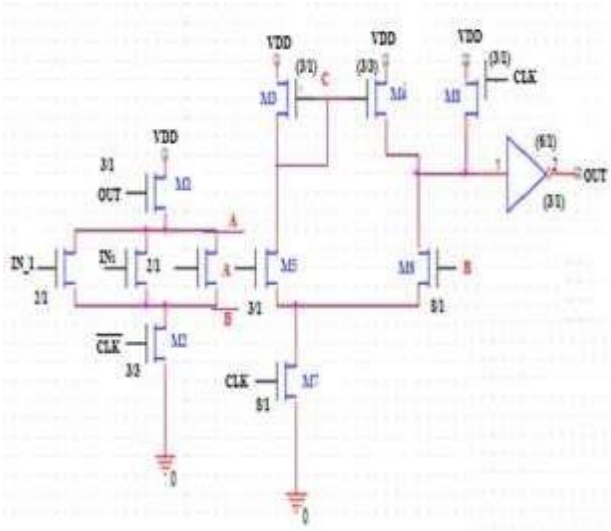


Figure 3.2 The voltage deviate-domino circuit

There are four timing parameters: Rising time (tr) During the transition, output switches from 10 % to 90 % Fall time (tf) When output switches from 90 % to 10 % After application of input, the propagation delay of the logic gate (e.g., inverter) is calculated at 50 % (calculated at input-output transition). Many designs could prefer 30 % to 70 % rising time and 70 % to 30 % fall time. Propagation delay high to low This is the delay when the output switches from high to low, after the input switches from low to high. The propagation delay is typically calculated at the 50 % point of the input-output transition. Different designs

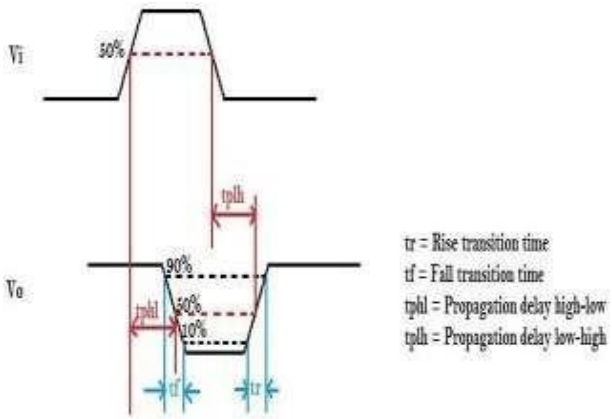


Figure 3.3 Propagation Delay

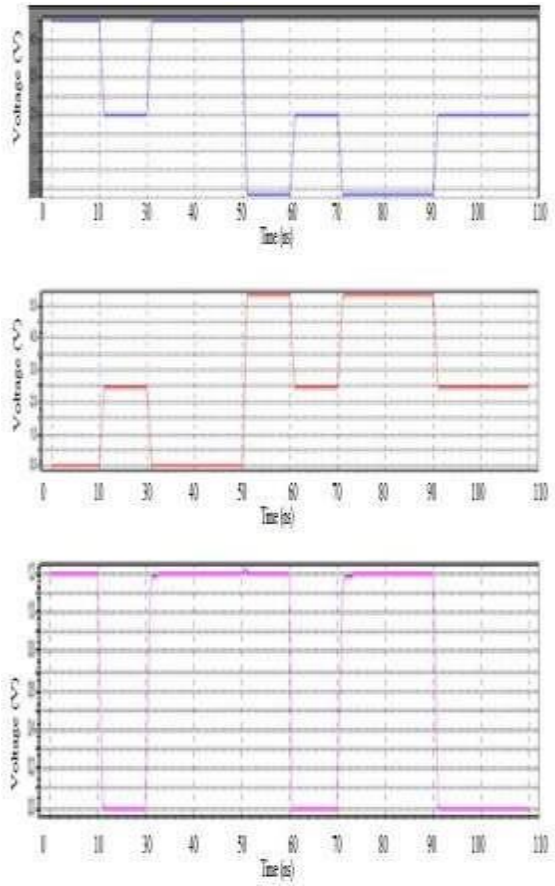
V. SIMULATION RESULTS AND DISCUSSSIONS

Maximal power reduction in domino logic gate with PIM v2.1 16nm technology compared to 0.8 V fan spice simulation (64 bits, 32 bits, 16 bits and 8 bits wide) in prescient innovation model (PIM) Proposed domino logic Voltage Deviate Domino Circuit Proposed voltage deviation domino circuit Domino logic technique Power assessment Domino logic voltage deviate circuit Voltage deviation domino circuit simulation parameters Table 4.1

Parameters	**Values**
Tool	Tanner EDA
Process Technology	0.18μm
Frequency Range	215MHz – 386MHz
Supply Voltage	0.8V
Temperature	25ºC – 110ºC

Table 4.1 Design Parameters used for voltage deviate-Domino circuit Domino Logic

Figure 4.1. Input and output power of the



voltage deviate-domino circuit

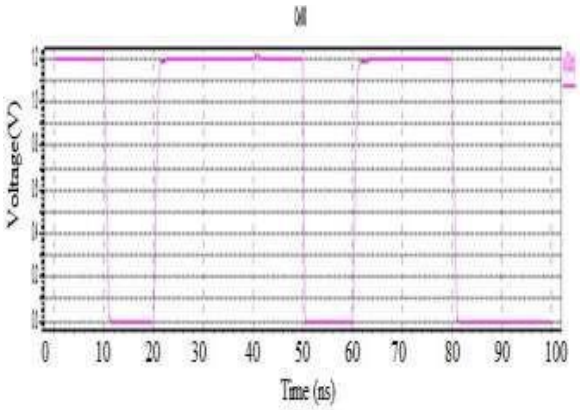


Figure 4.2. Simulation Results for Power Dissipation and Figure of Merit with VDD= 0.8V

Voltage deviate-domino circuit input and output power is shown in Fig. 4.2. The input and output waveform is obtained from the TSPICE simulation. The parameters are shown in Table1 and simulation result power dissipation and figure of merit against VDD is 0.8V.

VI. CONCLUSION AND FUTURE SCOPE

In this work, we proposed a new innovative technique based on domino circuits to solve all problems. Based on the results of the simulation, the domino logic circuit offers several benefits such as low power consumption and low propagation delay, in the proposed PIM domino system, different voltages are applied across the pull down network and finally the output is provided based on this operation. Thus, the performance improves without degrading the robustness. The proposed PIM has separated the pull-down net from the inverter, reducing the propagation delay and voltage swing in the pull down network, especially when the minimum range is of power consumption in the WFI gates. The threshold switching voltage of our proposed domino circuit was about twice as compared to the threshold range of the NMOS transistors, so the overall performance of our proposed system increased, only the number of fans-in increased. Our proposed method only achieves minimum power only. For example, the normalized power of a 64 bit PIM consumes 0.57 uw only.

REFERENCES

[1] Dev and R.K Sharma, Controlled delay- through dynamic logic: leakage-toleranthigh-speed dynamic logic, ELECTRONICSLETTERS, Vol. 51 No. 23 pp. 1856–1857, November 2015.

[2] Akanksha Chouhan; Vikas Mahor; Manisha Pattanaik,"A novel delay minimization technique for low leakage wide fan-in domino logic gates," International Conference on Computers and Devices for Communication (CODEC), 2012.

[3] Ambika Prasad Shah; Vaibhav Neema; Shreeniwas Daulatabad,"PVT variations aware low leakage DOIND approach fornanoscale domino logic circuits," IEEE Power, Communication and Information Technology Conference (PCITC), 2015.

[4] Asya, Mohammad. (2017). A new low-power dynamic circuit for wide fan-in gates.Integration, the VLSI Journal. 60. 10.1016/j.vlsi.2017.10.010.

[5] Angeline, Anita & Bhaskaran, V s Kanchan. (2018). High Performance Domino LogicCircuit Design by Contention Reduction. 10.1007/978981-10-7251-2_18.

[6] Ching-Hwa Cheng; Chiou-Kou Tung,"A High-Performance Pipeline Mixed Static- Domino Circuit Synthesizer," International Symposium on Computer, Consumer, and Control, 2012.

[7] D.Bhanu Chandra "Suppression of Short Channel Effects (SCEs) by Dual Material Gate Vertical Surrounding Gate (DMGVSG) MOSFET.

[8] Deepika Bansal "Efficient Keeper For Pseudo Domino Logic" International Journal of Pure and Applied Mathematics, Volume 117 No. 16 2017, 605-612.

[9] F. Frustaci; M. Lanuza; P. Zicari; S. Perri; P. Corsonello "Lowpower split-path data- driven dynamic logic" IET Circuits, Devices& Systems, Year: 2009, Volume: 3, Issue: 6,Page s: 303 – 312.

[10] Garg, Sandeep & K. Gupta, Tarun. (2019). FDSTDL: Low-power technique for FinFET domino circuits. International Journal of Circuit Theory and Applications. 47. 10.1002/cta.2627.

[11] Gavaskar, K. & Ragupathy, U.. (2018). Low power self-controllable voltage level and low swing logic-based 11T SRAM cell for high-speed CMOS circuits. Analog Integrated Circuits and Signal Processing. 100. 10.1007/s10470-018-1277-3.

[12] H. Mahmoodi, K. Roy Diode, Footeddomino: a leakage sophisticated high fan-indynamic circuit design style, IEEE Trans. Circ. Syst. -I 51 (3) (2004) 495–503

[13] Jitesh R Shinde; Suresh S Salankar; Shilpa J Shinde,"Multi-objective optimization domino techniques for VLSI circuit," International Conference on Advances in Computing, Communications, and Informatics (ICACCI), 2016.

[14] K. Roy, S. Mukhopadhyay, H. Mahmoodi, Leakage current mechanisms and leakage reduction techniques in deep-submicron CMOS circuits, Proc. IEEE 91(2) (2003)305–327.