MOSFETs' Technology – Linear and Planar to Hydrogen Terminated Non – Planar Devices

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***Abstract*—This paper presents a review of the development of SOI – MOSFET from Single Gate (SG) and Multiple Gate (MG) devices to the Hydrogen Terminated Diamond Transistor (HTDT) Structures. The physical structure of Double and Triple gate SOI – MOSFET is discussed along with the operation, advantages and drawbacks. The promising features of HTDT devices are also discussed with an objective of gaining a deeper insight into their futuristic developments.**

***Index Terms*— HTDT, MG SOI – MOSFET.**

I. INTRODUCTION

The single gate Silicon – On – Insulator MOSFET (SOI MOSFET) is categorized into Partially Depleted (PD) and Fully Depleted (FD) structures [1]. The PD – SOI is affected by phenomenon generally called floating body effects, which are suppressed to certain extent in the FD – SOI [2] – [4]. The floating body effects viz. Kink effect, single transistor latch phenomenon give undesirable behavior at high switching speeds. With continuous miniaturization of electronic components, it became necessary to improve the current driving ability of device and simultaneously reduce floating body effects. This led to the development of SOI – MOSFET with multiple gate terminals [5] – [12]. Subsequently the scaling down to sub nanometer level has led to the occurrence of Narrow Width Effects (NWE) which gained dominance along with the already existing Short Channel Effects (SCE) [13] – [15]. Lightly Doped Drain (LDD) – MOSFET, Selective Back Oxide (SELBOX) SOI – MOSFET did exhibited better channel control with higher electrostatic integrity [16], but were process intensive in the fabrication [17] and hence unfeasible for bulk techniques [18], [19]. Thereafter, the development of Diamond [20] as a substitute for silicon based bulk devices and the promising features of Hydrogen Terminated Diamond Transistors seem to provide an alternative with tremendous potential for developments against the performance debilitating drawbacks of the MG SOI – MOSFET.

III. PLANAR STRUCTURES FOR SEMICONDUCTOR DEVICES

The Gate All Around MOSFET (GAA – MOSFET) [5], shown in Fig 1, was the first planar double gate SOI – MOSFET.

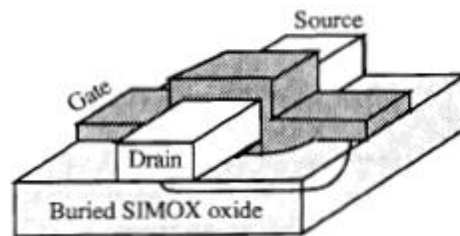

Fig. 1Gate All Around SOI – MOSFET

The Gate terminals at Top and Bottom of the channel as shown in fig 1, increase the effective width of Gate, thereby enhancing the volume inversion which results in a higher current drive and transconductance [6], as compared to earlier bulk devices. There was an increase in the demand for non – planar devices mainly owing to their higher channel control and better electrostatic integrity.

III. DIAMOND SEMICONDUCTOR DEVICES

Diamond as a material has shown to have high breakdown field, better mobility, and a larger thermal conductivity [21], [22], thereby leading to a drastic reduction of the conduction and switching losses. High temperature and high voltage operations [23] using diamond for diodes has been exhibited for various

structures. While the on state resistance varied from 83.4 mΩ cm^2 to 13.3 Ω cm^2 at 400 °C, the reverse leakage current was found to be a function of various parameters like thermionic emission: equation (1), and barrier lowering and Schottky barrier height as in equation (2).

$$j_R = A^* T^2 e^{-\frac{q\varphi_B}{k_T}} \quad (1)$$

$$j_R = A^* T^2 e^{-\left[\frac{q}{k_T} * \left(\varphi_B - \frac{qE}{4\pi\varepsilon}\right)\right]} \quad (2)$$

The floating metal ring structure for the edge termination has been proposed to ensure an enhancement of the breakdown voltage. However, the deposition of material like Titanium or Nickle proves to be process intensive, in addition to leading a variation of the breakdown voltage over a range of devices. Thereby, the barrier voltage can be evaluated from the coefficients of impact ionization of holes and electrons as given by (3), (4)

$$i_h = a_h . e^{-\frac{B_h}{|E|}} \quad (3)$$

$$i_e = a_e . e^{-\frac{B_e}{|E|}} \quad (4)$$

These apparent drawbacks have been overcome to a large extent by the inclusion of multichannel power devices, but with an added feature of the device being in the on state continuously, unless turned off.

IV. CONCLUSION

Put together it is apparent that many of these devices are limited by the breakdown voltage. More importantly the effects of surface roughness need to be further delved into for the mitigation of the conductivity issues arising out of the anomalies during the fabrication process. While it definitely seems to be future full of tremendous potential for the diamond semiconductor devices, in conjunction with the scope for non-planar devices does seem to hold a positive outlook for experimentation.

REFERENCES

[1] Keshkamat S. M., "Silicon – On – Insulator MOSFET", Proceedings of IEEE International Conference on Advanced Computing and Communication Technologies, Nov. 2012, pp. 168 – 171.

[2] Balestra F., Cristoloveanu S., Benachir M., Brini J., Elewa T., "Double Gate SOI Transistor with Volume Inversion: A New Device with Greatly Enhanced Performance", IEEE Electron Devices Letters, vol. 8, Issue 9, Sept. 1987, pp 410 – 412.

[3] Hisamoto D., Kaga T., Kawamoto Y., Takeda E., "A Fully Depleted Lean Channel Transistor – DELTA) –A Novel Vertical Ultra Thin SOI MOSFET", Tech. Digest IEDM, 1989, pp. 833 – 836.

[4] D. Hisamoto, T. Kaga, and E. Takeda, "Impact of the Vertical SOI DELTA Structure on Planar Device Technology", IEEE Trans. Electron Devices, vol. 38, 1991, pp. 1419-1424.

[5] Colinge J. P., Gao M. H., Romano A, Maes H., Claeys C., "Silicon On Insulator Gate All Around Device", Tech. Digest IEDM, 1990, p. 595.

[6] T. Tanaka, H. Horie, S. Ando, and S. Hijiya, "Analysis of p+ Double Gate Thin-Film SO1 MOSFET's," I991 IEDM Tech. Dig., pp. 683 – 686.

[7] Suzuki K., Tanaka T., Horie H., Arimoto Y., Itoh T., "Analytical Surface Potential Expression for Thin – Film Double Gate SOI MOSFET", Solid-state Electron. vol. 37, pp. 327-332, 1994.

[8] Suzuki K., Tanaka T., Horie H., Sugii T., "Ultra Fast Operation of Vth Adjusted p+ - n+ Double Gate SOI MOSFET", IEEE Electron Devices Letters, vol. 15, Issue 10, Oct. 1994, pp 386 – 388.

[9] Suzuki K., Sugii T., "Analytical Models for n+ - p+ Double Gate SOI MOSFET", IEEE Trans. Electron Devices, vol. 42, Issue 11, Nov. 1995, pp 1940 – 1948.

[10] Baie X., Colinge J. P., Bayot V., Grivei E., Proc., IEEE International SOI Conference, 1995, pp 66 – 67.

[11] Park J. T., Colinge J. P., Diaz C. H., "Pi-Gate SOI MOSFET", IEEE Electron Devices Letters, vol. 22, Issue 8, Aug. 2001, pp 405 – 406.

[12] Yang F-L, Chen H-Y, Cheng F-C, Huang C-C, Chiu H-K, et al, "25nm CMOS Omega FET" 2002 IEDM Tech. Dig., pp. 255 – 258.

[13] Ja – Hao Chen, Shyh – Chyi Wong & Yeong – Her Wang, "An Analytic Three Terminal Band – to – Band Tunneling Model on GIDL in MOSFET", IEEE Trans. Electron Devices, vol. ED – 48, p. 1400, No 7, July 2001.

[14] L. Huang, P. T. Lai, J. P. Xu and Y. C. Cheng, "Mechanism Analysis of Gate – Induced – Drain – Leakage in Off State n-MOSFET"

[15] P. P. Wang, "Device Characteristics of Short – Channel and Narrow – Width MOSFET" IEEE Trans. Electron Devices, vol. ED – 25, p. 779, No 7, July 1978.

[16] Y. Tseng, W. M Huang, D. J. Monk. P. Welch, J. M. Ford, J. C. M. Woo, "AC Floating Body Effect and the Resultant Analog Circuit Issues in Submicron Floating Body and Body Grounded SOI MOSFETs", IEEE Trans. Electron Devices vol. 46, No. 8, August 1999, p. 1682 – 1685.
[17] Ali A. Orouji, Abdollah Abbasi, "Novel Partially Depleted SOI MOSFET for Suppression of Floating Body Effects: An Embedded JFET", Superlattices and Microstructures, vol. 52, Issue 3, Sept. 2012, pp. 552 – 559.
[18] Ali A. Orouji, Mohamed K. Anvarifard, "Novel Reduced Body Charge Technique in Reliable Nanoscale SOI MOSFET for suppressing", Superlattices and Microstructures, vol. 72, Aug. 2014, pp. 111 – 125.
[19] J. Luo, J. Chen, Q. Wu, Z Chai, J. Zhou, T. Yu, Y. Dong, L. Li, W. Liu. C. Qiu, X. Wang, " A Tunnel Diode Body Structure for High Performance SOI MOSFET", IEEE Trans. Electron Devices vol. 59, No. 1, Jan. – 2012, p. 101 – 107.
[20] H. Umezawa "Recent Advances in Diamond Power Semiconductor Devices", Mat. Sc. In Semiconductor Processing, vol. 78 (2018), pp. 147 – 156.
[21] J. Isberg, J. Hammersberg, E. Johansson, T. Wikstrom, D.J. Twitchen, A.J. Whitehead, S.E. Coe, G.A. Scarsbrook, "High Carrier Mobility in Single-Crystal Plasma-Deposited Diamond", Science 297 (2002) 1670–1672.
[22] E.A. Konorova, Y.A. Kuznetsov, V.F. Sergienko, S.D. Tkachenko, A.V. Tsikunov, A.V. Spitsyn, Y.Z. Danyushevskii, "Impact Ionization in Semiconductor Structures Made of Ion-Implanted Diamond", Sov. Phys. - Semicond. 17 (1983) 146–149.
[23] K. Ueda ∗, K. Kawamoto, H. Asano "High-Temperature and High-Voltage Characteristics of Cu/Diamond Schottky Diodes"