Design Of Low Power SRAM Cell with Improved Noise Margin Using Finfet

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Abstract*—This project aims to develop an SRAM cell that can achieve a high noise margin at low power consumption by using FinFETs. The conventional use of CMOS technology introduces challenges such as elevated leakage current, short channel effect (SCE), and substantial power dissipation, all of which significantly impact SRAM performance. Therefore, we propose the adoption of Gated FinFET-based SRAM cells with pass transistor feedback as an alternative to CMOS-based counterparts. This strategic shift aims to address issues associated with short-channel effects, enhance operational speed, diminish leakage, reduce power consumption, improve mobility, and facilitate efficient transistor scaling. The ultimate goal is to create faster SRAM cells operating at lower power levels with high noise margins, thereby advancing the overall performance of the SRAM system.

***Index Terms*—Static Random Access Memory (SRAM), FinFET, Static Noise Margin (SNM), MTCMOS (HVT, LVT), CMOS, Subthreshold region, Low power, Leakage current, N-curve**

I. INTRODUCTION

Static Random-Access Memory (SRAM) cells are crucial components in modern integrated circuits. They offer fast access times and high-speed data storage capabilities. With the increasing demand for low-power electronics and the proliferation of battery-operated devices, there is a growing need to design SRAM cells with reduced power consumption while maintaining high performance and reliability. Additionally, as semiconductor technology scales down to smaller feature sizes, SRAM cells face challenges such as increased susceptibility to noise and variability, which can degrade their stability and robustness.

In response to these challenges, this project aims to explore the design of SRAM cells with improved noise margin using FinFET technology. FinFETs, with their three-dimensional transistor architecture, offer enhanced electrostatic control and reduced leakage currents, making them well-suited for low-power applications. By leveraging the advantages of FinFETs, this project seeks to develop innovative SRAM cell designs that not only consume less power but also exhibit increased immunity to noise, ensuring reliable operation in diverse operating conditions.

II. LITERATURE SURVEY

A. FinFET Technology

The Researchers have long focused on overcoming Short Channel Effects (SCE) in nano-scaled CMOS devices, which include sub-threshold increases, threshold voltage variations, and punch-through between drain and source. Multi-gate devices have emerged as a solution, evolving from single-gate designs. Gate length reduction exacerbates SCEs, prompting strategies like thinning gate oxide and increasing channel doping. However, these methods can raise gate-to-channel capacitance and Gate Induced Drain Leakage (GIDL). FinFETs address these challenges by employing multiple gate electrodes and a thin, fully depleted semiconductor body. The FinFET's 3D structure consists of thin vertical "Fins" that provide exceptional gate control. Increasing device width or Fin count enhances current flow. Double-gate FinFETs, with front and back gates, reduce SCEs further by coupling gates electrically. IG-FinFETs, suitable for low-power applications, excel in reducing standby and leakage power.

B. SRAM Cells

The conventional 6T SRAM cell is made up of two cross-coupled inverters that are connected back-to-back. These inverters act as a latch, allowing complementary values to be stored at Q and QB, the output nodes. The bit lines BL and BLB are connected to the output storage nodes Q and QB through access transistors. During write and read operations, the word line (WL) activates these access transistors (M5 and M6). The conventional 6T SRAM cell has a fundamental drawback known as read destruction.

During a read operation, BL and BLB are supplied with a high voltage. The node that is at logic '0' allows the discharge of the corresponding bit line, which in turn charges the storage node. This activates the pull-down transistor of the other inverter pair, causing a change in the value on the other storage node.

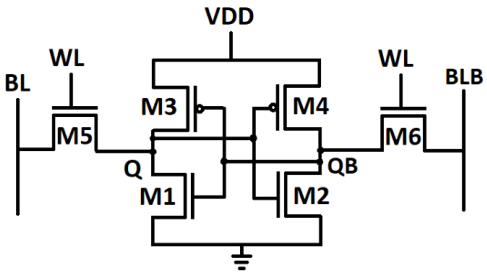

Fig. 1. Conventional 6T SRAM Cell

The Conventional 7T SRAM cell, consists of an additional transistor placed in the ground path of a 6T SRAM cell to reduce leakage while the cell is in standby mode. In the standby mode, the bottom transistor is intended to cut off the ground path and eliminate the leakage paths through the cross-coupled inverted from the supply voltage.

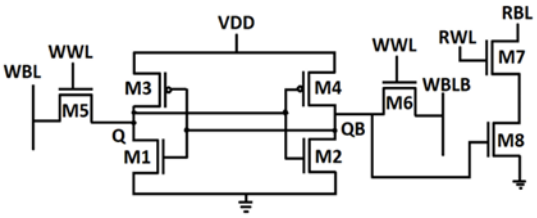

Fig. 2. Existing 8T SRAM Cell

The 8T SRAM was introduced to improve the read stability of previous SRAM cells. The above figure shows the structure of 8T SRAM cell. Due to a separate line for read and write operations the read stability was improved but more power is consumed.

III. PROPOSED 12T SRAM CELL

In our proposed 12T SRAM Cell architecture, we have implemented separate nodes for reading and writing operations, enhancing both stability and power efficiency. The design incorporates three pairs of inverters: M1&M2, M3&M4, and M7&M8. Inverters M1 and M3 function similarly to those in a traditional 6T SRAM Cell, acting as the memory storage element. However, we have introduced additional transistors, M5&M6, between these inverters. These transistors serve to disconnect the connection between the inverters during the reading operation, thereby improving stability and minimizing the risk of data corruption.

Furthermore, to optimize power consumption during writing operations, we have integrated M9&M10, which serve as gated ground logic. M9&M10 are strategically employed to minimize power loss during the writing process, ensuring efficient utilization of energy resources. Additionally, during idle periods, M9&M10 help to maintain power efficiency by controlling leakage currents and reducing standby power consumption.

Overall, the design of our 12T SRAM Cell leverages innovative circuit configurations to achieve improved stability, enhanced power efficiency, and robust operation, thereby advancing the state-of-the-art in SRAM cell architecture.

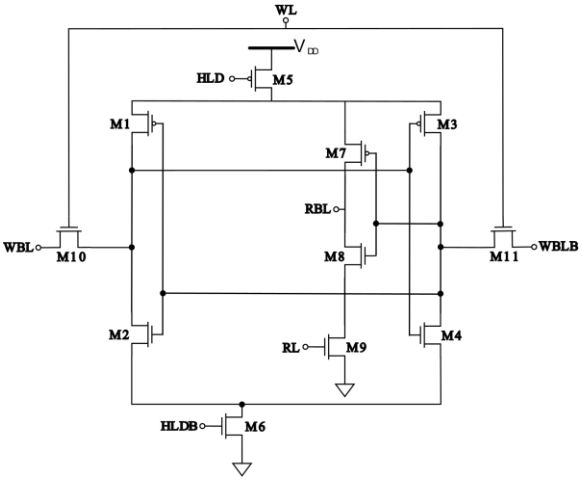

Fig. 3. Proposed 11T SRAM cell

During the read operation of logic 1, when node Q is at logic level 1, node $\bar{Q}$ is at logic level 0, the transistors M1 and M4 are turned on, while transistors M2 and M3 are turned off. When the read line (RL) is activated, it enables transistor M9. Given that $\bar{Q}$ is low, transistor M7 is enabled and transistor M8 is disabled. As a result, the read bit line (RBL) is pulled up by transistor M7. The exact complementary process happens for read operation logic 0.

During the write operation of logic 1, assuming node Q is at logic level 0, node $\bar{Q}$ is consequently at logic

level 1. In this state, transistors M1 and M4 are turned off, while transistors M2 and M3 are turned on. To write a logic 1, ground the WBLB and pull up the WBL to Vdd. When the WL is activated, it enables transistors M10 and M11. Thus the voltage at node $\bar{Q}$ will be low, which in turn disables M2 and enables M1, pulling up node Q. This action subsequently disables M3 and enables M4, which pulls down node $\bar{Q}$ to ground. The exact complementary process happens for write operation logic 0.

During the hold operation, the transistors M5 and M6 are turned on and the circuit is cut off from the power supply and ground. This allows us to reduce the static power dissipation.

IV. SIMULATION RESULTS

The conventional SRAM cell experiences lower stability and higher leakage current. The proposed 12T SRAM cell is proposed and analyzed in the previous section. The proposed 12T SRAM cell and the conventional 6T, 7T, and 8T SRAM cells were simulated using Cadence Virtuoso. All the simulations are carried out using the 18nm FinFET technology at a source voltage of 700mV. Multiple parameters such as Static Noise Margin (SNM), Transient analysis, and power analysis were simulated and obtained.

A. Transient Analysis

The transient analysis for the proposed SRAM cell was simulated for a time period of 60ns. All three operations of write, read, and hold were simulated for a period of 20ns each.

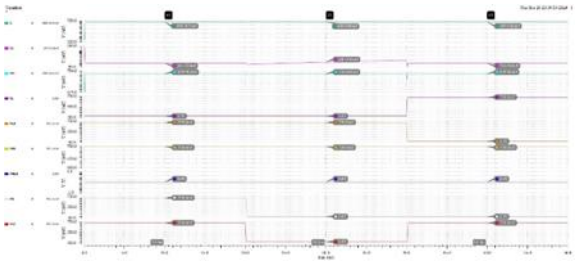

Fig.4 Transient Analysis for logic 1 at Vdd=0.7

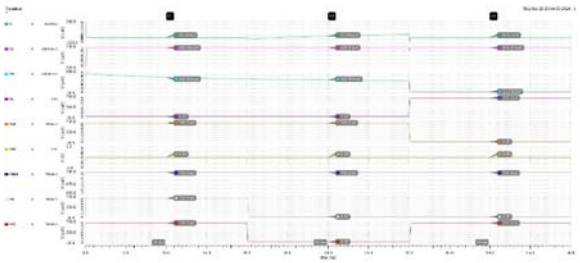

Fig.5 Transient Analysis for logic 0 at Vdd=0.7

Two simulations were performed, one for the write, read, and hold operation of logic 1, and the other for the write, hold, and read of logic0. The below figures show the transient analysis of logic 1 and zero respectively. Here RL, RLB, HLDB, and WL are control signals used for changing the mode of operation. Q, QB, and RBL represent the output lines.

Data Stored	Node	Operation Performed		
		Write (mV)	Hold (mV)	Read (mV)
Logic 0	Q	0.033	3.956	0.853
	Qb	699.9	699.94	699.94
Logic 1	Q	699.9	699.94	699.96
	Qb	0.034	2.123	0.781

Table 1. Transient analysis

The above table shows us the values of node voltages during read, write and hold operation. As it can be observed that the node voltages are approximately equal to the values of logic 1 and 0.

B. N-Curve Analysis

The N curve analysis is used to calculate the Static Noise Margins (SNM). The minimal amount of noise voltage necessary to flip the data stored on the storage nodes is known as the SNM of SRAM. N-curve is a plot of the voltage supply Vin enforced at the storage node Q versus the equivalent current Iin flowing through the source. The N-curve method is used to determine the static voltage noise margin (SVNM) of read and write for the SRAM cell.

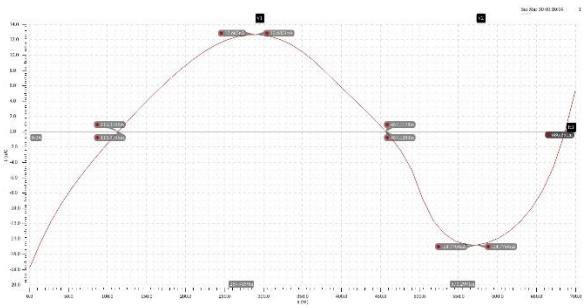

Fig.6 N-Curve Analysis for Vdd=0.7V

The N Curve analysis was performed on existing SRAM topologies to compare the performance of the existing and proposed SRAM cells. The results are tabulated above. From the tabular column, it can be observed that the proposed topology performs better in every aspect.

Vdd=0.7V	C6T	C7T	C8T	Proposed 12T SRAM Cell
SVNM (mV)	252.6	252.3	252.6	343.7
SINM (uA)	27.2	24.1	13.6	0.0127
WTV (mV)	343	257.3	334.4	229.7
WTI (uA)	9.3	5.9	4.6	0.0148
SPNM (uW)	6.8	6.0	3.4	0.0044
WTP (uW)	3.2	1.6	1.5	0.0034

Table 2. NCurve Analysis for Different Topologies

C. Transient Power Analysis

The transient power analysis was conducted over a 60ns period, with write, read, and hold operations each lasting 20ns. The figure below illustrates the Transient Power Analysis at a supply voltage of 0.7V. The peak power occurs precisely during the switch from one mode to another.

Supply Voltage (V)	Average power (nW)	Peak power (uW)
0.5	5.41	2.53
0.7	17.27	7.42
1	550.6	20.75

Table 3. Transient Power Analysis

The analysis was performed for supply voltages of 0.5V, 0.7V, and 1V, and the peak power and average power at each supply voltage were calculated. The average power was determined by averaging the results of the transient analysis plot. As anticipated, both the average power and peak power increase as the supply voltage rises.

V. CONCLUSION AND FUTURE SCOPE

In summary, the development of a low-power SRAM cell with improved noise margin using FinFET technology is a significant advancement in memory design. Our proposed design offers lower power consumption and enhances the reliability and performance of the SRAM system through improved noise margin. This innovation holds great promise for more energy-efficient and robust electronic devices in the future. Our proposed 12T SRAM cell demonstrated significant improvements in various aspects, such as read margin SVNM (increased by 104.54%, 104.76%, and 104.52%), write margin SINM (decreased by 90.58%, 89.36%, and 81.16%). Additionally, our proposed cell showed lower read power consumption (decreased by 80.73%, 78.22%, and 61.46%) and write power consumption (decreased by 88.2%, 76.95%, and 75.78%) compared to the conventional 6T SRAM cell, existing 7T, and existing 8T SRAM cell, respectively. Overall, the cell has better hold and write ability and good read and hold ability at sub-threshold voltages. Low-power cache memories and digital signal processors can be designed using the proposed 12T SRAM cell. As a further work, the body bias technique can be used and a cell array can be analyzed.

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