Study and Analysis of Universal Gates using different logic styles at CMOS Logic Style at 45nm Technology

SUBHODEEP SENGUPTA1, SAPTARSHI PRAMANIK[2], SAMBIT CHANDA[3], SWAGATA BHATTACHARYA[4]

[1, 2, 3, 4] *Electronics & Communication Engg., Guru Nanak Institute of Technology, Sodepur, India*

Abstract*— Research into the design and performance analysis of NAND and NOR gates using CMOS logic at 45nm technology is a captivating subject in the field of VLSI design. NAND and NOR gates because they are universal gates and they can form all basic gates (AND, OR, NOT, XOR, XNOR) and any logical Boolean expression can be implemented using only NAND gates or only NOR gates. The investigation involves the creation of two-input NAND and NOR gates using a variety of logic styles and the subsequent analysis of their performance in terms of average power consumption, average propagation delay, power-delay product, and transistor count. The technology employed is 45nm. The study offers an in-depth understanding of the workings of NAND and NOR gates. Additionally, the delay, rise time, and fall time are computed. The research findings indicate that the NAND gate has several advantages over the NOR gate, including lower static and dynamic power dissipation, smaller area requirement, reduced rise and fall times, and significantly lower delay. This knowledge equips engineers with the ability to develop increasingly sophisticated and efficient digital systems. By understanding these configurations, the abstract lays the groundwork for further exploration of complex digital circuits built upon these fundamental NAND and NOR gates. The construction and testing of NAND and NOR gates have been performed using Tanner EDA v15. An in-depth examination of delay and power for various logic styles of the NAND and NOR gate has been conducted. Additionally, a comprehensive Process, Voltage, Temperature (PVT) analysis has been executed for the circuits.

Index Terms- CMOS logic, PVT analysis, 45nm technology, universal gates, pseudo NMOS

I. INTRODUCTION

CMOS technology is widely used in IC design for its low power consumption and high noise immunity. NAND and NOR gates are fundamental to digital circuits and are commonly implemented using CMOS logic. This study analyses NAND and NOR gates using different CMOS styles at 45nm, a leading-edge technology node.

NAND and NOR gates are vital in digital logic, forming the basis for complex circuits like flip-flops and ALUs. This research aims to understand their behaviour, performance, power consumption, and area utilization. [1]

Using CMOS technology with NMOS and PMOS transistors, NAND and NOR gates achieve low power dissipation and high noise margins. The study will investigate:

1. Power consumption under various conditions.
2. Delay and propagation characteristics for speed analysis.
3. Noise immunity against glitches and crosstalk.
4. Performance trade-offs for optimal design choices.

By studying NAND and NOR gates in CMOS logic at 45nm, this research contributes to advancing digital circuit design for applications like microprocessors and communication interfaces.

In addition, we used NAND and NOR gates because they are universal gates and they can form all basic gates (AND, OR, NOT, XOR, XNOR) and any logical Boolean expression can be implemented using only NAND gates or only NOR gates. This universality, combined with their economical and easier fabrication compared to other logic gates, greatly simplifies the process of creating any circuit. As long we can construct a single type of gate many times using the same technique, and by connecting them logically, we can design and implement any circuit.

II. NAND OR NOR GATE USING CMOS

CMOS (Complementary Metal-Oxide-Semiconductor) technology is a fundamental building block in modern electronics, particularly in integrated circuits and microprocessors. Its significance lies in its low power consumption, high noise immunity, and scalability. In CMOS circuits, transistors are composed of both p-type and n-type semiconductor materials, creating a complementary pair that allows for efficient switching and minimal power dissipation. This characteristic makes CMOS ideal for portable devices, where power efficiency is crucial. Additionally, CMOS technology enables the integration of millions to billions of transistors on a single chip, facilitating the development of increasingly powerful and compact electronic devices [2]. Its versatility extends beyond microprocessors, encompassing memory chips, sensors, and various digital and analog circuits. With ongoing advancements, CMOS continues to drive innovation across a wide range of industries, from consumer electronics to healthcare and beyond, shaping the landscape of modern technology. [3]

A. NAND GATE Using CMOS

A NAND gate in CMOS technology is constructed by placing two NMOS transistors in series and two PMOS transistors in parallel between the power supply (v_{dd}) and ground (GND). The inputs are connected to the gates of these transistors, and the output is obtained from the connection point of the NMOS and PMOS transistors. [4][5]

Here's how it works for different input combinations:

1. Case 1: Both Inputs are Low (0, 0): In this scenario, both PMOS transistors are activated (ON) and NMOS transistors are deactivated (OFF). The output is linked to v_{dd} through the activated PMOS transistors and is charged to the v_{dd}level, leading to a high output.
2. Case 2: One Input is High and the Other is Low (0,1 or 1,0): The PMOS transistor corresponding to the Low input and the NMOS transistor corresponding to the High input are activated (ON). The output is linked to v_{dd} through the activated PMOS transistor and is charged to the v_{dd} level, leading to a high output.
3. Case 3: Both Inputs are High (1, 1): In this situation, both NMOS transistors are activated (ON), and the PMOS transistors are deactivated (OFF). The output is linked to GND through the activated NMOS transistors and is discharged to the GND level, leading to a low output.

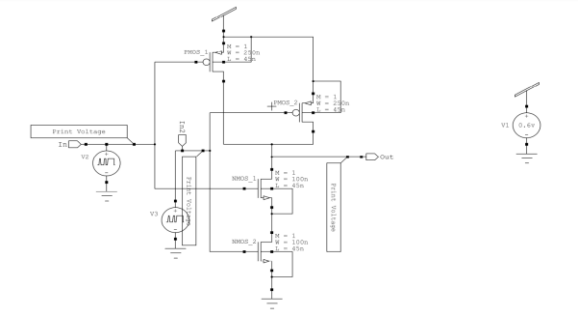


Figure 1. Circuit Diagram

a. *NMOS:* W = 0.100u L= 0.045u Temp = 25°C, 50°C, 100°C V= 0.6v, 0.45v, 0.5v
b. *PMOS*: W = 0.250u L= 0.045u Temp = 25°C, 50°C, 100°C V= 0.6v, 0.45v, 0.5v

TABLE I. NAND GATE USING CMOS RESULT ANALYSIS

Process		Voltage (v)	Temperature (°c)	Delay(ps)	Power(w)		
NMOS	PMOS				MIN	MAX	AVG
Nominal	Nominal	0.6V	25	t1 = -211.3841	0.000000e+000	2.006857e-008	8.592539e-011
			50	t1 = -355.6756	0.000000e+000	2.006857e-008	8.800290e-011
			100	t1 = -448.0746	0.000000e+000	2.107264e-008	9.056046e-011
Nominal	Nominal	0.45	25	t1 = -211.3841	0.000000e+000	1.953663e-008	8.592539e-011
			50	t1 = -355.6756	0.000000e+000	2.006857e-008	8.800290e-011
			100	t1 = -211.3841	0.000000e+000	2.107264e-008	5.169253e-010
Nominal	Nominal	0.5	25	t1=247.0399	5.736268e-010	1.204477e-005	1.502381e-007
			50	t1=248.7475	7.864857e-010	1.070765e-005	1.471604e-007
			100	t1=252.7294	1.670649e-009	9.027192e-006	1.541962e-007

Table Analysis - Upon examining Table 1, it is observed that the least power is achievable only at 0.5 V, while at 0.6 and 0.45 V, the power drops to 0V. Additionally, the maximum delay is noticed at 0.5 V.

Simulation Result: NAND GATE USING CMOS

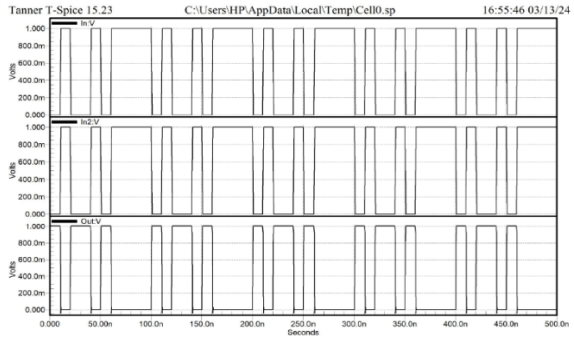


TABLE II. RISE AND FALL TIME OF INPUT IN CMOS NAND LOGIC

Voltage (v)	Input 1		Input 2	
	Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)
0.6v	20.10	20.90	10.10	10.90
0.45V	10.10	10.90	10.10	10.90
0.5V	10.10	10.90	10.10	10.90

TABLE III. RISE AND FALL TIME OF OUTPUT IN CMOS NAND LOGIC

Voltage (v)	Output	
	Rise(ns)	Fall(ns)
0.6v	30.59	31.09
0.45V	20.10	20.60
0.5V	10.10	10.60

B. NOR GATE Using CMOS

In CMOS technology, a NOR gate can be constructed by arranging two NMOS transistors in a parallel configuration and two PMOS transistors in a series configuration between the power supply (v_{dd}) and Ground (GND). The inputs are connected to the gates of both the NMOS and PMOS transistors. The output is derived from the junction between the NMOS and PMOS transistors. [5][6]

The operation of the NOR gate for different input combinations is as follows:

1. Case 1: Both Inputs are Low (0,0): In this case, both PMOS transistors are activated (ON) and NMOS transistors are deactivated (OFF). The output is connected to v_{dd} through the activated PMOS transistors and is charged to the v_{dd}level, resulting in a high output.
2. Case 2: One Input is High and the Other is Low (0,1 or 1,0): The PMOS transistor corresponding to the High input and the NMOS transistor corresponding to the Low input are deactivated (OFF). The output is connected to GND through the activated NMOS transistor and is discharged to the GND level, resulting in a Low output.
3. Case 3: Both Inputs are High (1, 1): In this case, both NMOS transistors are activated (ON) and PMOS transistors are deactivated (OFF). The output is connected to GND through the activated NMOS transistors and is discharged to the GND level, resulting in a Low output.

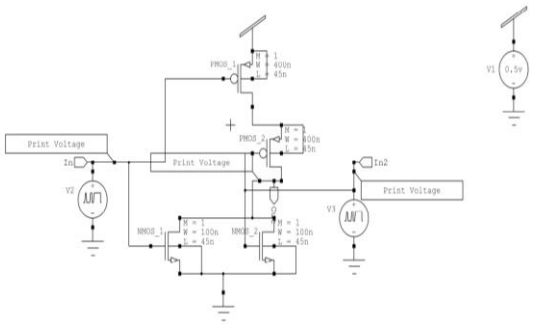


Figure 2. Circuit Diagram

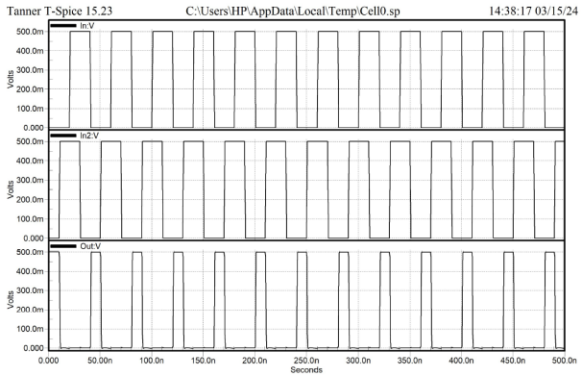
a. *NMOS:* W = 0.100u L= 0.045u Temp = 10°C, 20°C, 30°C, 50°C, 60°C, 70°C V= 0.5v, 0.7v, 0.62v
b. *PMOS*: W = 0.400u L= 0.045u Temp = 10°C, 20°C, 30°C, 50°C, 60°C, 70°C V= 0.5v, 0.7v, 0.62v

TABLE IV. NOR GATE USING CMOS RESULT ANALYSIS

Process		Voltage (v)	Temperature (°c)	Delay(ps)	Power(w)		
NMOS	PMOS				MIN	MAX	AVG
Nominal	Nominal	0.5	10	t1 = 50.22327	0.000000e+000	2.239786e-007	3.092061e-009
			20	t1 = 53.2197	0.000000e+000	2.213539e-007	3.084895e-009
			30	t1 = 56.0205	0.000000e+000	2.204718e-007	3.082519e-009
			50	t1 = 232.4608	0.000000e+000	2.082325e-007	3.054904e-009
			60	t1 = 65.5923	0.000000e+000	2.151566e-007	3.069993e-009
			70	t1 = 68.4074	0.000000e+000	2.136710e-007	3.069210e-009
Nominal	Nominal	0.7	10	t1 = 500.3841	0.000000e+000	3.426640e-007	3.091736e-009
			20	t1 = 670.6756	0.000000e+000	3.395306e-007	3.142463e-009
			30	t1 = 692.0746	0.000000e+000	3.367644e-007	3.192657e-009
			50	t1 = 774.0746	0.000000e+000	3.309740e-007	3.292842e-009
			60	t1 = 792.0746	0.000000e+000	3.275112e-007	3.370432e-009
			70	t1 = 812.0746	0.000000e+000	3.244694e-007	3.283050e-009
Nominal	Nominal	0.62	10	t1 = -774.0746	0.000000e+000	2.586699e-007	2.959776e-009
			20	t1 = -792.0746	0.000000e+000	2.560497e-007	2.995115e-009
			30	t1 = -670.6756	0.000000e+000	2.534883e-007	3.030049e-009
			50	t1 = -812.0746	0.000000e+000	2.485573e-007	3.098773e-009
			60	t1 = -692.0746	0.000000e+000	2.461959e-007	3.132219e-009
			70	t1 = -812.0746	0.000000e+000	2.439096e-007	3.164390e-009

Table Analysis - When scrutinizing Table 3, it's noted that the maximum delay occurs at 0.7 V at a temperature of 70°C. Regardless of the voltage values provided, the power remains constant at 0W. Furthermore, the power peaks at 0.7 V.

Simulation Result: NOR GATE USING CMOS



Upon comparing Tables 1 and 3, we can make the following observations:

i. The delay for the NAND Gate peaks at 0.5 V, whereas for the NOR Gate, it peaks at 0.7 V.
ii. The maximum power for the NAND Gate is achieved at 0.5V, while for the NOR Gate, it's achieved at 0.7V.

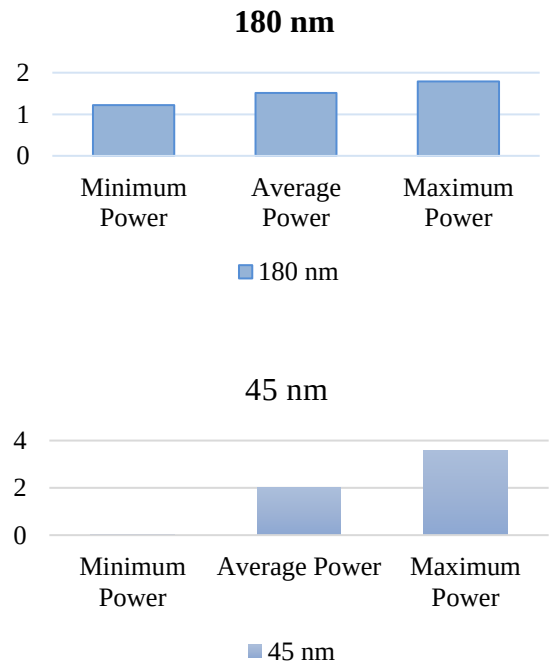
TABLE V. RISE AND FALL TIME OF INPUT IN CMOS NOR LOGIC

Voltage (v)	Input 1		Input 2	
	Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)
0.5	20.10	20.90	10.10	10.90
0.7	10.10	10.90	10.10	10.90
0.62	10.10	10.90	10.10	10.90

TABLE VI. RISE AND FALL TIME OF OUTPUT IN CMOS NOR LOGIC

Voltage (v)	Output	
	Rise(ns)	Fall(ns)
0.5	40.56	41.23
0.7	40.36	41.03
0.62	40.56	41.23

Graph - Comparison between the Power Analysis of 180nm and 45 nm CMOS



Analysis Using Pseudo NMOS

Pseudo-NMOS, a type of N-channel Metal-Oxide-Semiconductor, is a logic family that was commonly

used in the early stages of integrated circuit design due to its straightforward structure and low power usage. It utilizes a single N-channel MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) to perform both pull-up and pull-down operations, unlike the complementary CMOS (Complementary Metal-Oxide-Semiconductor) which necessitates the use of both N and P-channel transistors. [7]

In the case of a pseudo-NMOS inverter, the N-channel MOSFET serves as a switch that toggles between the output node and ground. If the input is high, the transistor is deactivated, which allows the output to be pulled up to Add via a resistor, yielding a low output. On the other hand, if the input is low, the transistor is activated, linking the output to ground, which pulls it down and results in a high output.

Despite the simplicity and efficiency of pseudo-NMOS for certain applications, it has limitations such as static power dissipation due to the resistor connected to v_{dd} and a restricted noise margin compared to CMOS, which limits its application in contemporary high-performance circuits. [8][9]

A. NAND GATE Using Pseudo NMOS

A Pseudo NMOS logic-based NAND gate can be constructed by arranging two NMOS transistors in a series configuration and a single PMOS transistor as a load. The inputs are connected to the gates of the NMOS transistors, while the gate of the PMOS transistor is connected to ground. [7][12]

The functioning of the Pseudo NMOS NAND gate for various input combinations is as follows:

1. Case 1: Both Inputs are Low (0,0): In this case, both NMOS transistors are deactivated (OFF), and the PMOS transistor is activated (ON). The output is connected to v_{dd} through the activated PMOS transistor and is charged to the v_{dd} level, yielding a high output.
2. Case 2: One Input is High and the Other is Low (0,1 or 1,0): The NMOS transistor corresponding to the High input is activated (ON), and the other NMOS transistor is deactivated (OFF). The PMOS transistor is also activated (ON). The output is connected to both v_{dd} and GND. However, since the PMOS transistor is less conductive when activated compared to the NMOS transistor, the output is pulled down to the GND level, yielding a Low output.
3. Case 3: Both Inputs are High (1,1): In this case, both NMOS transistors are activated (ON), and the PMOS transistor is activated (ON). The output is connected to GND through the activated NMOS transistors and is discharged to the GND level, yielding a Low output.

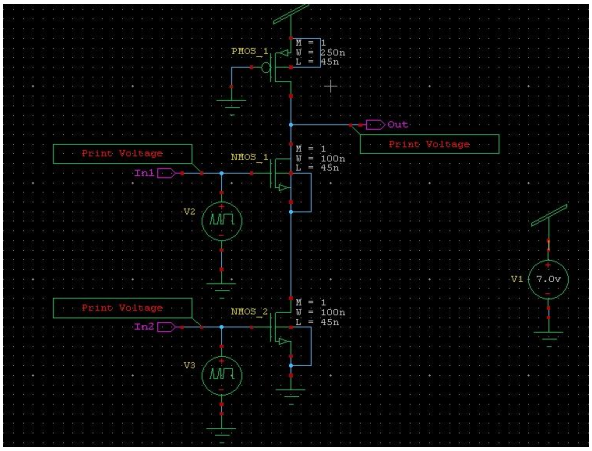


Figure 3. Circuit Diagram

a. *NMOS:* W = 0.100u L= 0.045u Temp = 10°C, 20°C, 30°C, 50°C, 60°C, 70°C V= 0.7v
b. *PMOS*: W = 0.250u L= 0.045u Temp = 10°C, 20°C, 30°C, 50°C, 60°C, 70°C V= 0.7v

TABLE VII. NAND GATE USING PSEUDO NMOS RESULT ANALYSIS

Process		Voltage (v)	Temperature (°c)	Delay(ps)	Power(w)		
NMOS	PMOS				MIN	MAX	AVG
Nominal	Nominal	0.7	10	t1 = -211.3841	0.000000e+000	7.947129e-007	1.754758e-007
			20	t1 = -355.6756	0.000000e+000	6.560053e-007	1.438867e-007
			30	t1 = -448.0746	0.000000e+000	5.489363e-007	1.196032e-007
			50	t1 = -211.3841	0.000000e+000	3.978899e-007	8.544739e-008
			60	t1 = -448.0746	0.000000e+000	3.435956e-007	7.317307e-008
			70	t1 = -355.6756	0.000000e+000	2.989764e-007	1.248960e-008

Simulation Result: NAND GATE USING PSEUDO NMOS

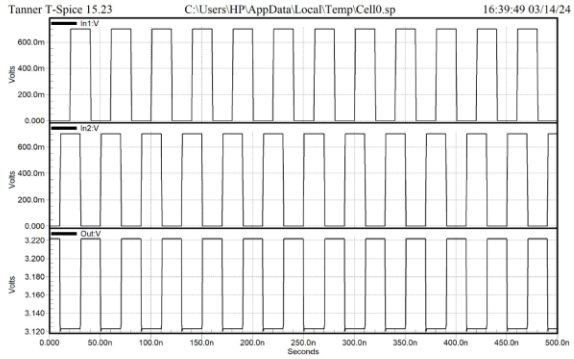


TABLE VIII. RISE AND FALL OF INPUT OF NAND GATE USING PSEUDO NMOS

Voltage (v)	Input 1		Input 2	
	Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)
0.7	20.10	20.90	10.10	10.90

TABLE IX. RISE AND FALL OF OUTPUT OF NAND GATE USING PSEUDO NMOS

Voltage (v)	Output	
	Rise(ns)	Fall(ns)
0.6v	25.59	25.09

B. NOR GATE Using Pseudo NMOS

A NOR gate, when designed using Pseudo NMOS logic, consists of two NMOS transistors configured in parallel and a single PMOS transistor acting as a load. The gates of the NMOS transistors are linked to the inputs, while the gate of the PMOS transistor is grounded. [10][12]

The operation of this Pseudo NMOS NOR gate for various input combinations can be described as follows:

1. Case 1: Both Inputs are Low (0,0): Here, both NMOS transistors are in an inactive state (OFF), and the PMOS transistor is in an active state (ON). The output is linked to v_{dd} through the active PMOS transistor and is charged to the v_{dd} level, leading to a high output.
2. Case 2: One Input is High and the Other is Low (0,1 or 1,0): The NMOS transistor corresponding to the High input is active (ON), and the other NMOS transistor is inactive (OFF). The PMOS transistor is also active (ON). The output is linked to both v_{dd} and GND. However, since the PMOS transistor is less conductive when active compared to the NMOS transistor, the output is pulled down to the GND level, leading to a Low output. [11]
3. Case 3: Both Inputs are High (1, 1): In this situation, both NMOS transistors are active (ON), and the PMOS transistor is also active (ON). The output is linked to GND through the active NMOS transistors and is discharged to the GND level, leading to a Low output.

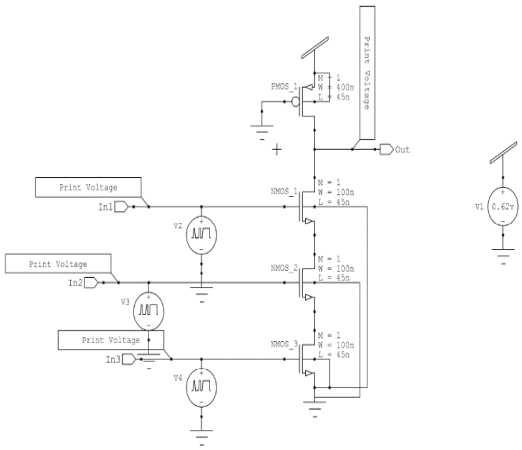


Figure 4. Circuit Diagram

a. *NMOS:* W = 0.100u L= 0.045u Temp = 10°C, 20°C, 30°C, 50°C, 60°C, 70°C V= 0.62v
b. *PMOS*: W = 0.400u L= 0.045u Temp = 10°C, 20°C, 30°C, 50°C, 60°C, 70°C V= 0.62v

TABLE X. NOR GATE USING PSEUDO NMOS RESULT ANALYSIS

Process		Voltage (v)	Temperature (°c)	Delay(ps)	Power(w)		
NMOS	PMOS				MIN	MAX	AVG
Nominal	Nominal	0.62	10	t1 = -448.0746	2.092251e-011	7.132621e-006	1.526959e-006
			20	t1 = -211.3841	2.043056e-011	6.762231e-006	2.423325e-007
			30	t1 = -355.6756	1.989751e-011	6.060868e-006	1.380758e-006
			50	t1 = -211.3841	1.873092e-011	5.773936e-006	2.079975e-007
			60	t1 = -448.0746	2.099437e-011	5.483544e-006	1.183955e-006
			70	t1 = -355.6756	2.071191e-011	5.211324e-006	1.128086e-006

Simulation Result: NOR GATE USING Pseudo NMOS

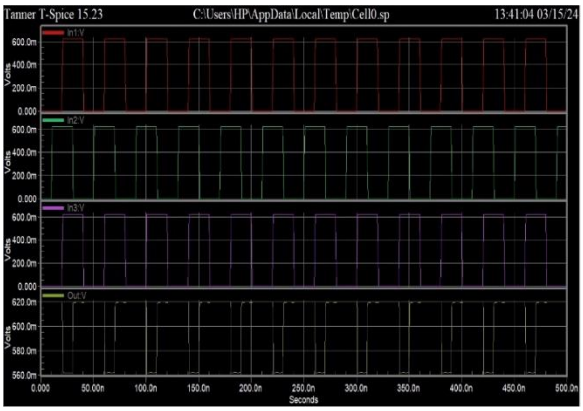


Table Analysis - Upon analyzing Tables 7 and 10, we observe that:

i. The peak power for the NAND Gate is achieved at 0.7 V when the temperature is 10°C, while for the NOR Gate, it's achieved at 0.62V under the same temperature conditions.
ii. The NOR Gate exhibits a higher minimum power compared to the NAND Gate.

TABLE XI. RISE AND FALL OF INPUT OF NOR GATE USING PSEUDO NMOS

Voltage (v)	Input 1		Input 2		Input 3	
	Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)
0.62	20.10	20.90	10.10	10.90	20.10	20.90

TABLE XII. RISE AND FALL OF OUTPUT OF NOR GATE USING PSEUDO NMOS

Voltage (v)	Output	
	Rise(ns)	Fall(ns)
0.62	30.09	30.59

CONCLUSION

The exploration into the application of CMOS logic with NAND and NOR gates in the realm of 45nm technology underscores the pivotal role these gates play in the landscape of digital circuit design. By scrutinizing the performance metrics of these gates, the study unveiled notable benefits associated with NAND gates, such as decreased power usage, compact spatial demand, and diminished latency in contrast to NOR gates. This comprehension serves as a cornerstone for enhancing the efficacy of digital systems, providing a solid foundation for the intricate design of circuits. The juxtaposition of various logic styles and technological approaches illuminates pathways for streamlining digital circuits concerning power efficiency, operational speed, and overall efficacy, fostering progress in VLSI design and the realm of microprocessor functionalities.

ACKNOWLEDGMENT

We would like to express our deepest appreciation to the DSP & VLSI Laboratory, ECE Department, GNIT. The laboratory played a crucial role in the success of our research. The resources and facilities provided by the laboratory significantly contributed to the completion of our work. We are truly grateful towards it.

We are immensely thankful for the unwavering support and dedication of the laboratory staff. Special thanks to (prof.) Sulata Pandit and (prof.) Dyuti Nandi, whose assistance and insights were greatly appreciated and significantly enhanced our research experience.

REFERENCES

To complete this paper we took reference from:

[1] M. Morris Mano, "Digital Design", Pearson Education, 5th Edition, 2012.J.

[2] "CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H.E. Weste and David Money Harris.

[3] "CMOS Technology for Analog and RF Integrated Circuits" by P.R. Gray et al., published in the IEEE Journal of Solid-State Circuits.

[4] Sung-Mo Kang, Yusuf Leblebici. “CMOS DigitalIntegrated Circuits (Analysis and Design),” 3rd edition, Tata McGraw-Hill.

[5] https://www.researchgate.net/publication/316548029_Analysis_of_CMOS_based_NAND_and_NOR_Gates_at_45_nm_Technology

[6] David A Hodges, Resve Saleh, Horace G. Jackson,“Analysis and Design of Digital Integrated Circuits,” 3rd Edition, McGraw Hill.

[7] "Digital Integrated Circuits: A Design Perspective" by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolić.

[8] "A low-power 4-bit CMOS full adder for portable applications" by A. H. M. Zahirul Alam et al.

[9] "Design and analysis of low power pseudo NMOS logic circuits" by Kamalakanta Mahapatra and Saraju P. Mohanty.

[10] "Essentials of Electronic Design" by Douglas A. Pucknell and Kamran Eshraghian.

[11] "CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H.E. Weste and David Harris.

[12] https://www.iue.tuwien.ac.at/phd-theses