The Adaptive Neuro Fuzzy Inference System Based Controller for UPFC Using 7 Level Casaded H Bridge (CHB) Inverters For Decreasing The Settling Time Of Power Wave Post Fault Conditions In Transmission Lines - A Comparison With Pi Controller

T. JAGANMOHANRAJU[1], PROF. G.TULASI RAM DAS[2]
[1] *Assistant Professor of EEE, Kakatiya University*
[2] *Professor of EEE, JNTUH Hyderabad*

Abstract – Advanced Computing Techniques and Control Strategies, in the field of Electrical Engineering, have gained great importance over the conventional computing and controlling techniques in the past few years. One such Advanced Computing and Controlling Technique is the ANFIS (Adaptive Neuro Fuzzy Inference System).In brief it's an intellectual combination of Fuzzy Logic System and the Artificial Neural Networks. ANFIS Controllers designed to deal with. Non Linear systems have proved to be very effective over the PI controllers. Unified Power Flow Controllers are very much known for their versatality in independently controlling the Active and Reactive Power Flow in a transmission line[1] This paper proposes a unique combination of Advanced MLIs like Cascaded H Bridge Inverters in the Converters of UPFCs and an Advanced Control Strategy ANFIS and Conventional Controller like PI CONTROLLERS for Alleviating the Performance Capabilities of UPFCs. This paper presents the detailed results showing the Improvement in Performance Capabilities of UPFC using the Proposed New Combination of CHB Inverters with ANFIS Controller over the PI Controller. The Performance of UPFC with a 7 Level CHB Inverter based UPFC and 7 a Level CHB based Inverter are analysed. The test is carried out on a Standard IEEE 5 Bus System. Different Shunt Faults like LG (on Phase A) , LL (on Phases A-B) , LLG (on Phases A - B - Ground) and LLL (on Phases A-B-C) are created at bus number 4 , Between bus 3-4 , and the capability of the ANFIS Controller based UPFC over the PI Controller based UPFC in restoring the system normalcy is also tested. The parameters used for analysing the controller's performance are Transient Overshoot Control and Settling Time. The PWM Technique used is Sine Triangle PWM (SPWM). Simulations pertaining to the entire test procedures are done using MATLAB software.

Index Terms – AC Transmission, FACTS, UPFC, ANFIS, PI Controllers, IEEE-5 BUS System, Shunt Line Fault, Power Flow Control, Cascaded H Bridge (CHB) Inverters, SPWM, Rise Time, Transient Overshoot, Settling Time.

I. INTRODUCTION

The Unified Power Flow Controllers were basically proposed for real time control and dynamic compensation of the ac transmission system parameters and for obtaining more flexibility in solving the problems faced by the Utilities. An earnest effort towards achieving the above goals is made here especially to improve the sensitivity of the device, the quality of output of the device, the response time of the device and also the controllability of the device by making the device to act like a self-thinking machine. The Unified Power Flow Controller has two converters, one a shunt converter (converter 1), connected in shunt with the transmission network and other a series converter (converter 2) , connected in series with the Transmission Network These two converters are connected to each other by a common DC link capacitor. The presence of a common DC link enables the transfer of real and reactive power to flow between the two converters thereby enabling the absorption and injection of voltages and currents from and to the transmission network respectively. Each of the converters can independently generate and absorb real and reactive power at their respective ac terminals. The basic function of the Shunt converter (converter 1) is to supply the real power it can also supply or absorb reactive power. The series converter (Converter 2) provides the main function of the UPFC by injecting an ac voltage of requisite magnitude Vpq ($0 \leq Vpq \leq Vpqmax$) and phase angle δ ($0 \leq \delta \leq \delta$ max) at power frequency in series with the transmission line voltage.

II. UPFC FUNDAMENTAL CONFIGURATION

Terminal Voltage Regulation is done with UPFCs wherein the required voltage of change required on the Transmission line say, ΔV (Vinj) , is injected either in-

phase or in anti-phase mode with the existing voltage Vo on the Transmission line.

Series Capacitive Compensation is done where the required value of voltage say, Vinj, is injected in Quadrature with the Line Current.

Phase Shifting or Transmission Angle Regulation is done by injecting a voltage of Vinj in an angular relationship with Vo to get the required Phase Shift (Advanced or Retarded) in the Line output voltage without change in the Magnitude of the Line output voltage.

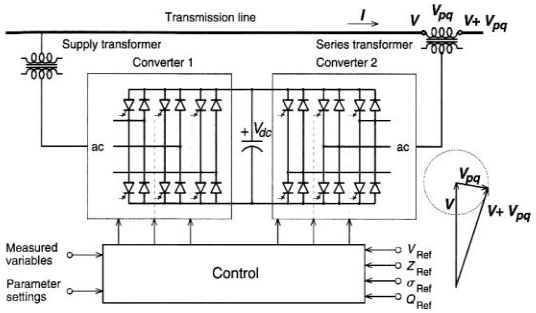
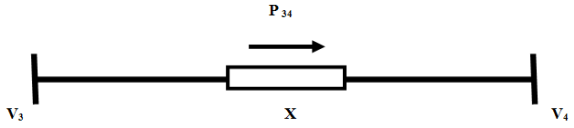


Figure 1. Detailed Circuits of UPFC showing Converters and Controller connections

POWER FLOW EQUATIONs OF UPFC CONNECTED BETWEEN THE BUSES 3 and 4



$$P = \frac{V^2}{X}\ Sin(\delta)$$

$$Q = \frac{V^2}{X}\ (1 - Cos(\delta))$$

Figure 2. Power Flow Between Buses 3 and 4 of the IEEE 5 Bus System

$$P = \frac{V^2}{X}\ Sin(\delta)$$

$$Q = \frac{V^2}{X}\ (1 - Cos(\delta))$$

Multi-Function Power Flow Control is obtained by simultaneously regulating the terminal voltage, series capacitive compensation and Phase Shifting action.

$$Vpq = \Delta V + Vc + V\sigma \qquad (1)$$

In the explanation that follows, the importance of using the PI Controllers in UPFC to enhance the Controlling Capabilities of UPFC are clearly explained. The UPFC incorporating a 7 Level CHB Inverter and a PI controller is tested for its improved performance on a Standard IEEE –5 Bus System. The UPFC is connected in the system between Bus number 3 and 4. The test conditions include conditions Transient Stability Enhancement Capabilities when the IEEE-5 Bus system is subjected to different Shunt Faults like LG,LL,LLG and LLL Faults. The PI controllers are best known to be the fundamental Controllers in restoring Normalcy on a Power System Network. The immediate changes in the network conditions more importantly at the point of connection of the UPFC are detected and Appropriate Corrective Actions are initiated by the PI Controllers. The UPFC Simulated in this paper mainly consists of a Cascaded H Bridge Inverter. The Advantage with the CHB Inverters is made use of in improvising the Performance of the UPFC there by Improving the Protection Levels offered to the Power System Network when the Power System is subjected to Certain Adverse and Abnormal Conditions. One of the most widely used software MATLAB is used for simulating the said test conditions.

- The Cascaded H Bridge Inverter

One of the outcomes of the Research on the attempt to improvising the Output Voltage of an Inverter through Modifying Network/Circuit configurations of an Inverter is the Cascaded H Bridge (CHB) Inverter. The low switching voltage stress and modularity has made the Multi Level Inverters (MLIs) gain more attention. The user desired Multi Level voltage is obtained by using different and separate voltage sources like Batteries, Fuel cells, Solar Photo Voltaic (PV) Cells, Capacitors etc., The major Advantages with Multi Level Inverters are their Minimum Harmonic Distortions in the Output Voltage, Low Electro Magnetic Emissions, High output to Input Ratios i.e., High Efficiency and More Importantly their High Voltage With Standing and Operating Capability and Modularity. The Multi Level Inverters have found great applications in the areas of Drive Controls, Uninterruptible Power Suppliers and Static Volt Ampere Reactive Generators (SVG).In general MLIs are divided in to three categories as Diode Clamped, Flying Capacitor and Cascaded Bridge Inverters. One of the advantages of MLIs over the Two Level Inverter is that they reduce the Common Mode Voltage causing the breaking leakage Current in Multi Drive Systems of High Power Ratings (Greater Than 250KW) based Vehicles.

The Circuit Topology of Cascaded H Bridge Inverter

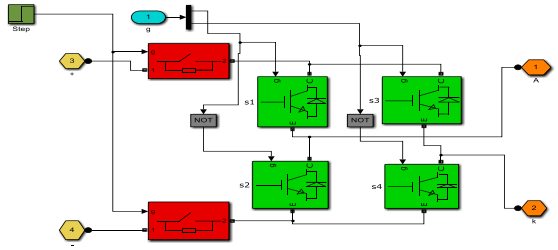


Figure 3.Basic Circuit of CHB Inverter used in this Simulation

The Fourier Series Output Voltage equation of the CHB Inverter (i.e., for a staircase waveform) is given by

$$V(wt) = \left(\frac{4\,Vdc}{\pi}\sum_{n=1,2,3\ldots}^{\infty}(\cos n\alpha 1 + \cos n\alpha 2 + \cos n\alpha 3 + \cdots . \cos n\alpha s)\sin nwt\right) \quad (3)$$

Where

α = the switching angle
n = harmonic number,
Vdc = DC Supply Voltage of the Inverter
s = number of switching angles

Here the value of V(wt) is Considered as = Vinj ∟Θinj For a given desired output fundamental voltage V (wt) it is required to find the switching angles α1, α2, α3.... αs in such a way that he total harmonic distortion is minimized.

The Magnitude of the Fundamental Waveform can be controlled by balancing the ratio of V and Vdc i.e., V/Vdc

The above ratio is called the Modulation Index denoted by M

Therefore

$$M = \frac{Vinj}{Vdc} \quad (4)$$

Where Vinj is the Maximum Value of the Inverters Fundamental Voltage, the Series Injected Voltage

From Eqn 2 , V1 is the voltage output of the first H Bridge H1, and so on till Vn which is the output of the n^{th} cell Hn. In the initial stages each of the cells are supplied by individual DC sources later on it is experimentally shown that it is sufficient to have one of the cells fixed with a real DC source and the remaining can be supplied with capacitors. The change in redundancy in changing the sources is discussed in Jingsheng Liao in his paper CHB a re-examination. In this paper a Seven Level CHB Inverter is used in the Series Converter of the UPFC. The operation of the Seven Level CHB is explained in brief in the following session. The user specified output voltage of the CHB Inverter will be the Voltage that will be Injected through the Series transformer of the UPFC.

The number of Voltage Steps or Levels that could be obtained by cascading X number of cells i.e., H Bridges is given by

$$N_{volt} = 2X+1$$

The Number of Levels of Voltages N_{volt} in case of CHB Inverters is always an Odd Number. Where as in case of Diode Clamped inverters it can be either even or odd.

The Total Number of Active Switches in a Cascaded H Bridge Inverter can be obtained from the following formulae

$$N_{act} = 6*(N_{volt} - 1)$$

In the Equation for Solution for Transfer of Power through the lines 3 and 4 , the magnitude of voltage and the corresponding phase angle at which it is to be injected in Series by the UPFC's Series device is calculated using the Newton Raphson Solution Method. The values thus calculated by the controller are generated using the UPFCs Converters .The Series Converter which consists of the Three Level Cascaded H Bridge Inverter plays a major role in producing the voltage of desired magnitude and phase angle i.e., Vinj ∟Θinj . To Control the values of Voltage and Power Transferred on the transmission line we can control the values of Vinj ∟Θinj i.e., we can control the magnitude of Vinj alone ,Phase Angle ∟Θinj alone or by simultaneously changing the values of Vinj and ∟Θinj .

The Adaptive Neuro Fuzzy Infrence System (ANFIS)

An Adaptive Neuro - Fuzzy Inference System or Adaptive Network-based Fuzzy Inference System (ANFIS) is a kind of artificial neural network that is based on Takagi–Sugeno fuzzy inference system. Since it integrates both neural networks and fuzzy logic principles, it has potential to capture the benefits of both in a single framework. Its inference system corresponds to a set of fuzzy IF–THEN rules that have learning capability to approximate nonlinear functions. Hence, ANFIS is considered to be a universal estimator ([1].

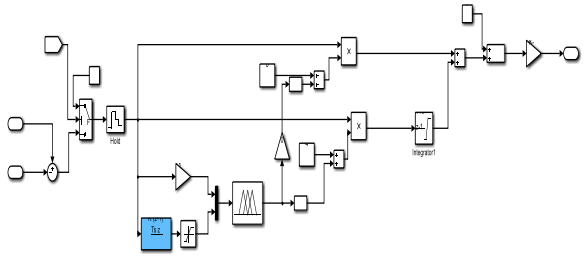


Figure.4 The ANFIS Controller Used in this Simulation

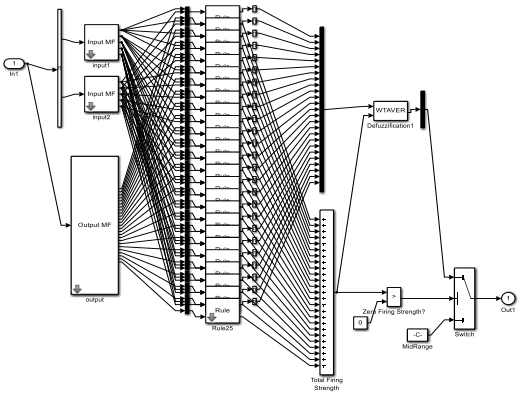


Figure.5 The Internal Structure of the ANFIS Controller Used in this Simulation

III. THE PI CONTROLLER

PI controller has been used in recent years with the purpose of improving the transient and the steady-state performance and also for rejection of disturbances caused by operation events throughout start up [25, 26, 27]. It comprises of proportional action and integral action. The proportional controller diminishes the system error by using proportion of system error to control the system. However, this incorporates an offset error into the system. The integral controller output is proportional to the amount of time there is an error present in the system. The integral action eliminates the offset which is introduced by the proportional control but incorporates a phase lag into the system. The PI controller tuning parameters K_P and K_I have been optimized by tuning with actuator constraint. In control engineering, the integral of weighted sum of error is the key for a PI controller (difference between the output and desired set-point) and the integral of that value.

Mathematically denoted as:

$$e_a(t) = k_p e(t) + k_i \int e(t)dt \qquad (3.6)$$

$$E_a(s) = k_p E(s) + \frac{k_i}{s} E(s) \qquad (3.7)$$

$$G_c = \frac{E_a(s)}{E(s)} = \left[k_p + \frac{k_i}{s} \right] \qquad (3.8)$$

$$G_c = k_p(1 + \frac{1}{sT_i}) \qquad (3.9)$$

The work is a development of the analysis, from the established work based on conventional equations. Control system is unstable for large values of K_P because of the integral control action when applied to PI Controller. The resulting stability of the system, when proportional control action is initiated, shows proportionality between Ti and overshoot and T proportional speed of response

- Overshoot tends to be smaller
- Speed of the response tends to be slower.

The PI provides the advantages of fast response and the zero steady state error

Ziegler and Nichols presented the systematic method for determining the parameters of control PI for the first time. The general control structure proposed for PI controller gain in UPFC system is shown in Figure. 7

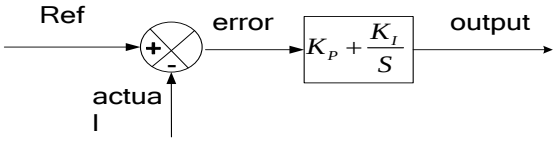


Figure.6. Conventional PI Controller

THE PROPORTONAL IINTEGRAL (PI) CONTROLLER designed here is supposed to maintain the Output voltage and Power Flow to be intact with the reference values defined by the user.
The PI controllers used here are Two in number

The DC Capacitor Voltage Controller (Shunt controller)
The Injected Voltage Controller (Series Controller)
The Following PI Controller takes inputs from the IEEE 5 bus system's 4th Bus i.e., the Load Bus for us, and the DC capacitor voltage at the DC Link , continuously and compares it with the Reference values defined by us and Processes it for further correction initiation action by the Shunt Converter. The Capabilities of the PI Controller Tested here are for the problems that occur at the Bus 3-4, during the Occurrence of faults like LG, LL, LLG and LLL.

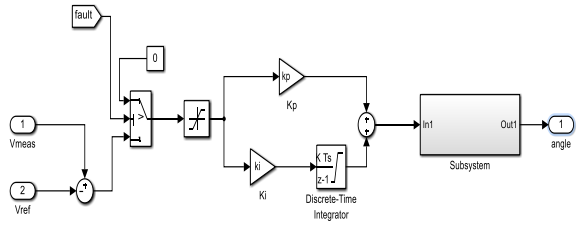


Figure 7 (a).

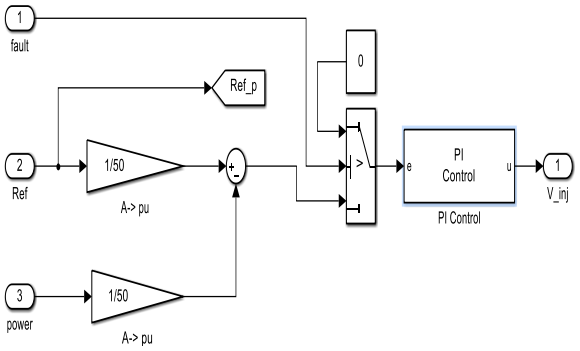


Figure 7.(b)

Figure 7. (a) and (b) : The Injected Voltage Controller

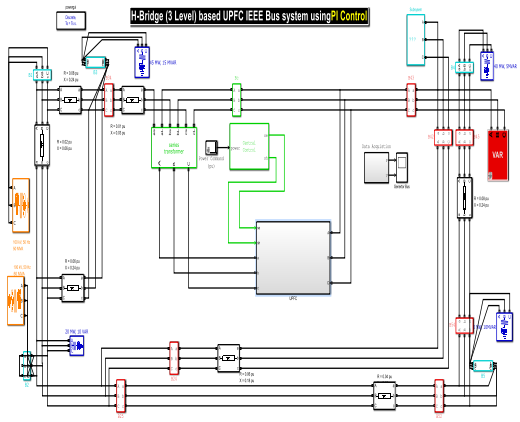


Figure.8. UPFC consisting of Three Level CHB Inverter connected between Buses 3 and 4 in an IEEE 5 Bus System

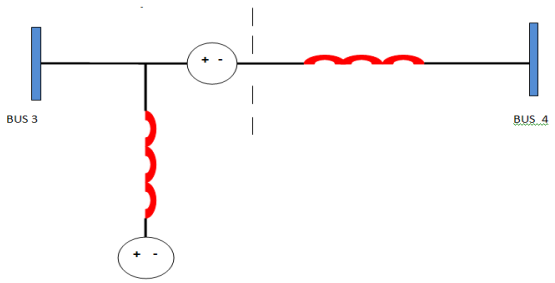


Figure 9 Equivalent Circuit of UPFC connected between buses 3 and 4

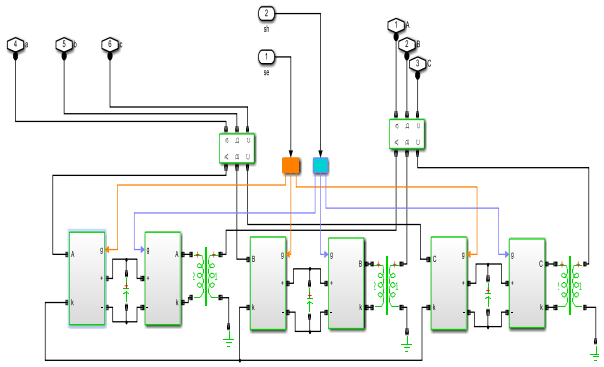


Figure.10. The masked Seven Level Three Phase Cascaded H Bridge Inverter based UPFC Circuit Connections MATLAB MODEL

IV. THE PI CONTROLLERS FOR THE SHUNT AND SERIES SYSTEMS OF THE UPFC

The following Figure shows the two PI Controller System connections used

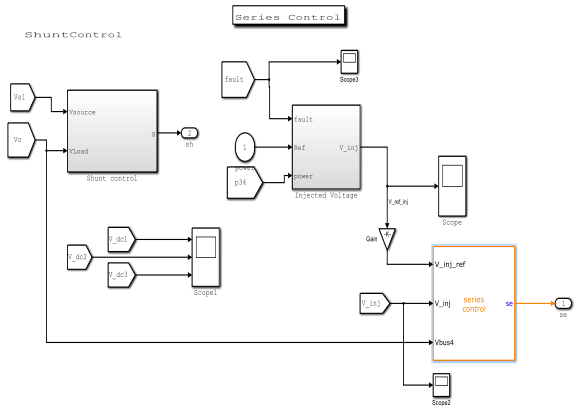
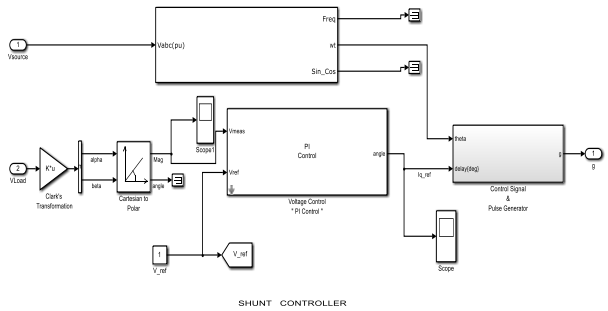


Figure.11. The Series and Shunt Controllers of the UPFC



Fiure.12. The Internal Structure of the PI Shunt Controller

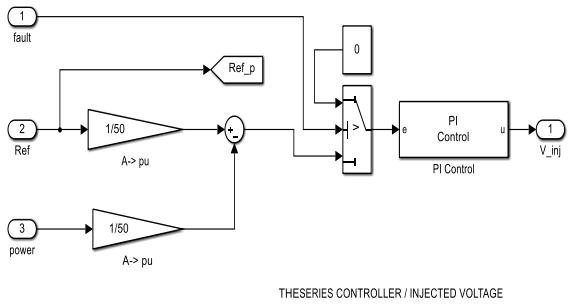


Figure.13. The Internal Structure of the Series Controller / Series Injected Voltage Controller

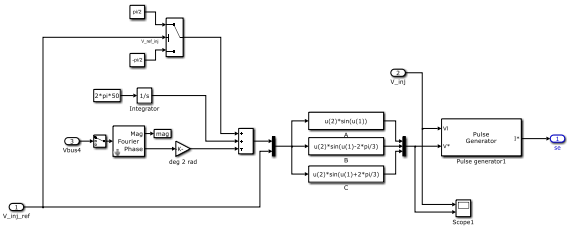


Figure.14. Internal Structure of the Series Injected Voltage Controller Pulse Generator Circuit

V. THE OUTPUTS - RESULTS AND DISCUSSIONS

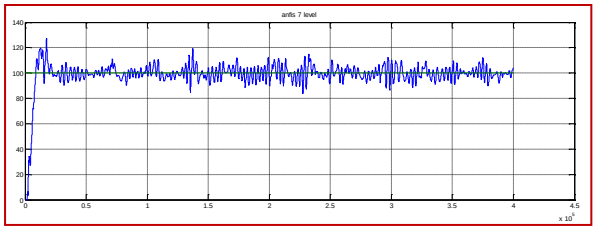


Figure 15 .The Power Transferred by UPFC using an ANFIS Controller

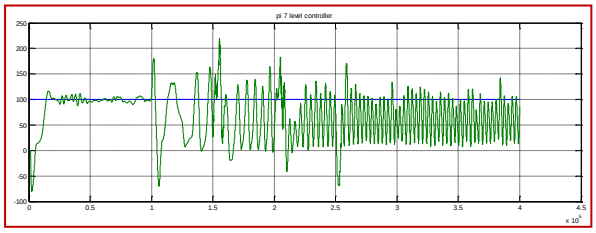


Figure 16 The Power Transferred by UPFC using a PI Controller

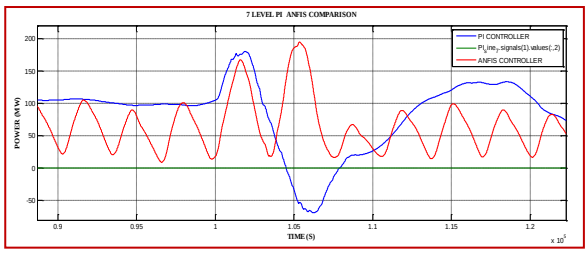


Figure 17 The Settling time of Power Wave while using a PI and ANFIS Controller after LG fault

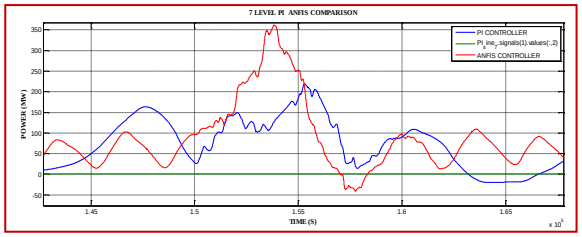


Figure 18 The Settling time of Power Wave while using a PI and ANFIS Controller after LL fault

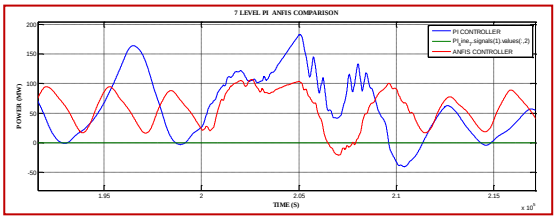


Figure 19 The Settling time of Power Wave while using a PI and ANFIS Controller after LLG fault

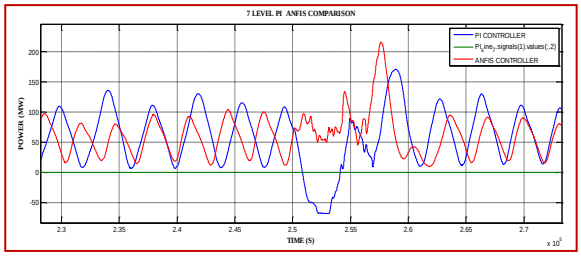


Figure 20 The Settling time of Power Wave while using a PI and ANFIS Controller after LLL fault

Table 1

Comparison of the Settling Times of Power waves transferred by UPFC with an ANFIS and PI Controller

S. No	TYPE OF DISTURBANCE	DURATION OF DISTURBANCE IN SECONDS	SETTLING TIME IN SECONDS (EXACT TIME)	
			ANFIS CONTROLLER	PI CONTROLLER
1	LINE TO GROUNG FAULT	0.5 (10 to 10.5)	11.3	14.2
2	LINE TO LINE FAULT	0.5 (15 to 15.5)	16.5	18.7
3	LINE TO LINE TO GROUND	0.5 (20 to 20.5)	21.6	23.4
4	THREE PHASE FAULT	0.5 (25 to 25.5)	27.3	28.4

CONCUSION

The more accurate the inputs from the 7 Level CHB Inverter the more accurate will be the processed outputs from the ANFIS Controllers , hence when ANFIS controllers are used in combination with 7 Level CHB inverter the accuracy in deciding the PWM and the phase angle of the injected voltages will be precise values enabling the UPFC to produce required voltages to be injected with less harmonics.

REFERENCES

[1] Gyugyi.L "A Unified Power Flow Control Concept for Flexible AC Transmission System" IEE PROCEEDINGS –C Vol. 139 No 4 ,July 1992.

[2] Gyugyi.L "Dynamic Compensation of AC Transmission lines by Solid State Synchronous voltage Sources" IEEE/PES Summer Power Meeting ,Paper No.93 Sm 434-1,PWRD, Vancouver , B.C., Canada , July 1993.

[3] Schauder C.D. and Mehta H ,"Vector analysis and Control of advanced Static Var Compensators", IEE PROCEEDINGS-C Vol. 140 No.4 July 1993.

[4] A.S.Mehraban et al., "Application of World's First UPFC on the AEP System", EPRI Conference ,The Future of Power Delivery Washinton D.C April 9-11,1996.

[5] B.A Renz, et al., "AEP Unified Power Flow Controller Performance", IEEE Transactions on Power Delivery Vol 14 No.4 Oct 1999.

[6] P. S Sen Sarma, K.R.Padiyar ,V Ramanayanan, "Analysis and Performance Evaluation of a DSTATCOM for Compensating Voltage Fluctuations" , PE065PRD(10-2000)

[7] Jingsheng Liao, Kai-tak van , "Cascaded H Bridge MultiLevel Inverters a Reexamination" , IEEE Proceedings on Vehicle Power and Propulsion Conference, IEEE Conference ,Sept. 2007.

[8] Timothy.J.E.MILLER , "Reactive Power Control in Electric Systems", John Wiley India Edition .

[9] W.D. Stevenson "Elements of Power System Analysis" Mc Graw Hill 4th edition

[10] K.R Padiyar and Awanish Jaiswal "Discrete Control of SSSC for Transient Stability Improvement of Power System", national Power System Conference NPSC 2002.

[11] K.R.Padiyar "FACTS Controllers in Power Transmission and Distribution" New Age Publications

[12] Narain G Hingorani and Lazlo Gyugyi, "Understanding FACTS Concepts and technology of Flexible AC Transmission Systems"IEEE Press wiley India Edition.

[13] Padiyar "Power System Dynamics and Stability " 2dn edn.BS Publications.

[14] Kundur , "Power System Dynamics and Stability".EPRI , TataMc Graw Hill

[15] Bambang Sujanarko , "Simulation Development of Carrier Based PWM for Cascaded Multi Level Inverters" International Journal of Computer Applications (0975-8887) Vol 104- No.5 October 2014.

[16] S. Tzafestas and N. P. Papanikolopoulos, "Incremental fuzzy expert PID control," *IEEE Transactions on Industrial Electronics*, Vol. 37, pp. 365-371, 1990.

[17] K. H. Ang, G. Chong and Y. Li, "PID control system analysis, design and technology," IEEE Trans. on Control Systems Technology, Vol. 13,no. 4, 559-576, 2005

[18] ANFIS: Adaptive-Network-Based Fuzzy Inference System , Jyh-Shing Roger Jang Department of Electrical Engineering and Computer Science University of California, Berkeley, CA 94720 IEEE Trans. on Systems, Man and Cybernetics, vol. 23, no. 3, pp. 665-685,May 1993