Implementation of a Modified Low Power Comparator for Flash ADC Used in Bio Medical Application

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Abstract— This project is about the design of low power comparator for flash ADC to be used in biomedical application. A novel comparator circuit architecture consists of the combination of new device and logic will be proposed. using device like FinFET will be proposed in 32nm technology. In day by day, the CMOS supply voltage is decreased to achieve less power consumption.. The main objective of the project is to To design a low power, comparator without stacking using FinFET process for flash ADC which will eliminate second order effects found in CMOS design. In this project, to eliminate the stacking problem and offset in comparator and provides a low power operation , a FinFET based dynamic comparator is to be designed the circuits will be implanted in 32nm technology. The project will be done in SPICE TOOL using predictive technology models of CMOS and FinFET.

I. INTRODUCTION

Latch comparators, also known as regenerative comparators, are finding wide spread use in many high-performance systems such as analogue-to-digital converters (ADCs) and static random access memory bit line detectors as well as radio-frequency transceivers and low-power applications. These dynamic circuits include positive feedback loops and provide high-speed operation, reduced silicon area and low-power consumption. At the same time, because of the metal–oxide–semiconductor (MOS) scaling, these building blocks are getting more subject to process variations which result in increased random offset errors and noise imbalance. Therefore, compensation schemes have become mandatory in latch comparators design. Despite the correction granularity, the digital offset calibration is a practical solution in terms of the operation speed, power consumption and design time and effort compared with fullcustom implementations. This is mainly true when the target calibration resolution is <4 or 5 bits. Further resolution increase will reduce the comparison speed, increase the calculation complexity and deviate the real calibration resolution from the target one. The target or the ideal calibration resolution corresponds to the size of the N-bit digital control word size.

II. METHODOLOGIES

3.1. FINFET TECHNOLOGY

In CMOS technology the channel length lower than 90nm causes in degradation such as high leakage current at gate terminal, threshold leakage current and also results in DIBL (Drain Induced Barrier Lowering). This clearly shows the failureof CMOS technology. So it is necessary to find an alternative with high mobility, better scalability and good stability. With all the above qualities SCE will also be eliminated.

Scaling of deep submicron process with SCE can lower the memory of the circuit but has an adverse effect on the power consumption, temperature and operating features.

The need is to design a device with high speed computation. So FinFET can be replaced as an alternative for CMOS technology due to its high speed performance but at the cost of increased memory.

FinFET not only provides fast computation but also reduces the leakage power to attractive range.

With today's technology there exist multi-gate devices like double gate that havetwo gates within it, a front and back gate respectively. Such multi-gate devices are flexible to use in both planar MOSFET and FinFET. The manufacturing of such devices is also simple. They have many advantages such as higher on-state current, lower off-state current and faster switching speed due to its conductive channel that has a strong control in gates. Therefore the further operation can be carried out with either front gate or back gate or both.

There are three different modes of operation in FinFET multi-gate devices. They are

- Shorted Gate (SG-mode)
- Low Power (LP-mode)
- Independent Gate (IG-mode).

Planar CMOS and FinFET:

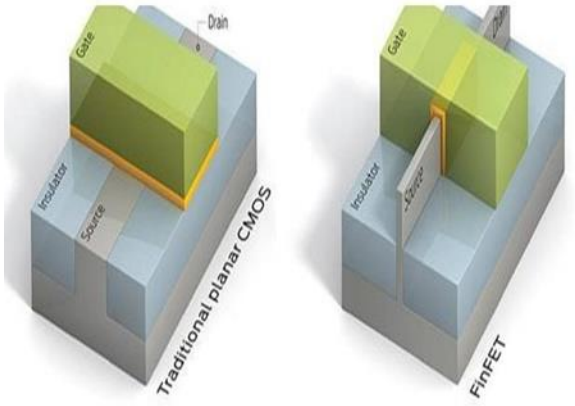


FIGURE 3.1 Planar CMOS and FinFET

The independent gate mode of FinFET behaves as a four-terminal device. In this mode each gate is controlled independently and has different operating voltages. In IG mode a pair of transistor is connected in parallel. By this mode the number of transistors used can be reduced. The threshold leakage is eliminated to a great extend in LP-mode. For this to happen, in the LP mode the back-gate is connected to reverse bias.

- Back-gate capacitance
- Fin thickness
- Oxide thickness

The threshold voltage of back-gate is lower than the front-gate but the power consumption is greatly controlled by back-gate.The main reason for the reduction of leakage current and power consumption in LP-mode is due to the reverse bias of back-gate. Figure 1.5 (a) represents the schematic of the V-I characteristics of CMOS and FinFET.

- Leakage current in CMOS = 43.8nA
- Leakage current in FinFET = 27.7nA.

3.2. Methodologies adapted in ADC

Pipelined ADCs are use mostly for applications that require high speed and medium resolution. Each stage in a pipelined ADC consist of a sub-ADC and multiplying digital to analog converter (MDAC).

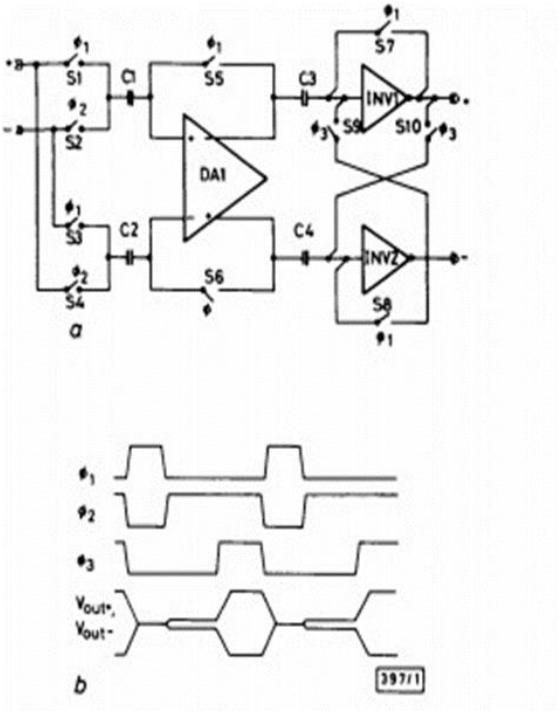


Figure 3.2 a) Circuit Topology and b) Timing Diagram

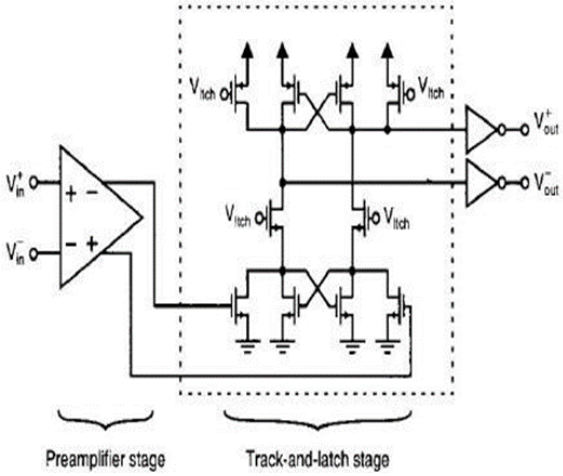


Fig. 3.3 Block schematic of track and latch comparator

Comparators fig 3.3 is the main components in sub-ADC. They are the second most widely used components after amplifier. A comparator is a device that compares an input voltage with a reference voltage and switches its output to either logic low or logic high depending on whether the input is lesser than or greater than the reference respectively. The performance of the pipelined ADC depends on the speed with which the comparison operation is done and hence the design of comparators plays an important role in pipelined ADC. The offset requirement is not of much importance in a pipelined ADC due to the employment of Digital Error Correction (DEC) circuit[5]. Moreover larger input swing, high speed and simple operation are the main objectives in the design of a comparator.

III. PROPOSED METHOD

INTRODUCTION

Design using 32nm FinFET Dynamic Comparator

The circuit in the base paper will be modified during the project phase.

The double-tail dynamic comparator topology has less stacking and therefore can operate at lower supply voltages compared to the dynamic comparator.

The CMOS and FinFET based comparators will be implemented and will be compared.

The FinFET design will be efficient when compared to CMOS method.

In existing method 180nm CMOS is used, in proposed 32nm FinFET will be used.

In the existing circuit, the idea is to combine the charge sharing comparator and output buffer circuit. The comparator combines the features of both the resistive dividing network and differential current sensing comparator. Therefore, the comparator consists of two stages.

Figure 4.1 shows the charge sharing topology for the dynamic latch comparator circuit.

In Figure 3, resistive comparing circuit for regenerative mode is used in series with NMOS transistor NMOS_9 in order to get lo w power consumption. Besides that, PMOS transistor for pre charging circuit is absent during reset mode and NMOS transistor NMOS_1 for output pass transistor is nearly to Vdd/2 for the equalization of both voltage. The latch now is disconnected from Vdd and ground with the aid from transistor PMOS_1 and NMOS_9.

Figure 4.1 shows the charge sharing topology for the dynamic latch comparator circuit.

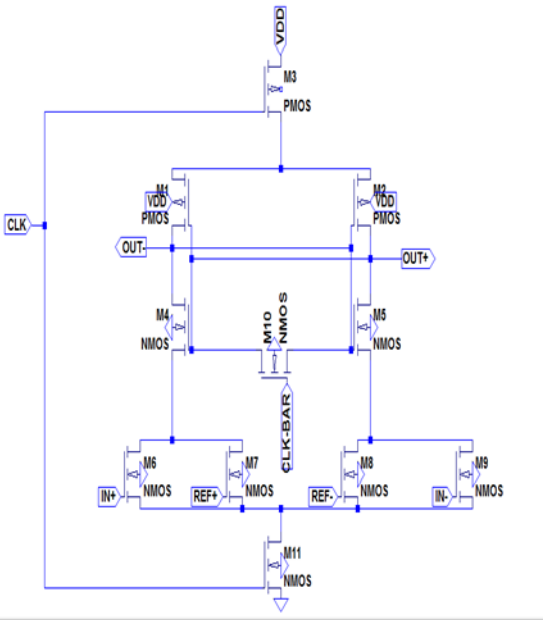


Figure 4.2.1. Charge sharing topology for dynamic latch comparator.

Figure 4.2 shows the output buffer circuit. This circuit is also known as post amplifier. Basically, the circuit receives the information from the latch and produces a digital output signal. The output buffer stage consists of a self-biased diffPPerential amplifier followed by an inverter which gives the digital output. It converts the output of the latch stage to a full-scale digital level output (logic 1 or logic 0). The output buffer stage should be able to accept a differential input signal (Out + and Out-) from the charge sharing circuit and will not have slew rate limitations.

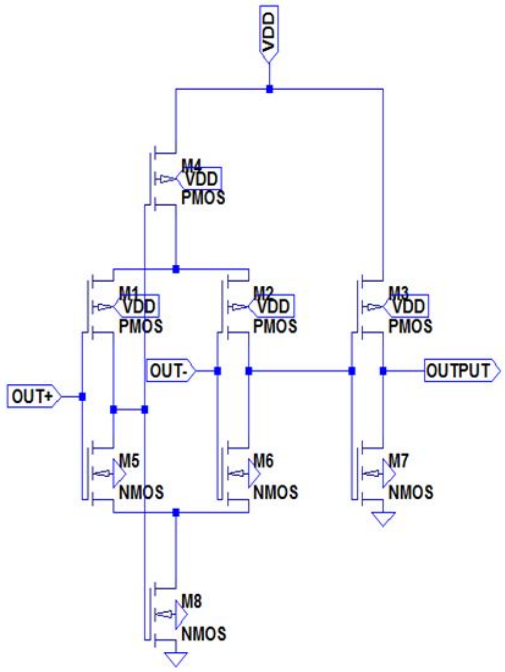


Figure 4.2.2. Output buffer circuit.

The schematic of the dynamic latch comparator is shown in Figure 4.3 which consists of both stages which are the dynamic charge sharing comparator along with the output buffer stage. Now, the two ended output of dynamic charge sharing comparator (Out+ and Out-) in Figure 4.1 become the input to the buffer circuit in Figure 4.2 Thus, making the two ended output of dynamic charge sharing comparator is being converted into single ended output which is labeled as Output.

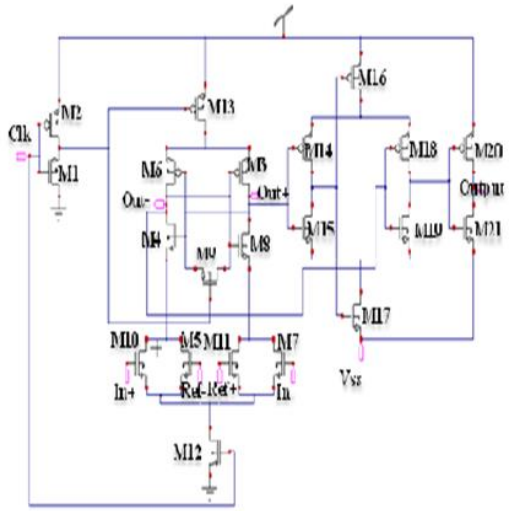


Figure 4.2.3.Proposed dynamic comparator circuit

Transistor sizing is important in ensuring the correct output of the comparator. Table 4.1 shows all the sizing of the transistors used in this design. It is based on CMOS technology of 0.25 µm. The right sizing is critical and will also affect the speed of the circuit.

Table 4.2 Transistor dimension(µm) of the dynamic comparator circuit in Figure 4.3

Transistor	Technology
	0.25 µm
M1, M4, M5, M7, M10, M11	5
M2, M3	10
M6, M13, M14, M16, M18, M20	8
M8, M9, M12, M15, M17, M19, M21	4

The circuit in Figure 4.3 is tested with a supply voltage of 2.0V, 1.8V and 1.6V respectively. The reference voltage is +1 V and -1 V.

4.3. SOFTWARE SPECIFICATION

4.3.1 SOFTWARE REQUIREMENTS

This System requires the following software

FRONT END USED :LTSPICE/HSPICE

BACK END USED :Ms Access

OPERATING SYSTEM :Microsoft Window 11

4.3.2 SOFTWARE DESCRIPTION

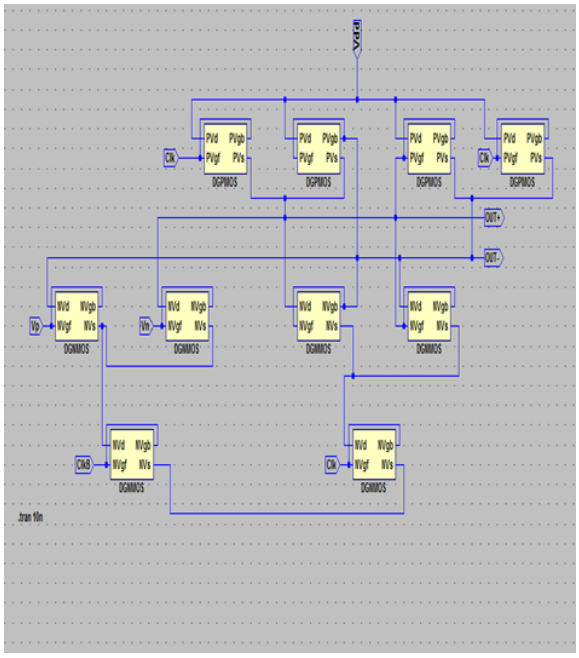
LTSPICE is an analog circuit simulator with integrated schematic capture and waveform viewer. It was explicitly written to outperform analogous tools for sale from software companies in the interest of being used for in-house IC design as part of Linear Technology Corporation's competitive advantage as a semiconductor company. This is a reasonable strategy despite the plethora of existing commercial SPICE offerings.

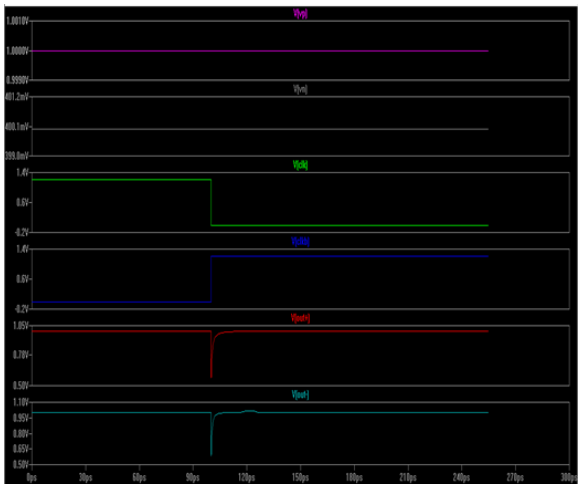
4.3.3 CIRCUIT DESCRIPTION

Circuits are defined by a text net list. The net list consists of a list of circuit elements and their nodes, model definitions, and other SPICE commands. The net list is usually graphically entered. To start a new schematic, select the File=>Open menu item. A windows file browser will appear. Either select an existing schematic and save it under a new name or

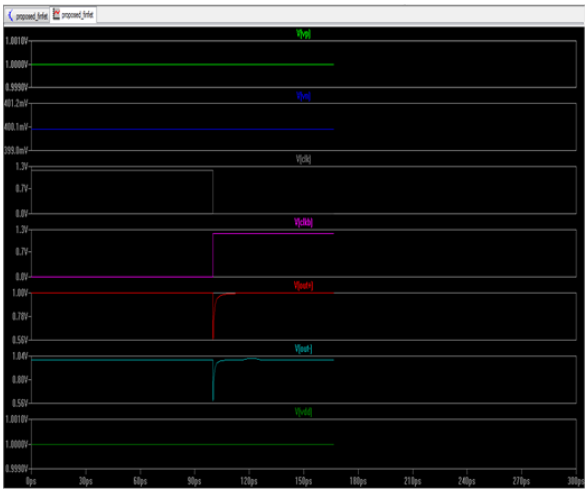
type in a new name to create a new blank schematic file. You will want to make a file with a file name extension of ".asc". The schematic capture commands are under the Edit menu. Keyboard shortcuts for the commands are listed under Schematic Editoroverview.

4.3.4 FINFET BASED DYNAMIC COMPARATOR DESIGN





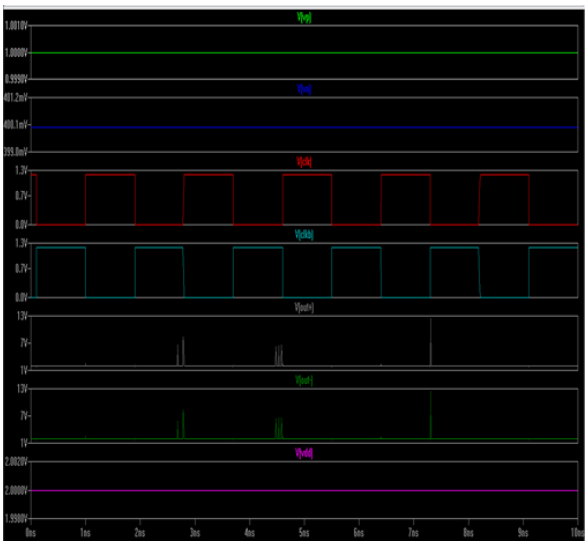
VDD=1.2V



VDD=1.8V

Table.4.3.comparison of power comparison in conventionaland proposed comparator VDDD=1.8V

	Time delay	Average power	Area (Number of transistors)
Conventional comparator (CMOS)	24.16E-10	30.12E-03	20
Proposed comparator (CMOS)	13.52E-10	18.16E-03	10
Proposed comparator (FinFET)	6.415E-10	8.0167E-04	10



VDD=1.2V

Table.4.4.comparison of power comparison in conventional and proposed comparator VDD=1.2V

	Time delay	Average power	Area (Number of transistors)
Conventional comparator (CMOS)	28.31E-10	34.53E-03	20
Proposed comparator (CMOS)	17.87E-10	19.05E-03	10
Proposed comparator (FinFET)	8.9961E-10	8.6124E-04	10

Table.4.5.comparison of power comparison in conventionaland proposed comparator VDDD=1.8V

	Time delay	Average power	Area (Number of transistors)
Conventional comparator (CMOS)	28.36E-10	34.72E-03	20
Proposed comparator (CMOS)	19.63E-10	19.35E-03	10
Proposed comparator (FinFET)	10.2161E-10	8.6124E-04	10

IV. NETLIST CODING

CONVENTIONAL COMPARATOR

```
* conventionalcomparator
.TRAN 1000P 4N
M9 Vdd Clk N002 N004 PMOS l=65n
M11 N002 Vp N006 0 NMOS l=65n
M12 Vdd Clk N003 N005 PMOS l=65n
M14 N003 Vn N006 0 NMOS l=65n
M15 N006 Clk 0 0 NMOS l=65n
V1 Vdd 0 1.2
V2 Clk 0 PULSE(1.2 0 0.1n 0.1p 0.1p 0.9n 1.8n)
V3 Vp 0 1
V4 Vn 0 0.4
V5 ClkB 0 PULSE(0 1.2 0.1n 0.1p 0.1p 0.9n 1.8n)
M1 OUT+ N002 0 0 NMOS l=65n
M2 OUT+ OUT- 0 0 NMOS l=65n
1
V2 Clk 0 PULSE(1.2 0 0.1n 0.1p 0.1p 0.9n 1.8n)
V3 Vp 0 1
V4 Vn 0 0.4
V5 ClkB 0 PULSE(0 1.2 0.1n 0.1p 0.1p 0.9n 1.8n)
M3 Vdd Clk OUT+ Vdd PMOS l=65n
M1 Vdd OUT- OUT+ Vdd PMOS l=65n
M2 OUT- OUT+ N002 0 NMOS l=65n
M4 Vdd Clk OUT- Vdd PMOS l=65n
M5 Vdd OUT+ OUT- Vdd PMOS l=65n
M6 N002 Clk 0 0 NMOS l=65n
M7 OUT- Vp N001 0 NMOS l=65n
M8 OUT+ Vn N001 0 NMOS l=65n
M9 N001 ClkB 0 0 NMOS l=65n

.include
C:\Users\Admin\Desktop\comparator\pmos.txt
.include
C:\Users\Admin\Desktop\comparator\nmos.txt

.PRINT I(Vdd)
.MEAS TRAN tdlay TRIG V(OUT+) VAL=0.5 RISE=1 + TARG V(N001) VAL=0.5 FALL=1

.meas tran avgpower AVG power from=1000P to=4N
.meas tran peakpower MAX power from=1000P to=4N
.meas tran avgcurrent AVG I(Vdd) from=1000P to=4N
.meas tran peakcurrent MAX I(Vdd) from=1000P to=4N

.end
```

DYNAMIC COMARATOR

```
.TRAN 800P 20N
.PRINT TRAN V(vdd) V(IN+) V(IN-) V(OUTPUT)

M1 N003 OUT+ OUT- VDD PMOS l=0.25u w=2u
M2 N003 OUT- OUT+ VDD PMOS l=0.25u w=12.5u
M3 VDD N001 N003 VDD PMOS l=0.25u w=2u
M4 OUT- OUT+ N007 0 NMOS l=0.25u w=1.25u
M5 OUT+ OUT- N008 0 NMOS l=0.25u w=1u
M6 N007 IN+ N009 0 NMOS l=0.25u w=1.25u
M7 N007 REF+ N009 0 NMOS l=0.25u w=1u
M8 N008 REF- N009 0 NMOS l=0.25u w=1.25u
M9 N008 IN- N009 0 NMOS l=0.25u w=1.25u
M10 OUT+ CLK-BAR OUT- 0 NMOS l=0.25u w=1u
M11 N009 CLK 0 0 NMOS l=0.25u w=1u
V1 IN+ 0 PULSE(0 2 0 0.001p 0.001p 1 2)
```

```
V2 CLK 0 PULSE(0 1 0 0.001p 0.001p 1 2)
V3 CLK-BAR 0 PULSE(1 0 0 0.001p 0.001p 1 2)
V4 IN- 0 PULSE(1 0 0 0.001p 0.001p 1 2)
V5 REF+ 0 1
V6 REF- 0 -1
V7 VDD 0 1
M12 N002 OUT+ N005 VDD PMOS l=0.25u w=2u
M13 N002 OUT- N004 VDD PMOS l=0.25u w=2u
M14 VDD N004 OUTPUT VDD PMOS l=0.25u w=2u
M15 VDD N005 N002 VDD PMOS l=0.25u w=2u
M16 N005 OUT+ N006 0 NMOS l=0.25u w=1u
M17 N004 OUT- N006 0 NMOS
M18 OUTPUT N004 0 0 NMOS l=0.25u w=1u
M19 N006 N005 0 0 NMOS l=0.25u w=1u
M20 VDD CLK N001 VDD PMOS l=0.25u w=12.5u
M21 N001 CLK 0 0 NMOS l=0.25u w=1.25u

.include Z:\HSPICE\NMOS_32nm.txt

.include Z:\HSPICE\PMOS_32nm.txt

.PRINT I(V1)
.meas tran avgpower AVG power from=800P to=1000N
.meas tran peakpower MAX power from=800P to=1000N
.meas tran avgcurrent AVG I(OUTPUT) from=800P to=1000N
.meas tran peakcurrent MAX I(OUTPUT) from=800P to=1000N
.end
```

PROPOSED CMOS COMPARATOR

```
.TRAN 1000P 4N

M11 OUT+ OUT- N002 0 NMOS l=65n
V1 Vdd 0 1.2
V2 Clk 0 PULSE(1.2 0 0.1n 0.1p 0.1p 0.9n 1.8n)
V3 Vp 0 1
V4 Vn 0 0.4
V5 ClkB 0 PULSE(0 1.2 0.1n 0.1p 0.1p 0.9n 1.8n)
M3 Vdd Clk OUT+ Vdd PMOS l=65n
M1 Vdd OUT- OUT+ Vdd PMOS l=65n
M2 OUT- OUT+ N002 0 NMOS l=65n
M4 Vdd Clk OUT- Vdd PMOS l=65n
M5 Vdd OUT+ OUT- Vdd PMOS l=65n
M6 N002 Clk 0 0 NMOS l=65n
M7 OUT- Vp N001 0 NMOS l=65n
M8 OUT+ Vn N001 0 NMOS l=65n
M9 N001 ClkB 0 0 NMOS l=65n
.include
C:\Users\Admin\Desktop\comparator\pmos.txt
.include
C:\Users\Admin\Desktop\comparator\nmos.txt

.PRINT I(Vdd)
.MEAS TRAN tdlay TRIG V(OUT+) VAL=0.5 RISE=1 + TARG V(N001) VAL=0.5 FALL=1

.meas tran avgpower AVG power from=1000P to=4N
.meas tran peakpower MAX power from=1000P to=4N
.meas tran avgcurrent AVG I(Vdd) from=1000P to=4N
.meas tran peakcurrent MAX I(Vdd) from=1000P to=4N

.end
```

FINFET BASED COMPARATOR

```
* ff
.TRAN 1000P 4N

XU3 Vdd Clk Clk OUT+ DGPMOS wdg=150n ldg=20n
XU4 Vdd OUT- OUT- OUT+ DGPMOS wdg=150n ldg=20n
XU5 Vdd OUT+ OUT+ OUT- DGPMOS wdg=150n ldg=20n
XU6 Vdd Clk Clk OUT- DGPMOS wdg=150n ldg=20n
XU7 OUT+ OUT- OUT- N002 DGNMOS wdg=100n ldg=20n
XU8 OUT- OUT+ OUT+ N002 DGNMOS wdg=100n ldg=20n
XU9 N002 Clk Clk N003 DGNMOS wdg=100n ldg=20n
XU10 OUT- Vp Vp N001 DGNMOS wdg=100n ldg=20n
XU11 OUT+ Vn Vn N001 DGNMOS wdg=100n ldg=20n
XU12 N001 ClkB ClkB N003 DGNMOS wdg=100n ldg=20n
V1 Vp 0 1
V2 Vn 0 0.4
V3 Clk 0 PULSE(1.2 0 0.1n 0.1p 0.1p 0.9n 1.8n)
```

```
V4 ClkB 0 PULSE(0 1.2 0.1n 0.1p 0.1p 0.9n 1.8n)
V5 Vdd 0 2

.include I:\phase2\proposed\pmos.txt
.include I:\phase2\proposed\nmos.txt

.PRINT I(Vdd)
.MEAS TRAN tdlay TRIG V(OUT+) VAL=0.5 RISE=1 + TARG V(N001) VAL=0.5 FALL=1

.meas tran avgpower AVG power from=1000P to=4N
.meas tran peakpower MAX power from=1000P to=4N
.meas tran avgcurrent AVG I(Vdd) from=1000P to=4N
.meas tran peakcurrent MAX I(Vdd) from=1000P to=4N

.end
```

CONCLUSION AND FUTURE WORK

A dynamic comparator with less power consumption and high speed is used. In phase 1, existing methodology like dynamic latched comparator , double tail and fully differential comparator is implemented which is suitable for a pipelined ADC which can work up to 10M samples/sec

In this project will design and implement Dynamic comparator in 32nm for ADC.

The simulation of the dynamic latched comparator is done in SPICE environment and the output observed.

In Future work, the proposed dynamic latch comparator will be implemented with smaller size and new device technol

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