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Power-Efficient SPI-Based BIST Design Using Clock Gating Method

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Abstract - In modern electronic systems, power efficiency is a critical design consideration, particularly in embedded systems where power resources are limited. Built-in Self-Test (BIST) methodologies are widely employed to ensure system reliability and facilitate fault detection and diagnosis. However, BIST implementations often introduce additional power utilization, which will be detrimental in power-sensitive applications. This project explores the optimization of power efficiency in Serial Peripheral Interface (SPI)-based BIST systems through the implementation of clock gating techniques. Clock gating is a dynamic energy optimization approach that minimizes power utilization by disabling the clock signal to idle modules, thereby minimizing switching activity. By integrating clock gating into the SPI-based BIST architecture, we aim to achieve significant reductions in power usage without compromising test coverage or performance. The proposed methodology involves designing a clock gating controller that dynamically monitors the activity of the SPI modules and selectively gates the clock signals. Our results indicate that the power utilization of the SPI-based clock-gated BIST system is reduced by up to 10.12% compared to a non-clock-gated SPI BIST system. Additionally, the area of the SPI-based clock-gated BIST is reduced by up to 8.42% compared to the non- clock-gated SPI BIST system.

Keywords— Low Power, SPI, BIST, TPG, Clock Gating.

I. INTRODUCTION

In contemporary embedded systems, power efficiency has emerged as a paramount design criterion, driven through the increasing demand for portable and battery-operated devices. BIST techniques are extensively utilized in these systems to enhance reliability and facilitate fault detection and diagnosis. Despite their advantages, BIST implementations can lead to elevated power consumption, posing a significant challenge in power-sensitive applications. Serial Peripheral Interface (SPI) is a widely adopted communication protocol in embedded systems due to simplicity and effectiveness. Integrating BIST into SPI- based systems can ensure robust fault coverage, but it can also exacerbate power consumption issues. Therefore, optimizing power efficiency in SPI-based BIST systems is essential for prolonging battery lifespan and improving overall system performance. Clock gating is a dynamic energy optimization approach that minimizes usage addresses this challenge by reducing unnecessary power usage. It operates by selectively disabling the clock signal to inactive modules, thereby minimizing switching activities and conserving energy. This project explores the application of clock gating in SPI-based BIST systems to achieve substantial power savings.

The primary objective of this project is to create and execute a clock gating mechanism tailored for SPI-based BIST architectures. The proposed solution involves developing a clock gating controller that dynamically monitors the activity of SPI modules and gates the clock signals accordingly. Through detailed simulations, Our goal is to show that this method subsequently lowers power usage while preserving the reliability and efficiency of the BIST process.

A BIST embedded SPI module designed for one master and one slave configurations. With increasing numbers of slaves complicating circuits, BIST offers a solution for self-testing to ensure fault-free operation, reducing care and validating costs. The module, which transfers 8-bit data, is created using Verilog HDL on the EDA playground platform, and is suitable for ASIC or SoC applications.[1]
BIST generates test pattern to evaluate circuits, targeting the CUT. Manual testing is time-consuming and costly, so BIST is used. A BIST design for four-bit combinational logic circuit, including the calculation of the golden signature value. The system comprises an LFSR (pattern generator), CUT, signature analyzer, and comparator. The LFSR generates 2^n - 1 test patterns, applied to the CUT. The signature analyzer processes the CUT output, and the comparator checks this against the golden signature. A matching result indicates a fault-free CUT, while a mismatch signals a fault.[2]
Low power utilization is crucial for portable and

mobile devices. BIST makes chips self-testable but adds extra circuitry, increasing power consumption. A new method to minimize shift operation, power in BIST architecture by modifying the LFSR to skip unnecessary shifts using clock gating. Implemented for stuck-at faults. [3]
As VLSI chips integrate more functions, minimizing power dissipation and enhancing battery life become crucial. Dynamic power dissipation, caused by logic switching, increases significantly in BIST systems due to low correlation between test pattern generated by LFSRs. This can double the test power compared to normal operation. This technique introduces a low-power LFSR using two clock gating method to optimized test power. Designed and simulated with Xilinx Vivado, the RTL schematics, simulation results, and power analysis reports are presented for comparison. [4]
A BIST architecture designed to minimize power utilization during testing while ensuring high fault coverage for low- power VLSI applications. Using Verilog HDL for modelling and simulation, the research explores power reduction techniques such as test pattern compression, selective clock gating, and power-aware test scheduling. Implemented on an FPGA platform, the proposed design demonstrates feasibility and practicality, significantly reducing test power utilization.

This work contributes to low-power VLSI design, offering a compatible solution for standard Verilog synthesis and a wide range of applications, enhancing energy efficiency and extending battery life in portable devices. [5]
A power-efficient BIST utilizing a bit-reciprocating LFSR and modified MISR for testing combinational circuits. The bit-reciprocating LFSR acts as the TPG, generating test patterns for the CUT. The modified MISR serves as the ORA, analysing CUT outputs to detect single stuck-at faults. This BIST architecture efficiently detects and identifies potential faults in combinational circuits.[6]

II. PROPOSED SYSTEM

The proposed system implements clock gating for optimizing power efficiency in SPI-based BIST systems. It consists of a TPG employing a LFSR with clock gating to minimize unnecessary bit shifting. The CUT is configured as an SPI adder, with correct and faulty operational states registered in the ORA for comparison. A BIST controller orchestrates the testing process, managing input pattern selection, clock gating, and result analysis. Detailed simulations validate the power savings achieved through clock gated while maintaining robust test coverage and system performance.

A. SPI ARCHITECTURE

SPI is a communication protocol used by various devices, notable for allowing continuous data transmission without interruption. It operates in a master-slave arrangement, where the master generates the main SPI clock to synchronize data. SPI supports higher frequencies than other serial protocols and allows multiple slaves to connect to a one master. Each slave is selected by an active-low chip select signal from the master. SPI uses two data lines: MOSI (Master Out Slave In) for data from master to slave, and MISO (Master In Slave Out) for data from slave to master.

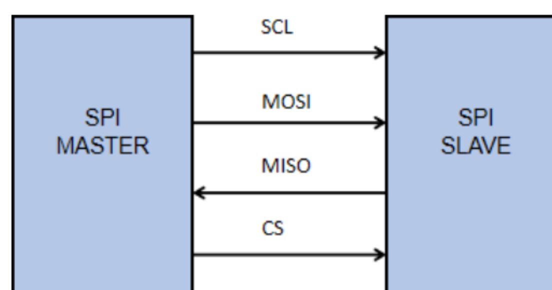

Figure 1: SPI Architecture

B. BIST Architecture

BIST is a self-test technique where all testing functions are external to the CUT. The BIST architecture includes three key blocks connected to the CUT:

- Test Patterns Generator (TPG)
- Output Response Analyzer (ORA)
- Test Controller

The TPG generates random pattern for the CUT, using methods like stored memory patterns, counters, or LFSR. The ORA block, consisting of a compactor (using Multiple Input Serial Register, MISR) and a comparator, compacts and analyzes the CUT's responses. These compacted responses, or output signatures, are compared to a golden signature registered in ROM to identify faults. The Test Controller manages the activation and analysis of all tests.

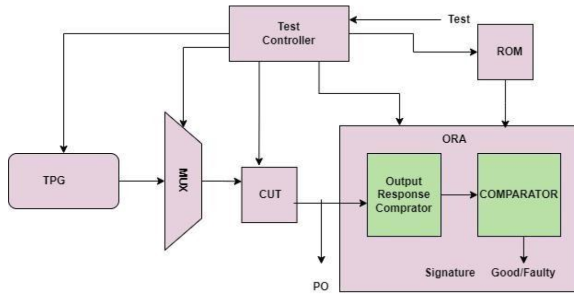

Figure 2: BIST Architecture

III. METHODOLOGY

The proposed methodology for optimizing power efficiency in SPI-based BIST systems involves several key phases. Initially, the system design and architecture are defined, identifying essential components such as the TPG using a LFSR, the CUT configured as an SPI adder, the ORA, and the BIST Controller. In the next phase, clock gating is implemented for the TPG by developing a mechanism to monitor the LFSR outputs and detect consecutive identical bits, there by gating the clock signals to avoid unnecessary bit shifting. The SPI adder is configured as the CUT, with mechanisms in place to store correct and faulty operational states in the ORA for subsequent comparison. The BIST controller is developed to sustaining the entire testing process, including input pattern selection, clock gating management, and triggering the ORA for result analysis. Detailed simulations are conducted to measure power consumed and validate the effectiveness of the clock gated technique. The simulation results are analyzed to evaluate power savings, test coverage, and system performance. Finally, the findings are documented, highlighting the achieved power efficiency and overall benefits, and prepared for presentation. This structured approach aims to attain substantial energy savings while preserving robust test coverage and system performance in SPI-based BIST systems.

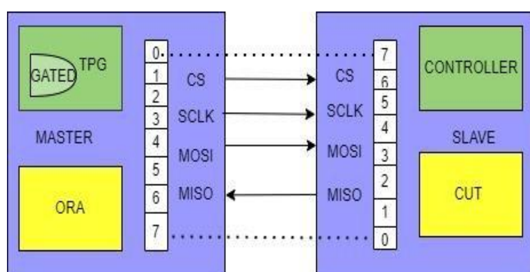

Figure 3: BIST embedded SPI block

A. *Implemented TPG*

Testing is crucial in digital systems for reducing costs and improving throughput. VLSI design testing involves scan chain insertion, compression logic, and ATPG algorithms for ATE machines. BIST is another method, featuring on-chip self-test capabilities with extra circuitry like TPGs, response analyzers, ROM, and controllers. LFSR-based test pattern are preferred over counter-based ones due to fewer combinational circuits. In conventional LFSR test pattern generators, bit sequences are created by shifting bits between flip-flops, which consumes power. This power minimization can be minimized by adding clock gated circuitry to skip unnecessary shift operations.

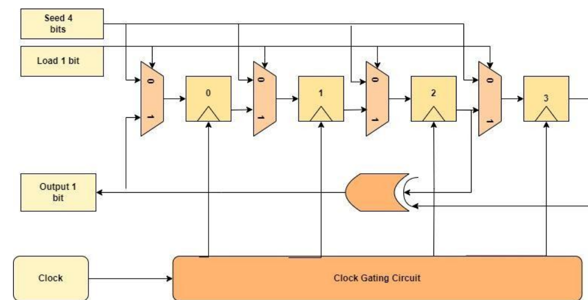

Figure 4. Proposed Clock gated TPG

Before clocking each flip-flop in the LFSR, compare the input and output. If they are the same, gate the clock. This means that if a flip-flop in the TPG has the same data as before, it is disconnected from the clock and excluded from the shifting operation. This reduces power utilization by eliminating the flip-flop from the LFSR until the shift operation is complete.

B. *Output Response Analyzer*

The MISR processes the output response from the CUT and generate a set of non-repeated sequences. It is implemented using a LFSR due to its linear properties. The MISR helps reduce the requirement for storing golden responses, which would otherwise need additional memory and area, and be difficult to compress. The circuit implementation of a four- bit MISR. The main operation of the response analyzer is to comparing the CUT's actual responses with the golden responses stored in ROM and produce a signature indicating whether the circuits are functioning correctly. The output of the response analyzer is a pass/fail signal, confirming whether the circuit has passed or failed the test. The response analyzer takes the non-repeated sequences from the MISR and verifies if the CUT is non-fault or not.

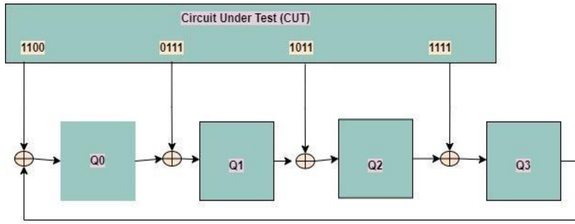

Figure 5: Multi Input Shift Register

IV. RESULTS

A. *Clock Gated TPG*

In this proposed work, an 8-bit LFSR has been designed to generate 255 pseudo-random patterns (2^8 - 1). The LFSR produces test patterns with a maximum sequence length of
255. When one complete cycle is finished, the signal goes high, indicating the completion of the cycle. This design shows reduced power consumption compared to a conventional LFSR. The Clock gating primarily used for reducing power utilization, can also indirectly lead to area reduction in digital circuits. By disabling the clock signal to inactive parts of the circuit, clock gating reduces the need for extensive power distribution networks and thermal management structures, allowing for a more compact layout. Additionally, it optimizes resource allocation, resulting in fewer components and interconnects, which further reduces the chip area also. As demonstrated below.

Parameter analyzed	CG-TPG	Non CG-TPG
Power consumed (mw)	1.27	1.68
Area Consumed (µm²)	605.302	861.391

Table 1: Power & Area Consumed by TPG

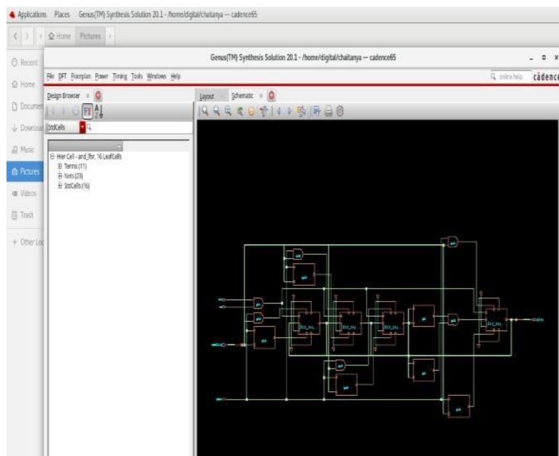

Figure 7: RTL of TPG with Clock Gated

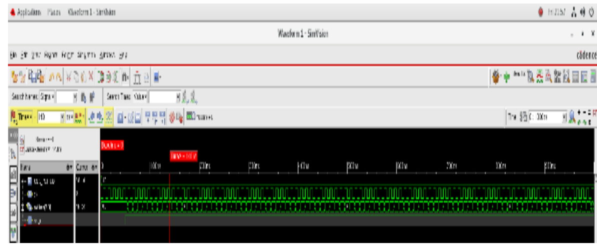

Figure 8: CG-TPG Waveform

B. *Output Response Analyzer*

The ORA in a BIST system for an 8-bit adder verifies the adder's correctness by comparing its outputs to expected results. The ORA processes test patterns from a TPG through the adder and captures the actual sum and carry- out. Simultaneously, an Expected Result Generator provides the correct outputs. The ORA compares these outputs, flagging discrepancies. If all match, the adder functions correctly; otherwise, it indicates a fault, ensuring automated, efficient, and reliable testing.

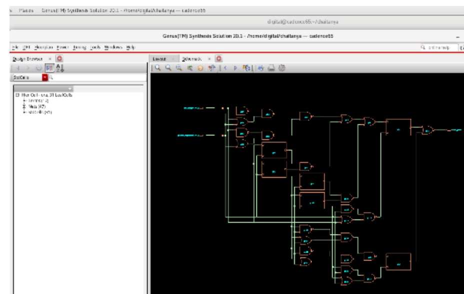

Figure 9: RTL of ORA

Figure 10: Waveform of ORA

C. *Circuit Under Test*

In a BIST system, the CUT is the component being tested for functionality. When the CUT is a 4-bit adder, the BIST system generates test patterns to thoroughly verify its operation. The 4-bit adder takes two 4-bit binary inputs and produces a 4-bit sum and a carry-out. The BIST includes a TPG to provide various input combinations to the adder. The outputs (sum and carry-out) are then checked against expected results using an ORA. Any discrepancies between actual and expected outputs indicate a fault, ensuring reliable and automated testing of the 4-bit adder.

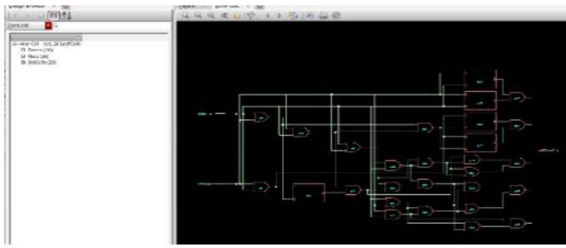

Figure 11: RTL of CUT

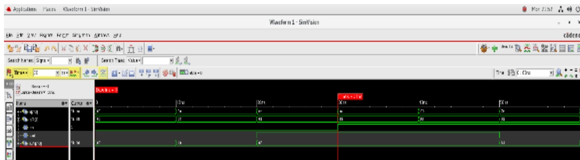

Figure 12: Waveform of CUT

D. SPI Embedded with BIST

SPI-based BIST for clock gating in a TPG optimizes power efficiency during self-tests in ICs. Clock gating selectively disables the clock signal to specific component of the circuitry when not in use, reducing power consumption. Integrating SPI control allows external devices to manage the clock gating mechanism within the BIST pattern generator. This ensures that only necessary components are active during test sequences, conserving energy. This approach is particularly valuable in low-power applications, maintaining efficient power usage while ensuring robust self-testing and reliable IC performance.

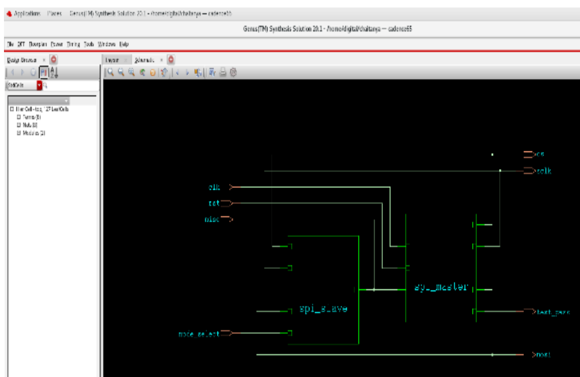

Figure 13: SPI with CG-BIST

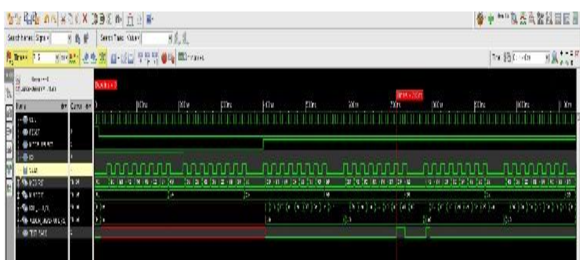

Figure14: Output of SPI with CG-BIST

Parameters Considered	Clock Gated SPI-BIST	Non-Clock Gated SPI-BIST
Power consumption (mw)	4.904	5.458
Area consumptions(μm^2)	3666.733	4004.430

Table 2: Power & Area Report

V. CONCLUSION

This project effectively showcases the implementation of clock gating to optimize power efficiency in SPI-based Built- in Self-Test (BIST) systems. By integrating a dynamic clock gating mechanism into the TPG using a LFSR, we substantially lower energy usage during test operations. The SPI adder, configured as the CUT, effectively validates the proposed approach by comparing correct and faulty operational states within the ORA. The BIST controller efficiently manages the overall testing process, including input selection and clock gating control. Simulation results confirm that the clock gated technique achieves substantial power savings with minimal effect on test scope and system performance. Specifically, the power utilization of the SPI- based clock-gated BIST system is minimized by up to 10.12% compared to a non-clock-gated SPI BIST system. Additionally, the area of the SPI-based clock-gated BIST is reduced by up to 8.42% compared to the non-clock-gated SPI BIST system. This work provides a scalable and energy- efficient solution for embedded systems, contributing to the advancement of low-power testing methodologies in electronic design.

VI. FUTURE SCOPE

In the future, the design and testing of SPI architectures for multiple slave devices will focus on creating efficient arbitration mechanisms and developing robust BIST strategies. These improvements aim to ensure seamless communication and thorough testing of all connected devices without interference, enhancing the reliability and efficiency of multi-slave systems.

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