Instrumentation Amplifier for Pacemaker Using 180nm CMOS Technology

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***Abstract*— An instrumentation amplifier is an essential component in a pacemaker, designed to amplify and filter the heart's weak electrical signals, typically in the frequency range of 0.05 Hz to 50 Hz. The proposed circuit was developed using 180nm CMOS technology and was simulated with Cadence Virtuoso software. The amplifier achieved a gain of over 150 dB, a gain bandwidth (GBW) of 13.115 kHz, a phase margin of 183°, and a common-mode rejection ratio (CMRR) of 100 dB, along with other performance parameters that meet the required specifications.**

Keywords— Pacemaker, Instrumentation Amplifier, Differential Amplifier, Gain, CMRR, Gain Bandwidth.

I. INTRODUCTION

A pacemaker is a medical device that regulates the heartbeat by delivering electrical impulses to the heart muscle. Pacemakers are broadly categorized into two types: internal (implantable) pacemakers and external (wearable) pacemakers. They are commonly used to treat conditions such as bradycardia (a slow heart rate), heart rhythm disorders, and instances where the heart's rhythm is not properly generated.

To function effectively, pacemakers must accurately sense cardiac signals. This is achieved through an amplifier, a bandpass filter, and an analog-to-digital converter (ADC) that processes these signals. The sensing mechanism typically uses a differential amplifier and a bandpass filter to detect the electrical signals from the heart's atrium and ventricle by comparing two sense signals.

This paper focuses on the design and implementation of an Instrumentation Amplifier (IA), which plays a critical role in accurately measuring the heart's electrical signals and distinguishing between normal and abnormal rhythms. An IA provides differential amplification, high common-mode rejection ratio (CMRR), high input impedance, precision, adjustable gain, and low noise—features essential for the pacemaker's proper operation.

II. DESIGN OVERVIEW

The proposed IA, depicted in Fig. 2, is designed using three identical differential amplifiers, as illustrated in Fig. 1, arranged in a specific configuration.

A. Differential Amplifier

Differential amplifiers are essential in pacemakers due to their ability to precisely amplify small differential signals, even in the presence of significant noise. By choosing the right components and meticulously designing the circuit, these amplifiers can achieve the high levels of performance needed for accurate medical diagnostics and continuous heart monitoring. This precision ensures reliable detection of cardiac signals, which is crucial for effective pacing and treatment.

It consists of the transistor NMOS (NM0, NM1, NM2, NM3) and PMOS (PM0, PM1). Vin1 and Vin2 are the inputs and Vout is output.

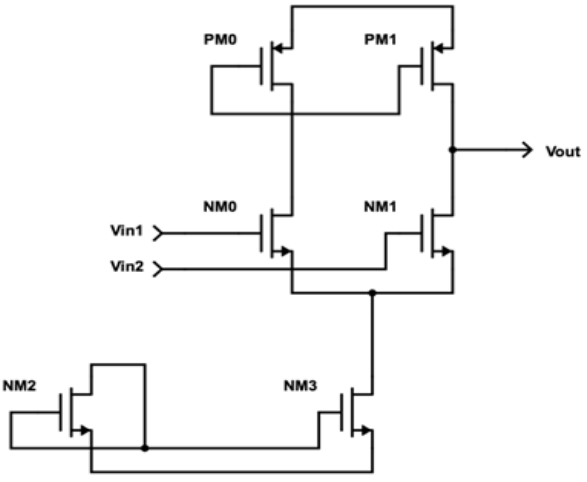

Fig. 1 Differential Amplifier

Transistor Dimensions of differential amplifier

Table No.1 Transistors Dimension

MOSFET	W/L SIZE
PM0	1.5µM/180nM
PM1	20µM/180nM
NM0	4µM/180nM
NM1	5µM/180nM
NM2	50µM/180nM
NM3	2µM/180nM

B. Instrumentation Amplifier

The proposed IA circuit, shown in Fig. 2, is built around three identical differential amplifiers. It consists of two stages: the first stage is the input stage, which amplifies the difference between Vin1 and Vin2 while providing high input impedance and initial common-mode rejection. The second stage is the output stage, where the differential amplifier (A3) subtracts the outputs of the input stage amplifiers to produce the final amplified output with improved common-mode rejection and differential gain. Precision resistors are typically used to set the amplifier's gain, and feedback networks are employed to regulate the input impedance, gain, and bandwidth.

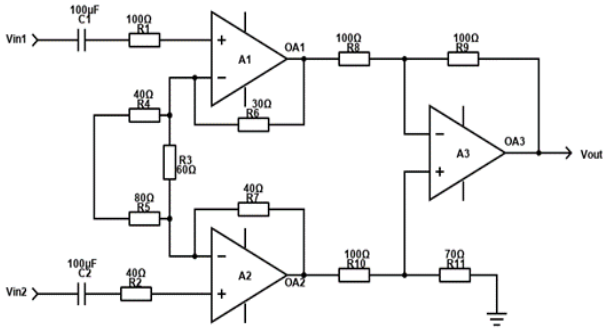

Fig.2 Proposed Instrumentation Amplifier

The voltage generated from the biological signal passes through capacitors C1 and C2, which help prevent polarization effects caused by the electrodes without distorting the ECG signal [2]. Resistors R1 and R2 limit the current to protect the human body from large currents. The common-mode output of amplifiers A1 and A2 is feedback to R3, ensuring that the voltage across R3 matches the input voltage of A1 and A2. The output signals from A1 and A2 pass through resistors R8 and R10 to amplifier A3, where the ECG signal is further amplified [2].

The amplified output voltage is:

$$Vout = -R9/R8(OA1 - OA2)$$

$$= -R9/R8[1 + 2(R6/R7)](Vin1 - Vin2) \dots (1)$$

Vin1 and OA1 are the input and output voltages of amplifier A1, while Vin2 and OA2 are the input and output voltages of amplifier A2. Using the resistor values provided in Fig. 1, calculate the value of Vout .

$$Vout = -2.5(Vin1 - Vin2) \dots\dots\dots\dots\dots\dots (2)$$

III TOOL DISCRIPTION

CADANCE VIRTUOSO -

Version IC6. 1.8-64b.500.18

Cadence Virtuoso is an electronic design automation (EDA) suite widely used in semiconductor design. It offers a comprehensive set of tools for designing and verifying complex integrated circuits (ICs), including analog, mixed-signal, and custom digital designs. Key features of Cadence Virtuoso include schematic capture, layout editing, parasitic extraction, design rule checking (DRC), layout-versus-schematic (LVS) verification, and options for customization and automation. The simulations were performed using the Analog Design Environment (ADE)-L platform.

IV SPECIFICATIONS

Here are the key specifications typically associated with IA required for implantable pacemaker :

- Gain: It refers to how much the input signal is amplified to produce the output signal.
- CMRR: It shows a good circuit that rejects the two common signals from two inputs.
- Open-loop gain refers to the gain of an amplifier circuit when no feedback is applied.
- CM Gain: It refers to the amplification of signals that are common to both input terminals of an amplifier.
- Offset voltage is a small voltage that is present at the input terminals of an amplifier when the input terminals are shorted together.
- PSRR: power supply rejection ratio. It measures the ability of an amplifier to reject variations or noise in the power supply voltage.
- Noise Analysis: Noise analysis is a process used to study and characterize the noise, such as thermal noise, shot noise, flicker noise, and others, to understand their impact on the circuit's performance.

- Stability refers to the ability of the circuit to maintain its intended operation over time and under varying conditions.

The desired specifications of the proposed circuit are given in table No.2 below:

Specifications	Desired Value
Supply Voltage	±1.8V
Technology	180nm
Frequency Range	1-200Hz
Gain	> 100dB
CMRR	> 70dB
Open Loop Gain	> 100dB
GBW	5MHz
Phase Margin	> 60deg.
Input Referred Noise	< 6uV RMS

Table No.2 Desired Specifications

V. SIMULATIONS RESULTS & DISCUSSION

To verify the correctness of the design, several simulations were performed, as shown below.

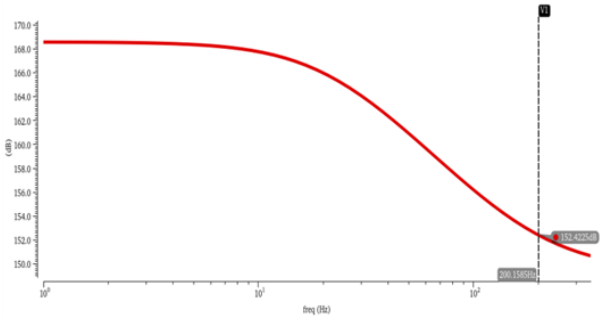

Fig.3 Differential Gain Plot

- Fig. 3 shows the differential gain of the IA. The result shows the gain obtained (>152dB) is better than desired (>100dB). Gain can be adjust by changing the W/L ratio of transistors and by changing the resistors value.

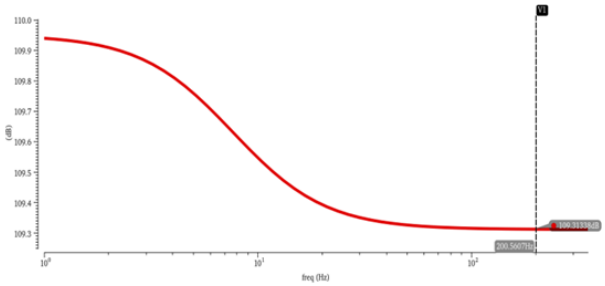

Fig.4 open Loop Gain Plot

- Fig. 4 shows the plot of the open loop gain of the IA, which shows that the obtained value (109dB) is better than the desired value (>100dB).

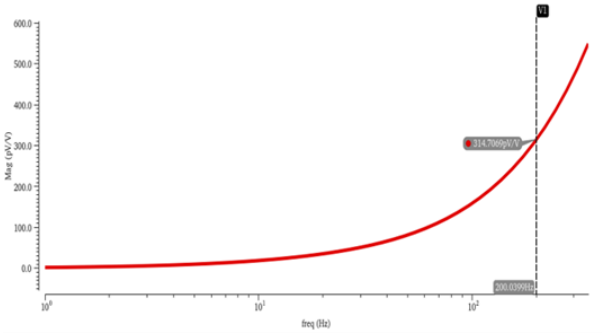

Fig. 5 CMRR Plot

- Fig. 5 shows the plot of the common mode rejection ratio (CMRR) of the IA. The result shows that the CMRR obtained (100dB) is better than the desired value (>70dB).

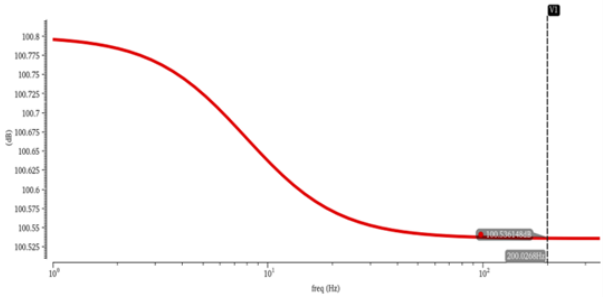

Fig. 6 PSRR Plot

- Fig. 6 shows the plot of the power supply rejection ratio (PSRR). PSRR is measured by applying a small variation in the power supply voltage and observing the resulting change in the output voltage.

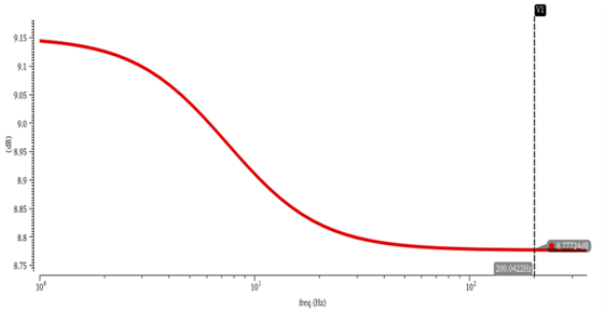

Fig. 7 CM Gain Plot

- Fig. 7 shows the plot of the common mode gain of the IA. Less common-mode gain is essential for high CMRR, which ensures accurate amplification of differential signals while rejecting common-mode noise.

Table No. 3 below shows the result that has been obtained after simulation and also the comparison.

Specifications	[2]	[6]	[9]	[12]	This Work
Supply Voltage (V)	±1.8	±1.8	±1.8	0.8	±1.8
Technology (nm)	180	180	180	180	180
Frequency Range (Hz)	0.1-100	-	-	-	1-200
Gain (dB)	40 ±5	-	-	41	>150
CMRR (dB)	62	82	124	80	100
Open Loop Gain (dB)	72	74.89	20.13	-	109
GBW	-	7.26MHz	.23KHz	114KHz	13.115KHz
Phase Margin (deg.)	60	48	72.16	72	183
Input Referred Noise (uV)	6.8	-	0.12	-	0.991

Table No. 3 Comparisons with previous published work

VI LAYOUT

Layout of Differential amplifier (Fig.8) and instrumentation amplifier (Fig.9) shown below.

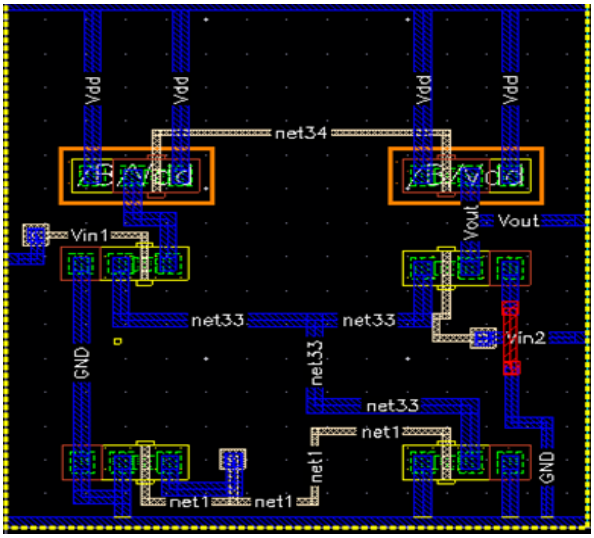

Fig.8 Layout of Differential Amplifier

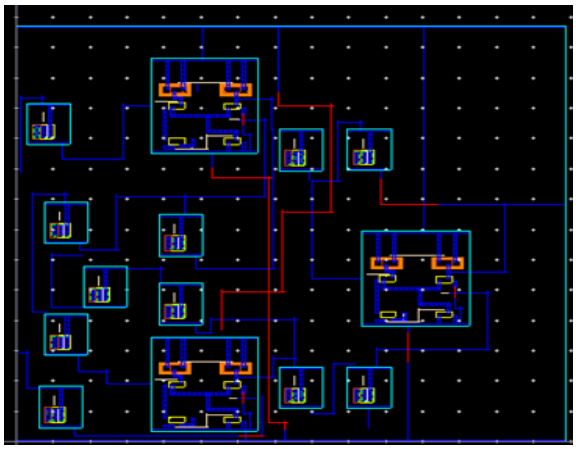

Fig.9 Layout of IA

VII. CONCLUSION

The proposed IA is capable of amplifying weak signals, and its design was validated through simulation. The results, as presented in Table No. 3, show that the IA demonstrates good amplitude performance, meeting all the specified targets except for the gain bandwidth (GBW). The desired GBW could not be achieved due to the selection of components. The choice of active and passive components, such as transistors, resistors, and capacitors, plays a crucial role in determining the gain-bandwidth product. Components with limited bandwidth or non-ideal characteristics can lower the overall GBW of the amplifier.

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