A Navel Rounding Based Approximate Multiplier for High Speed Mac Unit Design

[1]Shaik Nannu Shaida, [2]Shajahan Patan,
[1]M.Tech. Scholar, [2]Associate Professor,
[12]Department of Electronics and Communication Engineering
[12]Narasaraopeta Institute of Technology, Narasaraopet, A.P., India

Abstract: **In this paper we propose a advanced rounding based approximate multiplier (AROBA) which is highly accurate than the conventional multiplier (ROBA). The main concept of multiplier depends on rounding of numbers. This multiplier is applicable for both signed and unsigned numbers. The hardware consists of three major blocks, one block is for unsigned and two blocks are for signed operations. The accuracy of the multiplier is compared with the conventional rounding based approximate multiplier (which are in 2^n) where the advanced rounding based approximate multiplier gives an exact output for the given inputs (irrespective of 2^n) and parameters such as area, power delay, pass rates are been calculated and compared with conventional multiplier where, AROBA gives better results and with the AROBA MAC unit is implemented.**

Keywords- **Approximate multiplier; accuracy; MAC unit.**

I. INTRODUCTION

The crucial part of the arithmetic units are basically built by the multiplier hardware, so multipliers play a prominent role in any design. [1] If we consider a Digital signal processing (DSP) the internal blocks of arithmetic logic designs, where multiplier plays a major role among other operations in the DSP systems [1].So, in the design of multiplier and accumulate unit (MAC) multipliers play an important role. Next, important design in the MAC unit is the Adder. Adders also share the equal important in this design. By the appropriate function methods different kinds of adders and multipliers designs are been suggested. By the approximate computing the designer can make tradeoffs, accuracy, speed, energy and power consumption. In this paper we proposed the modified form of rounding based approximate multiplier which is low power design, high speed and energy efficient.

The multiplier designed was built using the conventional multiplier approach at the algorithm level by considering the rounded input values which are not in the form of 2^n so, we call this multiplier the modified rounding based approximate multiplier. This multiplier can be applied for Signed and Unsigned operations by which three different architectures are implemented. The collection of this paper can be further classified has:

1. Describing the conventional rounding based approximate multiplier (ROBA) and its inaccuracy.
2. Proposed modified rounding based approximate multiplier (AROBA) and its hardware implementation.
3. With the AROBA MAC unit is designed.

The paper further is given has follows: Section II describes the work of other approximate multiplier designs. Section III describes the conventional rounding based approximate multiplier and its inaccuracy. Section IV describes proposed modified rounding based approximate multiplier. Section V describes the hardware implementation. Section VI describes the comparison of AROBA with ROBA multiplier. Section VII describes specifications of AROBA. Section VIII describes the MAC unit design using AROBA. Section IX describes simulations and results. Section X describes the conclusion and Section XI is references.

II. LITERATURE SURVEY

The design of approximate multipliers which were applied in image processing has many applications and they lead to less delay and power compared with the logarithm. Appropriate accuracy-configurable multiplier architecture [2] was proposed for many applications. DRUM6[3] which is having the segment size has 6 helps in the comparison of relative error and pass rates where rounding based approximate multiplier has the best results compared with it. The accuracy of the multipler is compared with the DSM8 [4] where it more accurate than the multiplier and has

relative error smaller than 2%. Many of the error tolerant multipliers are been proposed by two parts one for the appropriate result and the other was for the accurate results. A 32-bit signed appropriate multiplier was designed which were used in many pipelined processors [5] DRUM6 and DSM8 are some of the approximate multiplier compared with the ROBA multiplier which yields in poor results in almost in all the cases. So, the design of AROBA helps in securing better results and with this AROBA MAC unit is been designed.

III. CONVENTIONAL ROUNDING BASED MULTIPLIER AND ITS INACCURACY (ROBA)

The main concept of conventional rounding based approximate multiplier [1] is selecting the *rounded values* for both the inputs which are in form of 2^n and both the inputs should be in the form of $3x2^{p-1}$ (p is considered as arbitrary positive integer value which is greater than 1) in this case of the conventional approach the final value obtained by the multiplier would be less or more than the exact result obtained. Depending on the Ar (rounded input value of A) and Br (rounded input value of B) respectively and the result obtained is inaccurate. Considering the table 1

Table 1: Inputs and rounded values of the conventional multiplier which producing an In accurate result

Inputs	Rounded value Ar	Rounded value Br	Result
A=B	Larger value	larger value	Smaller value than the exact value
A>B	Large value	Larger value	Smaller value than the exact value
A<B	Larger value	Larger value	Larger value than the exact value

So in this paper we design a modified rounding based multiplier which produces the exact output for the given inputs based on the selecting the appropriate rounding values Ar and Br respectively.

IV. PROPOSED MODIFIED ROUNDING BASED APPROXIMATE MULTIPLIER (AROBA)

Algorithm for AROBA multiplier:

The main concept of the proposed modified rounding based approximate multiplier is to design the multiplier so that it takes all values which are irrespective of 2^n . The detailed explanation of the multiplier is described further. Initially let us consider *Ar* as the rounded input value of input *A* and *Br* as the rounded input value of input *B*. Now the multiplication of the A* B is written has follows:

A * B= (Ar * B) (Br * B) + (Ar * B) + (Br *A) – (Ar *Br) - [1]

The basic key point to be considered is the product of (Ar * B) and (Br * B) is complex and the weight of the term would result in small values when compared with the exact numbers so the product of this term can omitted and it also leads to complex hardware design approach. Hence the multiplication can be performed by the following expression as

A * B = (Ar * B) + (Br * A) – (Ar * Br) - [2]

The product terms of (Ar * B), (Br *A), (Ar * Br) can be implemented by three barrel shifters of N bit and one adder is implemented by the parallel prefix kogge-stone adder of N bit and one Subtractor is also needed. If the values of A or B is equal to N where (N=1, 2, 3….N) it has two rounded values N+1 and N. depending on the inputs of A and B the rounded values can be chosen this kind of rounding values are applicable for both A greater B (A>B) and A less than B condition (A<B). Exception that for A equal B (A=B) the rounded input of A and B would be the middle number of N+1 and N i.e. (2N+1)/2 In the conventional rounding based approximate multiplier the numbers (which represents inputs of ROBA) in the form of $3x2^{p-2}$ (where p is arbitrary positive number which is greater than one) are considered and also we have two rounded values in the form of 2^p and 2^{p-1} both the values lead to the same effect but in this case the *larger* value is considered as the rounded value for both the inputs because larger values leads in smaller hardware implementation. But the accuracy of this multiplier is poor and the exact result is not obtained in this case so, we consider the modified rounding based approximate multiplier which is applicable to all N (N=1, 2, 3……N) numbers and the exact output is obtained for the given input. Fig 1.

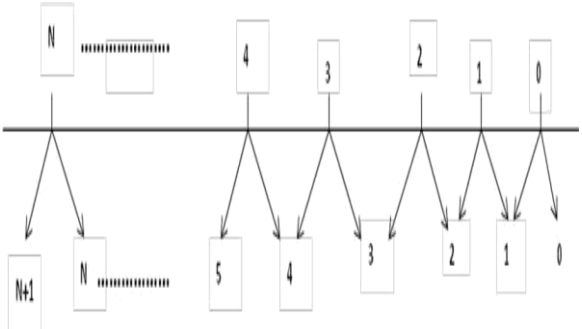

Fig 1: Top numbers represents inputs and below numbers represents the rounded values

V. HARDWARE IMPLEMENTATION OF THE PROPOSED ADVANCED ROUNDING BASED APPROXIMATE MULTIPLIER

Based on fig 2 we have the block diagram for the modified rounding based approximate multiplier. Initially we have a sign detector block where the inputs A and B are given. As in the case of the unsigned numbers the sign detector block can be applied to positive numbers. . But if the signed numbers are considered the absolute values are to be generated and then inputs are to be given. The input of A can have its rounded value has the larger value (N+1) or the smaller value (N). Similarly for input B the rounded value can either be the larger value or the smaller value.

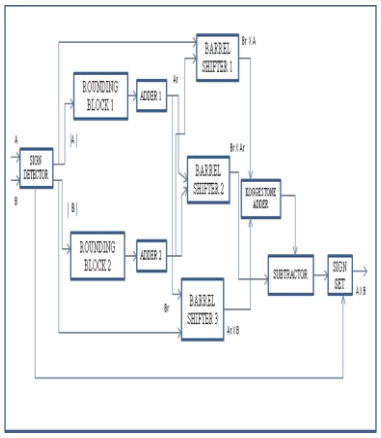

Fig 2: Block diagram of the modified rounding based approximate multiplier

This condition is applicable for both A greater than B (A >B) and for A less than B (A<B) Condition. But for the A equal to B (A=B) the rounded values are considered according to (2N+1)/2. Consider table 2.

NOTE: The rounded values of both the inputs should be compulsory differ from other rounded value eg: for input A its rounded value Ar should be larger value and for the input B the rounded value Br should be smaller value or vice versa for both inputs. Expect for (A=B) the rounded value should be the middle value or (2N+1)/2 which is same for both the inputs. Next block we have a basic adder we can add +1 i.e. (N+1). Now we need three shifters to compute the product terms (Ar *B), (Br * A), (Ar * Br). The amount of shifting is basically done on no of bits we considered and the shifting operation is performed on the rounded values of Ar and Br respectively Then the output of shifter 1 and shifter 3 are given has the input to the adder basically we considered an kogge-stone adder. And the output of the adder and the output of the shifter2 is given has the input to the Subtractor block and finally we have a sign set block which is needed if we considered the signed numbers. For the unsigned it is not necessary and the final multiplication A*B is obtained the output is exact for the given input when compared with the conventional rounding based approximate multiplier it gives the exact result for the input in all the possible conditions.

Table 2: Inputs and rounded values for all possible conditions for modified rounding based approximate multiplier

Inputs	Rounded value Ar	Rounded value Br	Result
A=B	Middle value	Middle value	Exact value
A>B	Larger Or smaller value	Larger or smaller value	Exact value
A<B	Larger Or smaller value	Larger or smaller value	Exact value

VI. COMPARISION OF AROBA MULTIPLIER WITH ROBA MULTIPLIER

Compared with the ROBA multiplier the AROBA gives the exact output for the given inputs in all the possible cases.

Table 3: Comparison of AROBA multiplier with ROBA multiplier

Conditions	ROBA multiplier	AROBA multiplier
A=B	Small value than the exact result	Exact result

A>B	Smaller value than the exact result	Exact result
A<B	Larger value than the exact result	Exact result

EXAMPLES-1:

ROBA multiplier: (unsigned) When: A=12 (3* 2^2), B=6 (3* 2^1)

Ar=2^4 =16 Br=2^3 =8

A * B= (Ar* B) + (Br *A) - (Ar * Br)

Here Ar=16, Br=8

(16*6) + (8*12) – (16* 8)

72 ≠ 64

In the conventional approach the inputs should be in the 3 x 2^{p-1} form and we have two rounded values in the form of 2^p and 2^{p-1} both the values lead to the same effect but here the larger value is considered as the rounded value for both the inputs because larger values leads in smaller hardware implementation.

EXAMPLES-2:

ROBA multiplier: (signed)

When: A= -12 (3* 2^2), B= -12 (3*2^2) Ar=2^4 =16

Br=2^4 =16

A * B= (Ar * B) + (Br * A) - (Ar * Br)

Here Ar=16, Br=16

(16*-12) + (16* -12) – (16*16)

144 ≠ 256

Here -256 is the value since we have a sign set block at the end only positive value is obtained.

EXAMPLES-3:

AROBA multiplier: (unsigned)

When: A= 7, B= 5

Ar=7 Br=6

A * B= (Ar * B) + (Br * A) - (Ar * Br) Here Ar=7 , Br=6

(7 * 5) + (6 * 7) – (7 * 6)

35 = 35

So, from the above examples of AROBA multiplier and ROBA multiplier we can say that the AROBA is more accurate than ROBA and the main advantage is that we can perform multiplication for all the numbers irrespective of 2^n since in the ROBA multiplier only the inputs and rounded values are strictly 2^n but in this AROBA we can perform multiplication for all N inputs (N=1, 2,3….) .

VII. SPECIFICATIONS OF AROBA

In this section we calculate some of the important parameters of the AROBA multiplier and compared them with the ROBA multiplier. Most of the parameters are considered by considering (A=B) condition

1. Maximum Error:

$$\text{Max[err(A,B)]} = \frac{((2N+1/2)-N)*(2N+1/2)-N}{N*N}$$

$$=\frac{1}{4N^2}$$

2. Approximate signed error:

$$\text{err(A,B)} = \frac{(Ar-A)\,(Br-B)}{A*B} + \frac{A+B+1}{A*B}$$

$$= \frac{(N+1-N)\,(N-N)}{N*N} + \frac{A*B}{N*N}$$

$$= \frac{(2N+1)}{N*N} = 1.6\%$$

So, from the table 4 when we compare the specifications of the AROBA multiplier with ROBA Multiplier so, Modified rounding based multiplier is more accurate in all the cases when compared with the ROBA multipliers specifications.

In the fig 5 we observe that the area and PDA of AROBA is more when compared with ROBA. Hence the main concept here is to obtain accurate results which are obtained by AROBA and in almost all cases AROBA achieve better results.

Table 4: Specifications of AROBA multiplier compared with ROBA multiplier

Multiplier	Maximum Error	Error rate	Error significance	Acc inf	Relative error <0.5%	Pass rates [32-bit]	Acc amp
AROBA UNSIGNED	< 0.25%	~0.2%	~0.2%	45.3%	~0.2%	1.05%	0.997%
AROBA SIGNED	1.5%	~0.2%	~0.2%	42.5%	~0.5%	2.3%	0.5%
AROBA AS-SIGNED	1.6%	~0.2%	~0.2%	42.3%	0.09%	5.3%	3.0%
ROBA UNSIGNED	0.1%	~1%	~1%	60.0%	18.1%	1.5e-6	1.77%
ROBA SIGNED	2.66%	~1%	~1%	58.0%	18.1%	2.98e-6	2.58%
ROBA AS-SIGNED	2.35%	~1%	~1%	58.0%	17.9%	>7.45e-7	2.58%

Fig 3: MROBA Power (m W), delay (ns), Energy delay product (EDP in ns X p J) and Energy (p J) of 32-bit AROBA multiplier

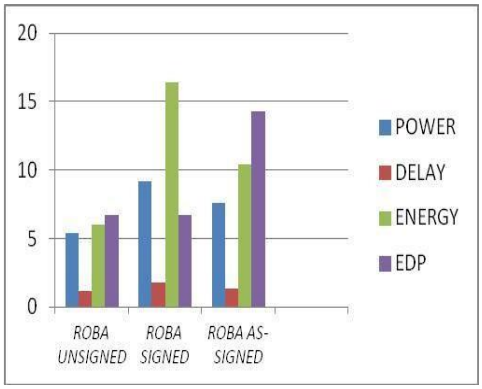

Fig 4: ROBA Power (m W), delay (ns), Energy delay product (EDP in ns X p J) and Energy (p J) of 32-bitROBA multiplier

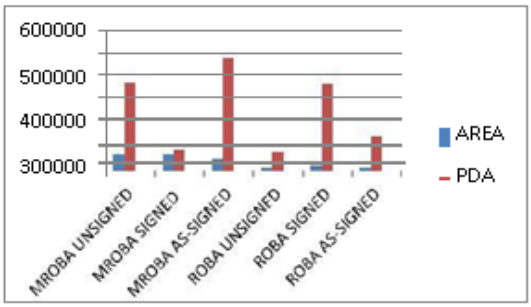

Fig 5: AREA (μM^2) and PDA (p J X μM^2) of AROBA and ROBA multiplier

Basically MAC (Multiply and Accumulate) unit is formed by Adders and Multipliers and the result is accumulated.[7] We find many advantages of MAC in Digital signal processing and many logical units design and implementation. The basic MAC unit using AROBA is shown in fig 6. Here we are designing a MAC unit of 32 *32 bit using AROBA multiplier. The detailed explanation of multiplier can be seen in the above description. The basic MAC has three sub systems namely Multiplier, Adder and Accumulator. The main purpose of multiplier is to find the partial products. [7]Adder helps in adding the partial products generated by the multiplier and finally we have the accumulator to store those values. Here in this implementation kogge- stone adder is been used because when compared to other adder like carry save adder, carry select adder etc kogge stone adder has less delay, minimum fan-out and it performs fast logical addition when compared with the other designs.

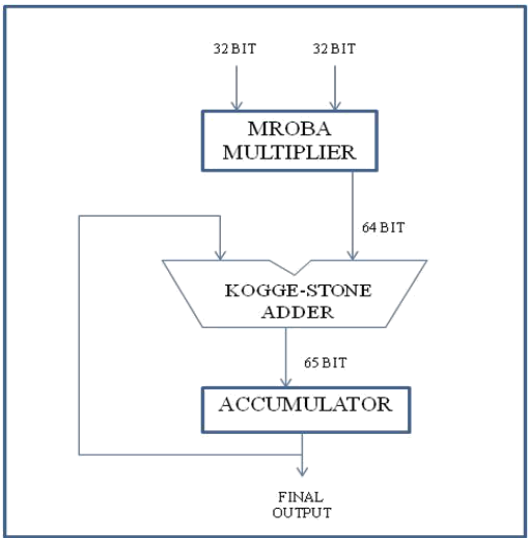

Fig 6: MAC unit design using AROBA Multiplier

VIII. SIMULATIONS AND RESULTS

The AROBA multiplier was designed using the hardware description language verilog Xilinx ISE 14.7 and other parameters like area, power and delay are been calculated in Cadence Encounter at 180 nanometer technology.

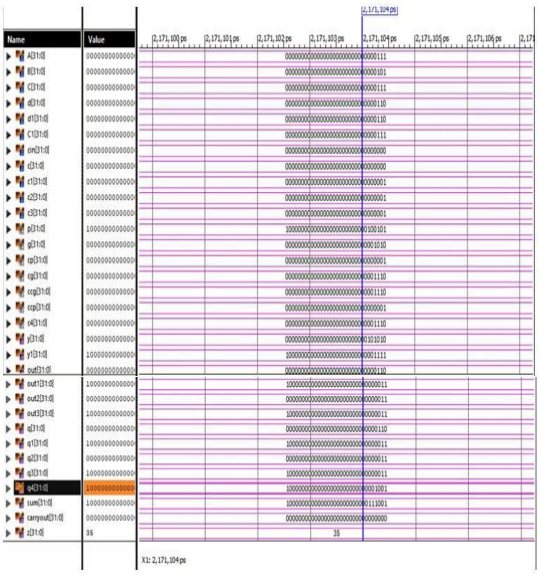

Fig 7: A>B condition for unsigned AROBA multiplier

IX. CONCLUSION

In this paper we propose a Modified rounding based approximate multiplier (AROBA). By modifying the conventional multiplier for the accurate results. Compared with the conventional multiplier the modified multiplier gives exact result to the given inputs and the multiplier can also perform operations which are not in the form of 2^n (as performed in the conventional method) so, the exact result can be obtained for the numbers irrespective of 2^n . The AROBA is designed using Xilinx ISE 14.7 and results are shown above and other parameters like area power delay are been calculated using cadence encounter and the design of MAC unit is also implemented in Xilinx ISE 14.7

X. REFERENCES

[1] Reza Zendegani, Mehdi Kamal, Milad Bahadori,Ali Afzali- Kusha and Massoud Pedram," RoBAMultiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy Energy- Efficient Digital Signal Processing" IEEE transactions on very large scale integration (VLSI) systems syst., pp.1-9, July 2017.

[2] K. Bhardwaj and P. S. Mane, "ACMA: Accuracy-configurable multiplier architecture for error-resilient system-on-chip," in Proc. 8th Int. Workshop Reconfigurable Commun.-Centric Syst.- Chip, 2013, pp.1–6.

[3] MD.Javeed Ahammed, Satyanarayana: "Cmos/Vlsi Circuit For Power Optimization On Portable Devices" IJITEE, October-19, ISSN:2278-3075

[4] D. R. Kelly, B. J. Phillips, and S. Al-Sarawi,"Approximate signed binary integer multipliers for arithmetic data value speculation," in Proc. Conf. Design Archit. Signal Image Process., 2009, pp. 97–10.

[5] A.B. Kahng and S.Kang,"Accuracy-configurable adder for approximate arithmetic designs," in Proc 49th Design Autom Conf (DAC), Jun 2012, pp.820- 825.

[6] S. Deepak, B J kaliath,"Optimized MAC unit Design".Electron devices and solid state circuit IEEEinternational conference on 2012.

[7] P. Siva Nagendra Reddy and M. Saraswathi,"Design and Implementation of FPGA based 64-bit MAC Unit using VEDIC Multiplier and Reversible Logic Gates, Indian Journal of Science and Technology,Vol10(3),DOI:10.17485/ijst/2017/ v10i3/ 109413, January 2017.

[8] S. Narayanamoorthy, H. A. Moghaddam, Z. Liu, T. Park, and N. S. Kim, "Energy-efficient approximate multiplication for digital signalprocessing and classification applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 6, pp. 1180–1184, Jun. 2015