Design & Analysis of Power Efficient Flip Flop and its Application in Nanometer Technology

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***Abstract*—Due to continuous scaling of transistors and increasing requirement of portable equipment, power reduction is of main concern. For design of sequential circuits. flip-flops play very important role. Various existing single edge triggered master slave flip flops and pulse triggered flip flops are examined, simulated, analyzed and optimized in SPICE EDA tool. A novel design will be proposed that consumes low power when compared with the existing literature. The design shall not be only power efficient but area and delay constraints will also to be taken into consideration. The competitiveness of the new design (proposed work) will be shown in terms of power, area and delay with a comparison with existing design. Simulations will also be carried out at different voltage levels to check the viability of the design. Not only voltages, calculations at various data activity (duty cycle) will be obtained for fair comparison and optimum power saving. The proposed work is desired to find application in sequential circuits.**

Keywords: Switching power, CMOS, power consumption, delay, flip-flops

I. INTRODUCTION

Worldwide consumer electronics is growing at a faster pace. Mobile phone in pocket is as powerful as a desktop at home. Power dissipation has become a major concern for semiconductor industry due to increase in complexity of the circuit, speed and density of the device. The requirement for lower power VLSI circuits is driven both by technical needs and business.To achieve low power VLSI circuits following two steps are to be followed:

1 Analysis: for calculations of power dissipation

2 Optimization: the process of generating the best design without violating design specifications.

A Flip-flop is a sequential circuit used for storing binary data. A primary characteristic of sequential logic circuit is the ability to remember the state of the inputs, that is, memory. Two bits which are stored by flip-flops are I and 0 . A flip-flop circuit is controlled by control flags which are incorporated by clock signals. Flip-flops are bi-stable elements which sample - its input data & produce the output data accordingly with respect to a clock edge (P.Joshi et al, 2015). Clock distribution network and flip-flop which are included by clock system are the components which consume highest power that is up to 30% to 60% of the total system power and 90% power consumption is in flip-flops and clock network that is driven by the flip-flop. Mostly edge triggering flip-flop are used as a sequencing element by Application Specific Integrated Circuit (ASIC) design because their timing models are simple (I.A.Khan and M.T Beg, 2013) (S. Kotta and R. Mallavarapu, 2018).

Flip-flop can be categorized as
a] JK flip-flop
b] D flip-flop
c] T flip-flop
d] RS flip-flop

In this study, those flip-flops which belong to D family are discussed. D flip-flop has I input that is Data input and the clock input. Data input value is reflected on the Q output when the clock triggered. Therefore, if the D-input is I, Q output is also I and vice versa.

II.LITERATURRE SURVEY

Dashan Pan et al (2019) demonstrated feedthrough flip-flop and named conditional feedthrough pulse triggered flip flop. The advantage of this flip flop was that the power consumption was highly reduced and delay was optimised. Delay optimisation was done using pre discharging and conditional signal feed through scheme. Power was reduced by feedback controlled conditional keeper. At the output node a pull down path was provided to enhance the driving strength. Result of this design also showed higher energy efficiency. The simulation results of this

design showed 62% delay reduction when compared to conventional transmission gate flip flop, 66% power efficient and energy efficiency of 87%. All these results demonstrated that the new feed through design is a better option for high efficiency synchronous sequential circuits.Ahmad Karimi et al (2019) keeping in view the power requirements and scaling factors of day today's fast pacing electronics, pulse triggered CNT FET based D flip flop was investigated. To achieve this, the idea is to reduce the number of transitions occurring between zeros to ones and one's to zeros. Zero to one transition is optimised using signal feedthrough technique, for 1 to 0 transition the discharging path is renewed which reduces the delay, one of the most novel characteristics of this structure is that the pulse generation here does not depend upon the size of the transistor. The simulation result showed great improvements in power dissipation, Delay as well as in the power delay product. Not only this, the number of transistors where are also reduced when compared to the conventional pulse triggered FF .Chi Yeon Kim and Chul Lee (2019) This letter proposed a readout integrated circuit (ROIC) and uses asynchronous clock gat:ng technique to demonstrate the high dynamic range operation of mid wavelength infrared focal planc arrays. It also uses double edge triggered D flip flop instead of single edge triggered D flip flop in the capacitor reset block. The advantage of using DET D flip flop is that it reduces the error at final output. The input signal and elock signal is controlled by the asynchronous elock gating technique. Using this structure it was observed that the power consumption reduced by 2% when compared to the conventional ROICs. This reduction was observed for low input signal currents.

III. DESCRIPTION OF WORK

Power dissipation in VLSI chip became a parameter that cannot be ignored nowadays. Frequency and density of a device where some factors which were low in the past, but now since the evolution of Ultra Large Scale integration (ULSI) more and more transistors are packed in a chip increasing packaging density. The increased device density and operating frequency resulted in higher power dissipation. M present there stands no slowdown in the growth of processing technology. Needles to mention the growth of consumer electronics from the past 10 to 15 years where battery powered mobile phones and laptops have seen tremendous success. A light weighted. compact and efficient product with higher battery life is the need of the hour.

Flip flops are the basic storage elements bistable in nature, sample input data and produces output data at a given clock. There are many designs of D flip flop available: some designs are efficient at power whereas some are faster i.e. with less delay. Some designs are areaefticient as well. In this research. existing D flip flop designs will' be studied, analysed and simulated in SPICE tool. Nanometre technology will be adopted for all the simulations. Various parameters like power, delay. Power Delay Product (PDP) of these designs with variation of supply voltage and temperatur, will be obtained. A novel D flip-flop design will be proposed. Again various parameters of this new design with varistions in temperature and supply voltage will be obtained. The results of the novel design will then be then compared with the existing designs which should show the capability of new design to be a viable option for the sequential circuits.

3.1 Power Consumption in CMOS:

The increased importance of mobile systems and, consequently, the energy consumption (and consequently thermal dissipation) in dense ULSI chips should be limited to quick, creative low-power advancements in recent years. The main factors for these advances are mobile appliances that require a low energy dissipation and a high output, such as laptops, [3] mobile devices and private digital assistants (PDAs). In most situations, the requirements for low power consumption should be fulfilled with equally tighter objectives of high chip density and high output. Thus, low power digital style. The limited battery duration generally puts extremely stringent requirements on the general energy usage of the moving system. While new kinds of reversible battery such as binary nickel-metal composites (NiMH), with larger energy capacity than the traditional Nickel cadmium batteries, are being developed, there is no provision for a revolutionary rise in energy capacity in the near future. The energy density supplied by modern battery technologies (i.e. NiMH) refers to 30 DH/lb which remains low visible to growing applications of mobile systems. Reduce the dissipation of the integrated system. Accordingly, a further key aspect of reliability added flavor is a reduction in energy usage. The methods used for square metering are large-scale, from the device technique level to the level of control with low energy consumption in digital systems. Device features (e.g.

threshold voltage), geometry of the unit, and square interconnections assess key variables for reducing installation consumption. Measurements of circuit level, such as the right selection of circuit type designs, voltage swing reduction and continuance procedures may be accommodated at the level of the semiconductor back energy dissipation. [4] Incorporate specific the measurements of the circuit or transistor level that may be used to reduce the dissipation of digital integrated circuits. Numerous energy consumption sources are well discussed and techniques for reducing waste from the plant have been presented. System level problems such as pipeline replication and hardware (parallel processing), and the effect of such measures on power supply will be investigated.

3.2 Switching Power Dissipation

This component is an installation which is dissipated when a switching event, that is, after a logical transition is made to the power node voltage of CMOS gate [5]. The switching power is wasted in digital CMOS circuits, once energy is taken from the facility offering to power the output node. The power node voltage generally transfers from zero to VDD throughout this load-up portion and simply dissipates the energy derived from the factory offer as heat within the conductive PMOS transistors. The power disconnection of the switch is also a linear operation of the clock frequency, although the general system performance would be significantly reduced only by lowering the frequency. Therefore, reducing the clock frequency would only be practical when different indications imply the overall outturn of the system. One of the most often utilized measurements for low power is the drop in power supply voltage [6]. While this is generally terribly successful, a great many important problems should be solved by themselves in order to avoid sacrificing system performance.

3.3 Short-Circuit Power Dissipation

The dissipation of the switch power discussed above is purely due to the energy needed to activate parasitic capacity in the circuit, and hence the switch power is independent of the increases and decreases in the input signals. If, however, each NMOS and indeed the PMOS transistors inside the circuit are operated by input voltage waveforms at finite times, each of the NMOSs can simultaneously lead for a short amount of your time throughout the switch, thus forming an immediate current path between the facility offer and thus the present part passing through the earth.,[7] The whole switch does not charge the capacity in the circuit and is consequently considered to as the current section of the short circuit

IV. PROPOSED MODULE DESCRIPTION

The Flip flips we saw in current style are affected by the problems that all of them face a time schemes of zero to one control and data in an analogous worst scenario. In order to increase this latency the planned style uses a proof-feed approach. Like the style of the SCDFF, the proposed style combines a static latch structure with a conditional discharge theme to minimize needless node shifts. There are nevertheless three important differences, each of which results in a unique. TSPC latch structure, creating a different projected style from the preceding one.

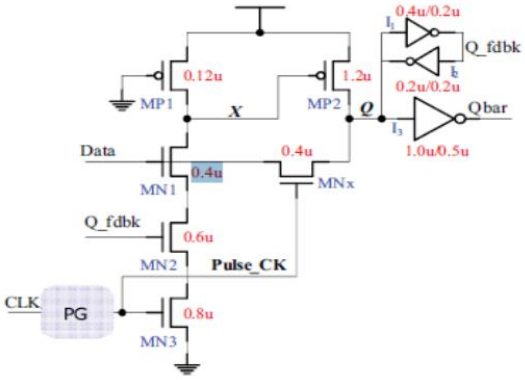

Figure 1: Proposed flip flop

The initial phase of a TSPC lock uses a weak electrical MP1 pull-up with a gate linked to the bottom. The load keeping circuit for the internal node X will be saved, which gives the pseudo-NMOS logic trend. This method decreases the load capacity of node X together to simplify the circuit. Secondly, an electronically controlled pass transistor MNx is included so that the latch node letter is directly driven by the input file. This further transmitter allows the auxiliary signal from the input supply to the letter node together with the pull-up of the electronic transistor MP2, at the second stage of the TSPC latch electrical converter. The level of the node is forced to reduce the transition time of information rapidly. Thirdly, the second-stage electric converter pull-down network is completely eliminated. The newly used electronic transistor MNx offers a download route. Thus, the role life of MNx is twice as important, that is, over zero to one transitions, the additional driving to node letter and the unloading of node letters via "1" to "0" transitions. The planned-type load keeper (two inverters), a pull-down network and electrical converter are the circuit

savings of the projected style compared to the loop structure used in the SCDF-type.The proposed model Shown in figure 4. Once the "I" to "0" transition of knowledge takes place, the SCDFF also activates the clock pulse on the electrical transistor MNx and the input step discharges the node letter through this route. The input supply does not carry the only actual discharge duty, like the case of "0" to "1." The loading result for the input supply isn't relevant as MNx is enabled for under a brief time. In particular, this discharge does not correlate to the fundamental route delay and does not require a tweak to strengthen the speed of the electronic transistor. Moreover, because the keeper logic is positioned on the node letter, the release duty of the supply is elevated as soon as the maintainer logic status is reversed. 4.1 Double Edge Triggered Flip Flop At the rising and falling edges of the clock the flip-flop input is transferred to the output. The consumption of the facility is lowered when the electronic transistor is used. At each perimeter at the same moment, the information will be activated, thereby reducing clock power. The distribution of the clock power is important disadvantage, and hence the most prevalent technology is. In comparison to single edge triggering, this technique delivers greater turnout. For twoedge triggers, the frequency needed is 0.5 in comparison with the single-edge triggering. The dual edge causes the flip flop, thereby decreasing the delay to greater operating speed. It conjointly reduces space by triggering each positive and negative edge at the same time. It decreases space by simultaneously activating every positive and negative edge. Together, the pulse noise sensitivity is reduced. The measurement square of the inverters used in the double edge caused a flip flop and not a NAND door. The NMOS is provided on both sides and the clock is added. When the entry is supplied, the info on each edge is activated by the electrical converter. Therefore, when a clock is supplied, the information transfer is faster. Thanks to the gate, the current style occupies plenty of room. The anticipated style because space is reduced by just electrical converter. In order to prevent switching at an internal node, the design also uses a static latch structure and a conditional discharge technique. This system uses a standard explicit type pulse-triggered flip-flop to solve the lengthy discharge route problem. There is no data transition when a clock pulse appears. Table1 illustrated the Power Comparisons.

Table1: Power Comparisons

Parameter	Power (Watts) at Time 1.8328e-007	Power (Watts) at Time 1.8328e-007
Average power consumed	->1.87526e-003	1.0948176e-004
Max power	8.117876e-003	6.543203e-003
Min power	1.054530e-003	6.658484e-007

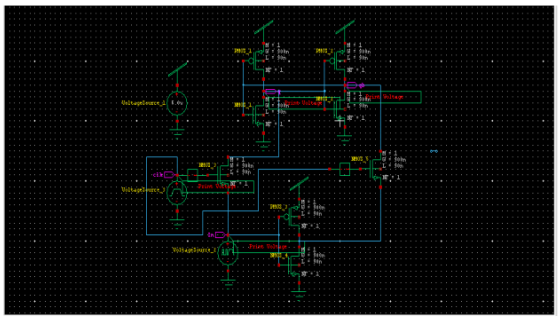

Figure 2: Schematic results of proposed scheme

The information activates either on a positive or a negative edge in single edge triggered flip flop. To convey the information it takes several cycles. The existing style of each generating gate is used. When the info is sent from zero to one with one to zero, the inverters cut down the dump path. Figure 2 shows the Schematic results of proposed scheme.

Table2. Power comparisons at different time

Parameter	Power (Watts)
Average power consumed	-> 2.902832e-004
Max power	1.433808e-002
Min power	4.514772e-007

V. CONCLUSION

The single edge triggered true one-stage flip flop and double edge triggered flip flop with pulsing feed system are designed and analyzed with low power and speed. During this period we also built circuits based on existing literature such as Ep-DCO, CDFF, S-CDFF and MHLFF. This design is also implemented by using the double edge clocked technique. Substantial power savings in the clock distribution network can be achieved by reducing the clock frequency by one half. Hence it is concluded that this design achieves low power consumption. Shift registers has been constructed to show how the power will decrease as the sharing of a single pulse generator among multiple flip- flops is increased can be extended for the future work.

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