Design and Area verification of CMOS Two Stage OP-AMP in 45nm Technology

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***Abstract*—The design and area verification of a two-stage operational amplifier (op-amp) that is designed for effective functioning in integrated circuits are the main goals of this research. High gain, stability, and low area consumption while following industrial norms are among the goals. Techniques include a thorough design approach that balances power, speed, and area limitations employing CMOS technology, Cadence simulation, and layout optimization. To guarantee the intended functionality, important parameters including gain, phase margin, and power dissipation are regularly monitored. The results show that the developed op-amp raises 58 dB with a 63 degree phase margin while taking up very little chip space, making it ideal for small and effective circuit designs. Analog signal processing, data converters, and low-power applications are among the uses, and there is potential for future improvements in scaling and integration for smaller technology nodes..**

***Index Terms*--Two-stage op-amp, CMOS design, gain stability, area optimization, analog circuits**

I. INTRODUCTION

The operational amplifier is currently one of analog circuit design's most important and versatile parts. Operational amplifiers have a forward gain high enough that, when negative feedback is added, the closed-loop transfer function is practically gain-independent. Operational amplifiers with two or more gain stages are commonly used when higher gains are needed. One of the most popular kinds of op-amps is the two-stage op-amp. Bipolar op amps and their CMOS counterparts have very similar designs. The differential input stage improves offset and noise performance by contributing a sizable portion of the total gain. If the op-amp is driving a low-resistance load, the second stage must be followed by a buffer stage that attempts to lower the resistance. Biasing circuits are provided to ascertain the optimal operating point for each transistor in its quiescent condition. Compensation is required to achieve stable closed-loop performance.

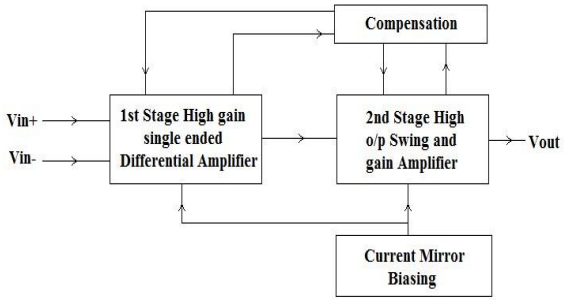

Fig1. General block diagram of two-stage Op-Amp

II. LITERATURE SURVEY

The design and execution of a two-stage operational amplifier (Op-Amp) are presented in Paper [1]. The PTM 45 nm CMOS technology was used to design the circuit. The design is area-optimized because it uses a relatively limited number of transistors. The amplifier's achieved open loop gain is 76 dB. With a 1000K ohm resistive load and a 10 pF capacitive, the phase margin is 50 degrees and the unity gain bandwidth (UGB) is 10 MHz. This circuit's high bandwidth makes it appropriate for high-speed applications, while its high gain allows it to function effectively in a closed-loop feedback system. The amplifier has an average power consumption of 0.167 µW and a slew rate of 8 µ/us.

Paper [2] addresses the issues with this conventional approach and demonstrates how the miller compensation of opamp has been explained intuitively. By dividing the second stage, an area/power efficient method has been suggested. In order to increase stability, the splitting adds an additional zero to the transfer function. This technology was simulated using Spectre and realized in 45nm CMOS technology. According to simulation data, the suggested circuit uses half as much capacitance as the Miller approach. The circuit uses a 1.5V supply to draw 320uA of current and takes up 0.003108mm2 of silicon space.

In [3] Paper, An operational amplifier's gain is a crucial characteristic that determines its accuracy and

speed. There are numerous design strategies (such as cascading, gain boosting, etc.) that can raise an OPAMP's gain. A body bias technique is used in this work to increase gain and speed up an OPAMP's operation. Technology scaling has no effect on the transistor's threshold voltage, which results in a lower DC gain for an OPAMP and slows down its operation. OPAMP shows enhanced DC gain because the body bias approach overcomes the threshold voltage limitation of technology scaling. With a DC gain of 57.83 dB, the suggested OP AMP is 5 dB higher than the traditional OP AMP design that uses a transistor pair with a gain bandwidth of 74 MHz. The op-amp is constructed using 45nm CMOS technology; a 1.3V power supply was used for simulation and results in Cadence.

In paper [4] a low opamp compensation technique suitable for the bio-medical application has been proposed and intuitively explains the existing compensation techniques. The Present technique relies on the passive damping factor control rather power hungry damping. Implemented in 45nm CMOS technology and simulated with Spectre. Simulation results show that 100dB dc gain, wellcompensated 25MHz bandwidth opamp while driving a 1pF capacitive load. Draws with 12uW power consumption from 1V supply and occupying 0.004875mm2 silicon area.

III. DESIGN PROCEDURE

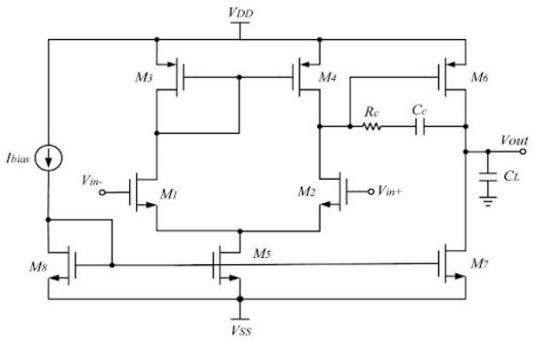

Fig.2 Circuit Diagram of Two-stage Op-Amp

1) The design procedure begins by choosing a device length to be used throughout the circuit.
2) The minimum value for the compensation Capacitor Cc should be 0.22 times more than CL to get a phase margin of 60º.
3) Based on slew rate requirements the value of the tail current I5 is determined.
4) The aspect ratio of M3 can be determined by the positive input common mode ratio range by using the equation (vii).
5) The aspect ratio of M1 can be determined through transconductance gm1 by using equation (iv).
6) To calculate the saturation voltage of transistor M5 negative input common mode ratio range is used by equation (viii).
7) For a reasonable phase margin, the value of gm6 is approximately ten times the input stage transconductance gm1.To achieve proper mirroring of the first stage current mirror load of M3 and M4 requires VSG4 VSG6. By VSG6 we can get the aspect ratio of M6.
8) The device size of M7 can be determined from the I6 current flowing through M6 and balanced equation.
9) The total amplifier gain against the specifications is given by[1] .

$$\text{Av} = (2)\ (gm2)(gm6)$$
$$I5(\lambda 2+\lambda 4)I6(\ \lambda 6+\lambda 7)$$

Relationships describing the op-amp performance[1]:

$$\text{Slew rate SR} = \frac{I_5}{C_c} \quad .(i)$$

$$\text{First} - \text{stage gain Av1} = -\frac{g_{m1}}{g_{ds2}+g_{m4}} = \frac{-2g_{m1}}{I_5(\lambda_2+\lambda_4)} .(ii)$$

$$\text{Second-stage } A_{v2} = \frac{-g_{m6}}{g_{m6}+g_{m7}} = \frac{-g_{m6}}{I_6(\lambda_6+\lambda_7)} \quad .(iii)$$

$$\text{Gain bandwidth GB} = \frac{g_{m1}}{C_c} \quad .(iv)$$

$$\text{Output pole } p_2 = \frac{-g_{m6}}{C_L} \quad .(v)$$

$$\text{RHP zero } Z1 = \frac{g_{m6}}{C_c} \quad .(vi)$$

$$\text{Positive CMR Vin(max)} = V_{dd} - \sqrt{\frac{I_5}{\beta_3}} + |V_t|(\max) + V_{T1}(\min) \quad .(vii)$$

$$\text{Negative CMR Vin(min)} = V_{ss} + V_{t1}(\max) + V_{Ds5}(\text{sat}) + \sqrt{\frac{I_5}{\beta_1}} \quad .(viii)$$

$$\text{Saturation voltage } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{ds}}{\beta}} \quad .(ix)$$

IV. SIMULATION RESULTS

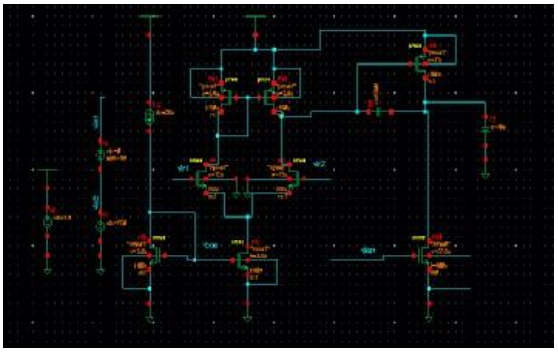

Fig.3 Schematic diagram of two-stage CMOS Op-Amp

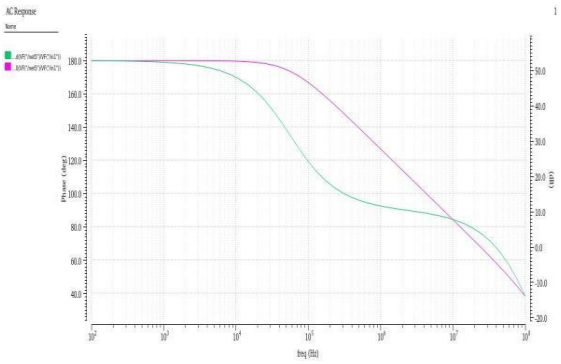

Fig.4 Gain and Phase plot of Op-Amp in 45nm

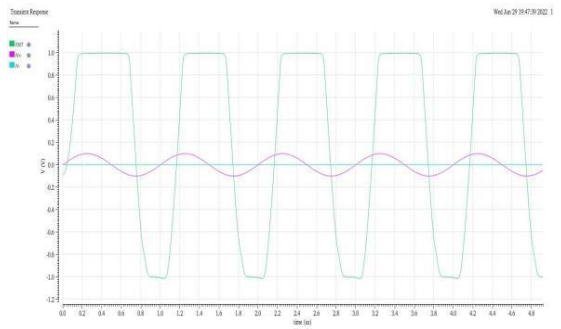

Figure 5: Transient analysis of op-amp

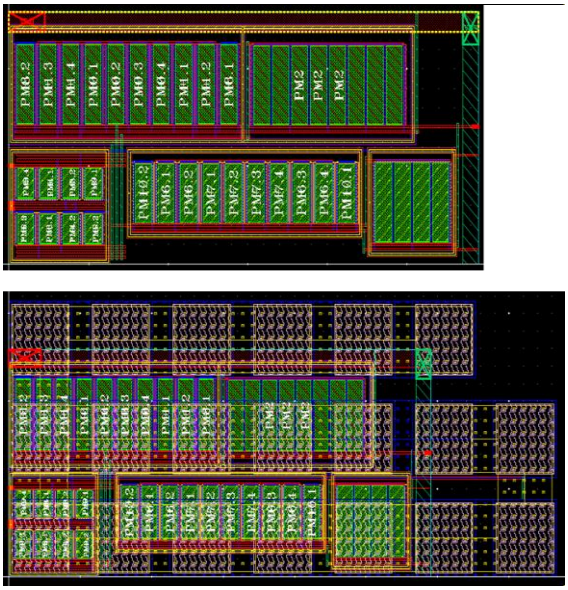

Fig.6 Final Layout (With and Without Capacitor)

Fig3. shows a schematic diagram of a two-stage CMOS op-amp which was designed according to the procedure. For the frequency response plot, an AC signal of 1V is swept with 5 points per decade from a frequency of 100Hz to 100MHz. Fig4 illustrates the frequency response of 45 nm op-amp which shows a dc gain in dB versus frequency in Hz(in log scale) and phase margin of Op-Amp in open loop.

The DC gain is found to be 58dB and the phase margin is 600 which is good enough for an Op-Amp operating at a high frequency. A DC gain of 58 dB at a unity gain frequency of 36.12MHz and a slew rate of 20v/µs is excellent for an Op-Amp when all the other parameters are also set at an optimized value. Fig5 shows the transient analysis of 180nm CMOS Op-Amp.Fig.5 illustrates the frequency response of 45nm op-amp which shows a dc gain in dB versus frequency in Hz(in log scale) and phase margin of Op-Amp in open loop. The DC gain is found to be 45 dB and the phase margin is 750 which is good enough for an Op-Amp operating at a high frequency.

Table 5.1: Results after Simulations

Parameters	Desired value	Obtained
Dc gain	>=60dB	58dB
Gain Bandwidth	>=30 Mhz	36.12 Mhz
Phase Margin	$> 45^O$	$> 66^O$
Slew Rate	$> 5V/\mu sec$	$> 20V/\mu sec$
CMRR	$>= 60dB$	$>= 58dB$
Power Dissipation	$<= 300\mu W$	$261\ \mu W$
Load Capacitance	2pF	2pF
ICMR(max,min)	1.6V , 1.8V	..–
Area occupancies	”’	601.31 μm^2

IV. CONCLUSION

The two two-stage op-amp was designed and work on its area optimization has been achieved, While working on this objective the two-stage op-amp was designed with the implementation of different blocks of the op-amp i.e. differential pair, current mirror, and common source amplifier. Each block was checked for functionality by simulating it and obtaining the appropriate waveforms. The characteristics of op-amps have also been studied throughout the entire process.

Matching methods were followed while doing the layouts, for the current mirror inter-digitized method was followed whereas, for the differential pair, the common Centroid method has been followed. Also, dummies have been placed around the real devices, and drain sharing has been carried out wherever possible. .The layout has been done in 45nm technology and the area on optimization is 381.186 µm2 without capacitor and 601.31 µm2 with capacitor.

REFERENCES

[1] Ranjan Kumar, Mukesh Maheshwari, " A 45 nm Low Power Two Stage Cmos Operational Amplifier" Fourth International Conference on I-SMAC / 07-09 October 2020."
[2] R. Nagulapalli, K. Hayatleh, S. Barker, B. Naresh Kumar Reddy, " A two-stage opamp frequency Compensation technique by splitting the 2nd stage"
[3] Sanjay Kumar, Pathak Jay, Rajendra Prasa, " Gain Improvement Of Two Stage Opamp Through Body Bias In 45nm CMOS Technology"
[4] Srilakshmi Ravali Madabhushanam, Lalitha Malladi, Soumya Reddy Gudepu, "Design High gain dual stage operational amplifier using CMOS 45nm Technology"
[5] R. Nagulapalli, K. Hayatleh, S. BarkerB. Naresh Kumar Reddy, B. Seetharamul, " A Low Power Miller Compensation Technique for Two Stage Op-amp in 65nm CMOS Technology"