Design and Analysis of Ripple Carry Adder using MOSFET Current Mode Logic Circuit with Power Reduction Technique

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***Abstract*—MOS current mode logic (MCML) is a new alternative for the traditional CMOS logic style for mixed signal analog applications. The MCML library shows the less power dissipation at the operating frequency of higher values and more in comparison to the conventional CMOS style. It is nearly impossible to create robust, power efficient and cost-effective design and time to market product. To reduce this problem there are many MCML techniques are used and found the success.**

I. INTRODUCTION

The demand for electronic circuits with extremely low supply voltages and power consumption is important in development of microelectronic technologies. In many applications, additional requirements appear, particularly the extreme speed or the accuracy of signal processing. Simultaneous fulfilment of the above demands is problematic. In the last two decades, the evolution of modern applications of analog signal processing has followed the trends of so-called current mode, where signals, representing the information, are in the form of electric currents. In contrast to the conventional voltage mode, which utilizes electric voltages, the current mode circuits can exhibit under certain conditions among other things higher bandwidth and better signal linearity. The current mode approach for analog signal processing circuits and systems has emerged as an alternate method besides the traditional voltage mode circuits due to their potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption and high operating speed. Till recently, CMOS technology was being used extensively to implement digital circuits. CMOS has the advantage that its static power consumption is extremely less. It uses power only when charging and discharging. That is, dynamic power consumption of CMOS logic is considerable.

Ripple carry adder is the basest and simplest design among the family of the long chain adder. The following adder can be designed by cascading the n number of full adder cells. For generating a carry for the next stage, one bit adder generates the sum along with the ripple

result for next stage. Here the result of one stage,

i.e. carry_out is fed to the next stage carry_in. However, being the simplest one, the ripple carry adder could not be used for the long chain of adder as it will not be sufficient. The main drawback has shown by the following adder that its delay increases as the adder chain extends. Ripple carry adder shows the case of worst delay scenario when carry line goes through all the participated stages of adder block rail from least significant bit right to the most significant bit [1]. The MCML universal gate, the popular topology due to the relatively small size and versatility has an asymmetric topology and has considerable robustness. The irregularity at the gate terminal of MCML logic style degrades the overall circuit functionality. It increases the complexity of any prospective MCML model of any gate for simulation [2].

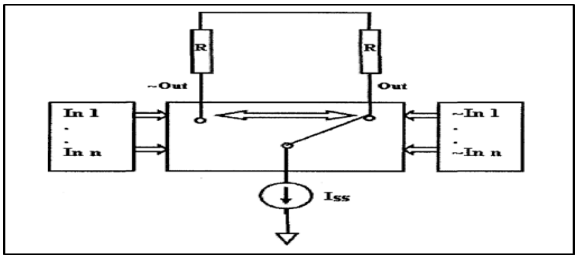

Fig 1: Basic MCML operation

Basically, MOS current mode logic (MCML) is a digital realization of the differential amplifier. As displayed in Fig 4.1, by transferring the current form one stage to another stage, the given logic can be realized [3].

II. POWER REDUCTION TECHNIQUE

For any digitalized circuit, power can be characterized as the key element for boosting the performance. Any changes in terms of power consumption make a device more reliable and competent. It is also very important to know not only how to calculate total power consumption, but it is also needed to understand how factors such as input voltage level, input rise time, fall time, power-dissipation, input voltage swing, internal capacitances, and output loading affect the power consumption of any device. The MCML technique also requires lesser power supply and can work on high operating frequencies. The power consumed by devices is divided into the different categories. This function statement addresses the different nature of power consumption in a MCML logic circuit, and, finally, the purpose of entire power consumption in a MCML appliance [4].

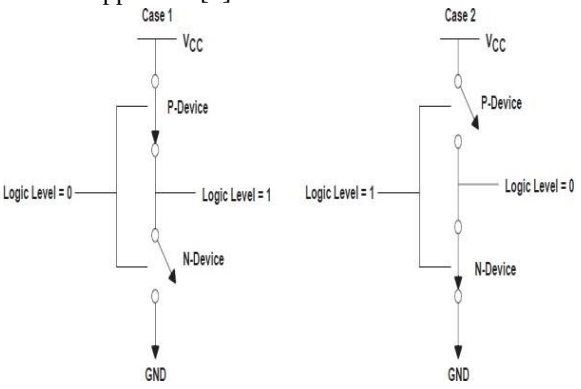

Fig 2 Static Power Consumption for the inverter

In general, all of the low-voltage devices have a CMOS inverter circuit design in their input and output stages and also used in test bench circuit. Therefore, for a obvious understanding of static power consumption in inverter circuit, the CMOS inverter modes is referred as shown in Fig 2. It is built with the connection of a pair of PMOS and NMOS transistors. As shown in Fig 3.1, if the input is at logic '0', the n-MOS device is OFF, and the p-MOS device is ON (Case 1). The output voltage is VCC or logic '1'. Similarly, when the input is at logic '1', the associated NMOS device is biased ON and the PMOS device is OFF. The output voltage is on 'GND' terminal, or logic '0', it is to be noted that one of the transistors is always in 'OFF' stage when the gate is in either
of these logic states. Since no current are flowing into the gate terminal, and there is no dc current conducting path from VCC to GND, the resultant steady-state (quiescent) current is at 'zero' stage, therefore, static power consumption is zero. There are three main sources of static power dissipation, diode leakage current, sub threshold current and bias current.

III. RIPPLE CARRY ADDER

Ripple carry adder is the basest and simplest design among the family of the long chain adder. The following adder can be designed by cascading the n number of full adder cells. For generating a carry for the next stage, one bit adder generates the sum along with the ripple result for next stage. Here the result of one stage,
i.e. carry_out is fed to the next stage carry_in. However, being the simplest one, the ripple carry adder could not be used for the long chain of adder as it will not be sufficient. The main drawback has shown by the following adder that its delay increases as the adder chain extends. Ripple carry adder shows the case of worst delay scenario when carry line goes through all the participated stages of adder block rail from least significant bit right to the most significant bit [1].

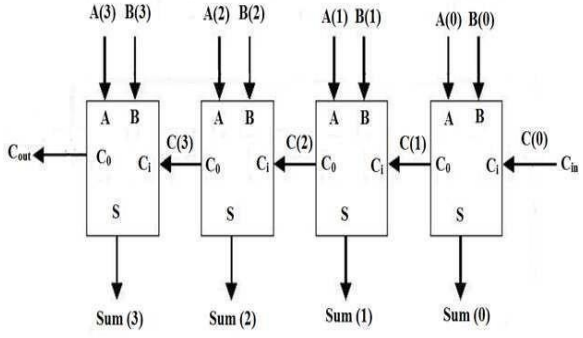

Fig. 3 4-bit Ripple Carry Adder

In the ripple carry adder, one gets the sum output of the most significant bit, while generating the carry by the previous stage. Here the result would be known,

after the carry generated from the previous stage. This is why; the sum of most significant is generated after the carry wave signal is flow through the adder to the most significant bit from the least significant bit. As a consequence, the final result of sum and carry are generated with the sizeable delays [5].

IV. RESULTS AND DISCUSSION

Fig 4 shows the symbolic representation of 4-bit Ripple Carry Adder (RCA). Here, three initial inputs such as bit A, bit B, and bit C, has been supplied to the first full adder in the adder chain. This full adder spawns the carry and sum as an outcome. The output is then supplied to the next adder in the adder chain, acts as third input along with bits A and B and so on. This process continues until the fourth adder where the final carry and sum is spawned for 4-bit RCA. The objective of this design is to calculate the delay on sum signal caused by the process of propagating the carry signal. Here, all the delay of all the sum signals is evaluated and determined. In the MCML design, for driving the outputs from the ripple carry adder, buffers are also added in order to get the less rippled signals. The delays are calculated here for the sum signals. A 4-bit RCA is an important realization for having understood the working nature of MCML in large designs [7].

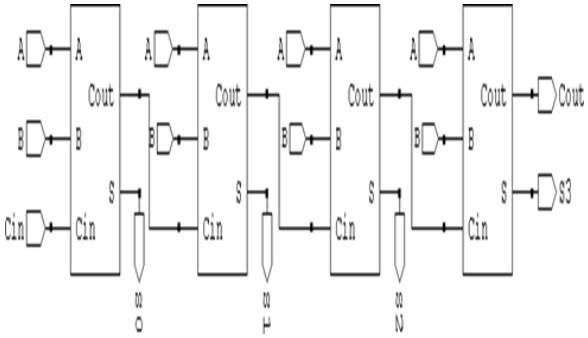

Fig 4: Generalized setup for 4-bit RCA Adder

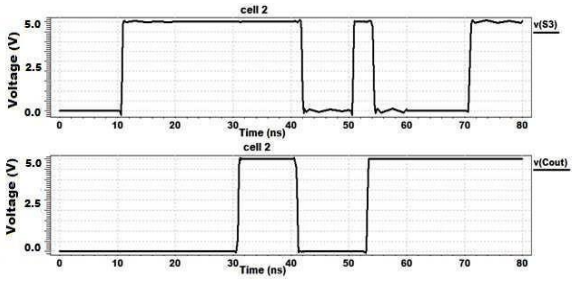

Fig 5: Waveform for the Mirror CMOS RCA Circuit for S3, Cout

The final sum and carry pointer is produced and displayed in Fig 6 and gives the results. The Mirror based design is dependent upon the identical image. Here, 'AND' and 'OR' gate is also used for refraining the particular bits and filters the others. The intermediate sum and carry pointer is produced and displayed in Fig 5 and

gives the results. The MCML based design is dependent upon the bias voltage.

This circuit only works while the bias voltage is given to the circuit. The circuit works only for the particular pulse width, and for the rest of waveform, it is off. This bias voltage works more like a clock signal in the domino circuit network with the little difference that MCML design do not have to put inverter at the output. So, this is helpful in power saving.

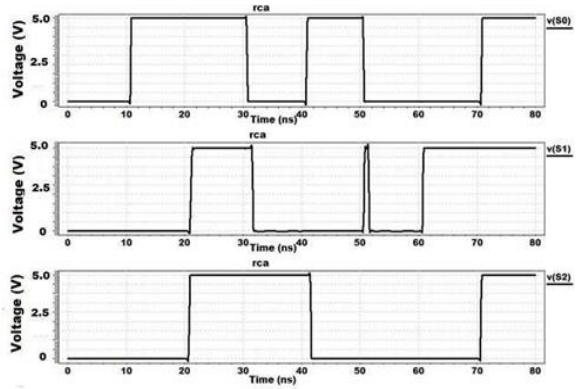

Fig 6: Waveform for the Proposed CMOS RCA Circuit for S0, S1, S2 Bits

The voltage waveform is shown, in Fig 7 for S3 bit and Cout bit. The ripple showed in sum bit is due to the delay induced by the previous state. The following waveform displays the placement of bits according to the intermediate carry bit which is extracted from the second intermediate stage.

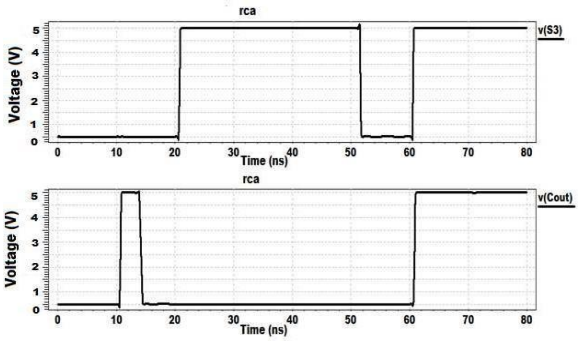

Fig 7: Waveform for the Proposed CMOS RCA Circuit for S3, Cout Bits

Delay, ns	S0	S1	S2	S3 6.
Mirror CMOS	14.521	20.817	27.124	33.437
Proposed design simulated results	0.071	0.142	0.126	0.151

Table 1 Comparison of delay of sum bits of RCA designs (for 5Volts)

Table 1 shows the estimation of sum bits for all RCA designs. From the above comparison it can be concluded that proposed design shows the improvement in delay from other approaches. The following ripple carry adder results are simulated and carried out for voltage supply of 5 volts. This table 1, analyses the results for the consumed power and also for the reduced delay and total power delay product (PDP). The following results shows the MCML based full adder-based ripple carry adders are also power efficient circuits and reduce the delay to the manageable limit. There are various applications where is the delay reduction is the basic requirement and also requires a circuit which works for the mixed signal approach. RCA is one of the applications where when it is used somewhere in the other application requires the vast reduction in power supply. Here the RCA is supplied with 5V power supply, and even then, it shows the vast reduction in the delay for each bit. For the S0 bit it shows minimum delay and for the S3 bit, it shows maximum delay. It is because of the fact that while processing the stage, it faces the lag from the previous input stage.

V. CONCLUSION

The MOS Current Mode Logic (MCML) method is adopted to acquire the set goals. The goal was to reduce the number of transistors used in design, reducing total consuming power and delay, also the corresponding power delay product (PDP). The objective is also to reduce the delay from the carry terminal as the carry is fed to the next stages in the large adders. Also, the sum signals are compared for the 4-bit ripple carry adder (RCA). By analyzing the results, we can conclude that the MCML based adder is most efficient adder. The following adders were simulated at 50 MHz.

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