© February 2025 | IJIRT | Volume 11 Issue 9 | ISSN: 2349-6002

Design and Simulation of 8-Bit Ripple Carry Adder using 45nm

Pratiksha P Hosamani[1], Nikhil Kulkarni[2], Deepak Sharma[3]

[1]*Student of Electronics and Communication Engineering, College of KLS VDIT Haliyal- 581 329, Visvesvaraya Technological University, Jnana Sangama, Belagavi – 590 018, Karnataka, India.*

[2,3] *Assistant Professor, Department of Electronics and Communication Engineering, College of KLS VDIT Haliyal- 581 329, Visvesvaraya Technological University, Jnana Sangama, Belagavi – 590 018, Karnataka, India.*

***Abstract*—For the Modern Digital Systems the computational performance can be enhanced by an efficient Arithmetic unit. The proposed work describes about the design and implementation of the adder Architectures which are proposed in this work using XOR, AND, OR Logic and Second by NAND Logic with 45 nm CMOS technology. Adders play a crucial role in processors, digital signal processing, and various computational applications, making their optimization vital for performance improvement. The Ripple Carry Adder (RCA) is known for its simplicity and minimal area usage, as it generates the sum and carry sequentially. However, this architecture suffers from significant propagation delay, which increases linearly with the number of bits, making it less suitable for high-speed operations. The design utilizes CMOS logic gates optimized for minimal power consumption and delay reduction. Cadence Virtuoso with 45 nm process technology is utilized in the proposed work.**

***Index Terms*—Ripple Carry Adder (RCA),8-bit Ripple Carry Adder.**

I. INTRODUCTION

8-bit Ripple Carry Adders are fundamental components in digital systems used for performing arithmetic operations such as addition. The 8-bit Ripple Carry Adder (RCA) each addressing different performance requirements. The 8-bit Ripple Carry Adder (RCA) performs addition by connecting a series of full adders, where the carry output of one stage serves as the input carry for the next. This straightforward structure allows the addition process to ripple through the bits sequentially, starting from the least significant bit to the most significant bit.AA ripple carry adder is a basic type of digital circuit used to perform binary addition. It is called "ripple carry" because the carry output from each bit addition "ripples"to the next higher bit.

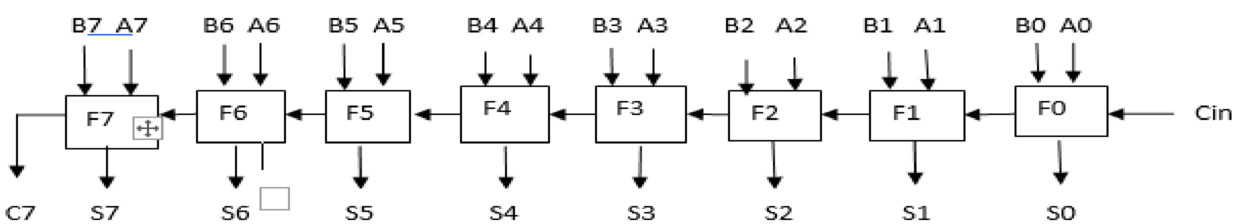

Figure 1. 8-bit Ripplr Carry Adder

An 8-bit Ripple Carry Adder (RCA) is a fundamental digital circuit used for performing binary addition of two 8-bit numbers. It is constructed by cascading eight 1-bit full adders, where the carry output from one stage serves as the carry input to the next stage. Due to its sequential carry propagation, this adder is referred to as a Ripple Carry Adder, as the carry signal "ripples"yhrouhh each stage,impacting the computation speed. The Ripple Carry Adder (RCA) is implemented by connecting a series of full adders in a cascade configuration, where the carry output of each full adder serves as the carry input for the next stage.

II. CMOS SINGLE BIT FULL ADDER

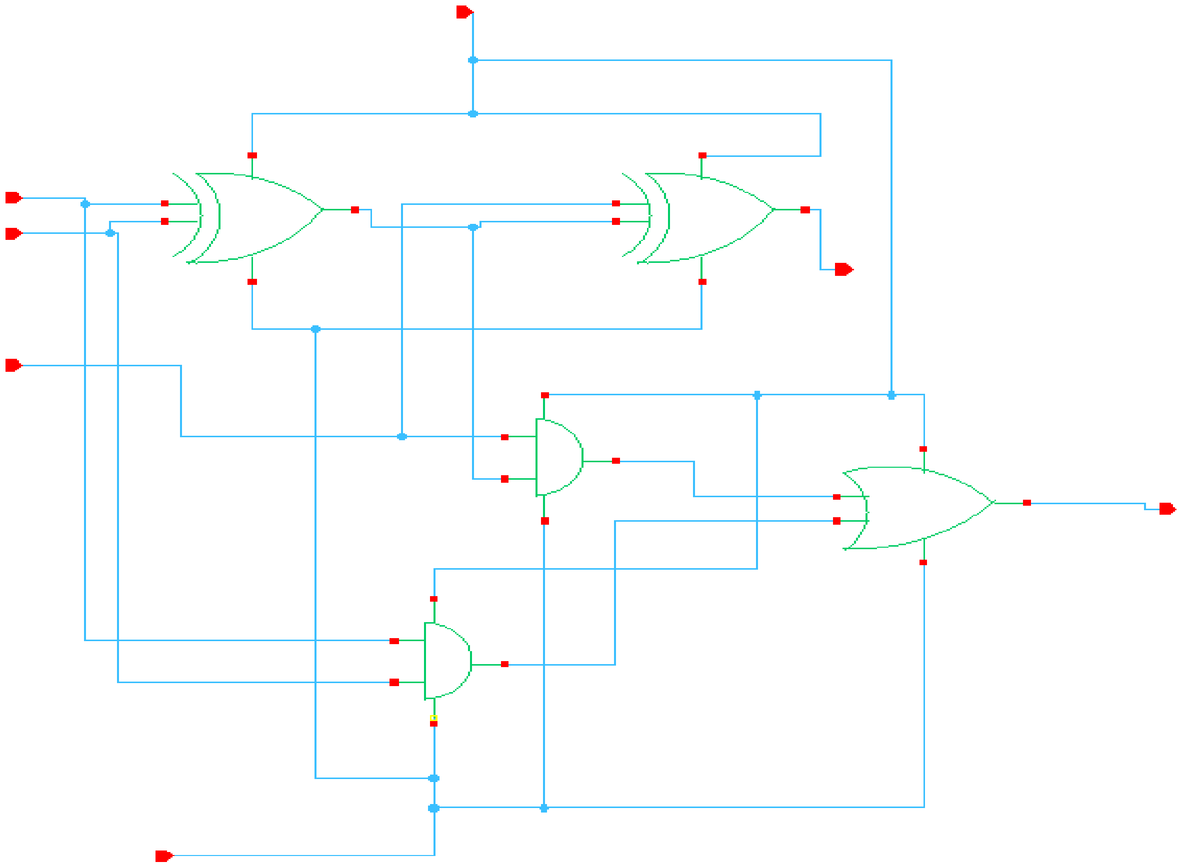

Figure 2. 8-bit Ripplr Carry Adder

A structure of multiple full adders is cascaded in a manner to gives the results of the addition of an n bit binary sequence. Fig 2: schematic of 8-bit ripple carry adder. This adder includes cascaded full adders in its structure so, the carry will be generated at every full adder stage in a ripple-carry adder circuit. These carry output at each full adder stage is forwarded to its next full adder and there applied as a carry input to it. This process continues up to its last full adder stage.

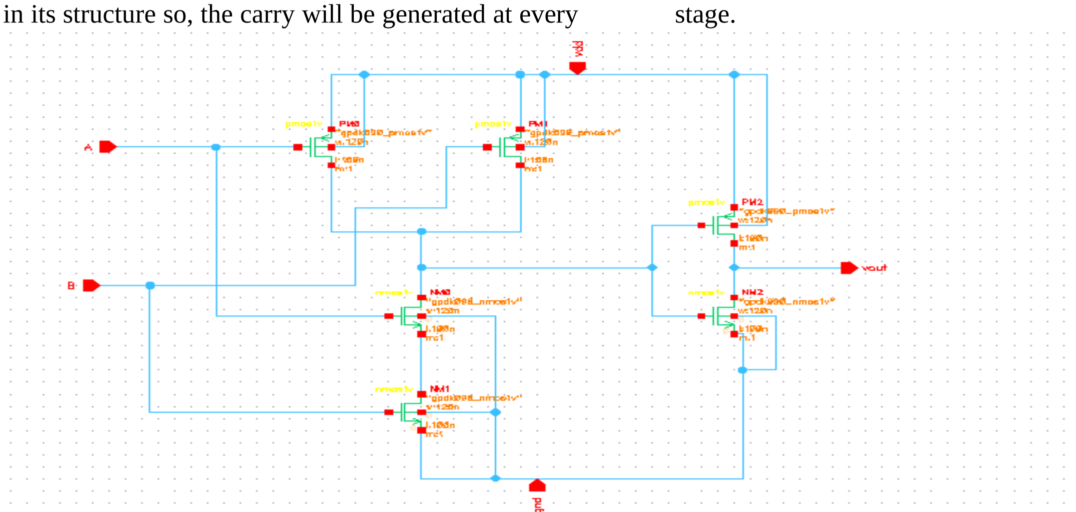

Figure 3. 2-input AND Gate Schematic

Fig 3. 2-input AND Gate Schematic shows the circuit consists of six MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), both PMOS (P-channel MOS) and NMOS (N-channel MOS), arranged to perform the logical AND function.

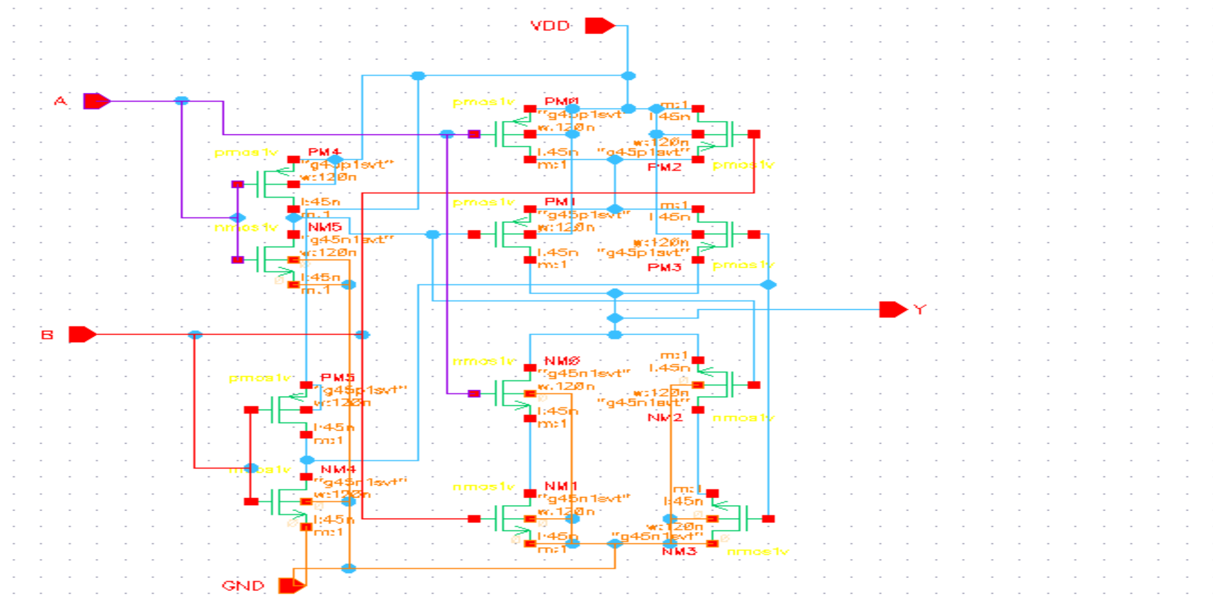

Figure 4. 2-input XOR Gate Schematic

The Fig 4. 2-input XOR Gate Schematic shows design of a digital logic gate, probably a full adder, utilizing CMOS transistors and domino logic with dynamic body biasing for improved performance. It provides a visual representation of the circuit's structure and connectivity, essential for understanding its functionality and implementation.

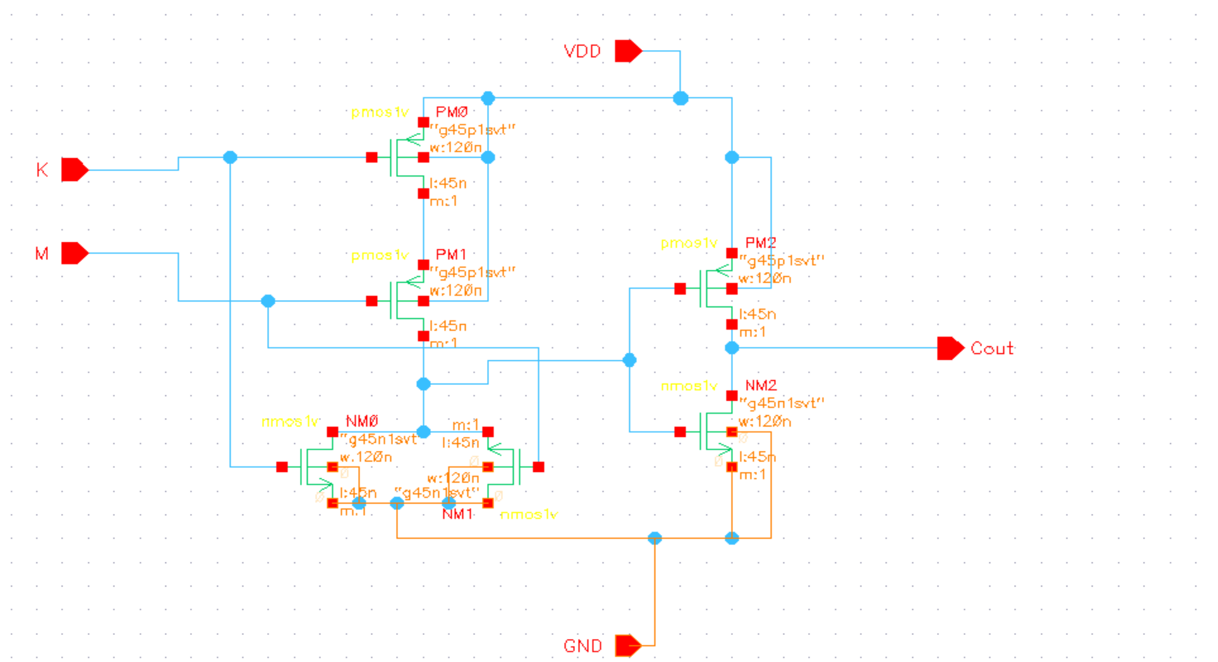

Figure 5. 2-input OR Gate Schematic

The Fig 5. 2-input XOR Gate Schematic shows which uses transistors (both PMOS and NMOS) to manipulate voltage levels. The circuit has inputs K and M, an output Cout, and is powered by VDD and GND. The labels on the transistors (e.g., PM3, NM2) and their associated parameters.

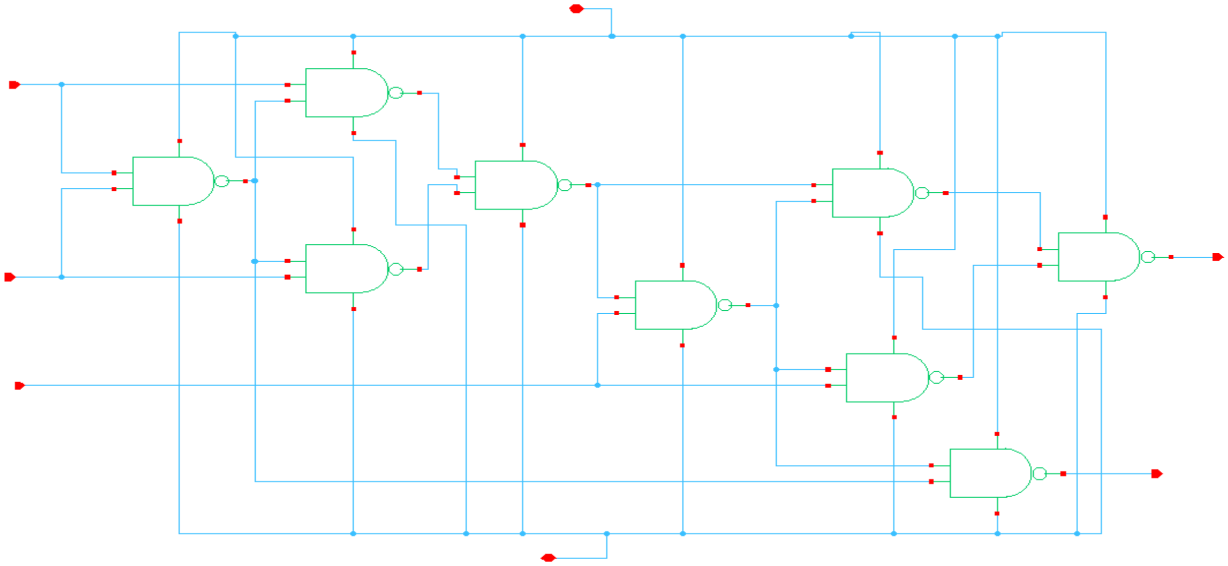

Figure 6. 8-bit Ripplr Carry Adder

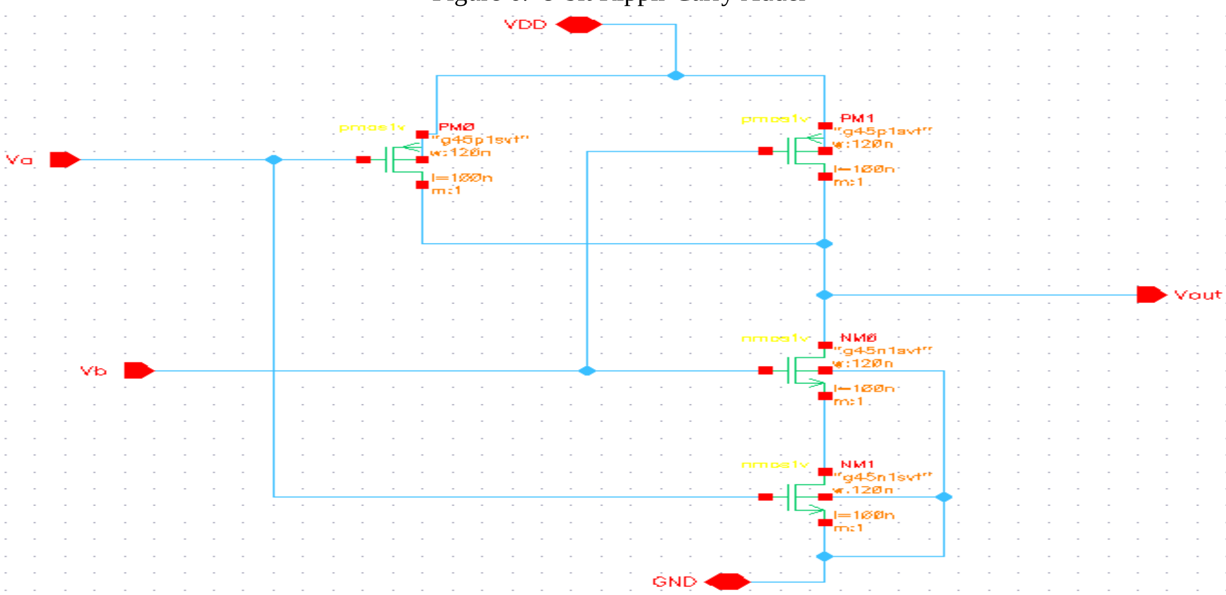

Figure 7. 2-input NAND Gate Schematic

The Fig 7. 2-input NAND Gate Schematic shows NAND gate is a fundamental logic gate that produces a false (0) output only if all its inputs are true (1); otherwise, the output is true (1). The circuit in the image uses four transistors to achieve this function: two PMOS transistors (PM1) and two NMOS transistors.

III. PROBLEM STATEMENT

This project aims to design, implement, and analyze,compare two 8-bit Ripple Carry Adder architectures using 45-nanometer CMOS technology.The implementation of this paper proposed system includes the Delay and Power consumption of Ripple Carry Adder(1) using AND,XOR,OR logic gates and Ripple Carry Adder(2) using only NAND logic gate.This project will involve simulation and analysis to validate the performance metrics of the RCA designs. This analysis will provide valuable insights into the strengths and weaknesses of each adder architecture, enabling informed design decisions for future digital systems.

IV. OBJECTIVES

- To study, design and functionally verify 8-bit Ripple Carry Adder using AND, XOR, OR and NAND logic gates.
- To compare the parameters for designed two Ripple Carry Adders using different logic gates delay and power consumption

V. LITERATURE SURVEY

"Design and Analysis of 8-bit ripple Carry Adder using nine Transistor Full Adder", 'G. R. Padmini, 2O. Rajesh, 3K. Raghu, 4N. Megha Sree, 5C. Apurva, 6K saikumar, DOI: 10.1109/ICACCS51430.2021.9441928. This paper uses a nine-transistor full adder model to design an eight-bit ripple carry adder for less power consumption. The conventional full adder design consists of 28 transistors which constitute high power consumption. Decreasing the transistor count decreases the power consumption in the circuit. A single bit full adder using a nine-transistor is implemented and using this adder, an eight-bit ripple carries adder is designed. A conventional CMOS adder, both single bit and 8-bit ripple carry adder remain also designed to compare the power outputs. Microwind-2.6a and DSCH 2.6 are used to acquire the power outputs of each circuit. To conclude, power comparisons for both single and eight-bit adders using the 9- transistor and conventional CMOS models are made.[1]

"A Compact Design of n-Bit Ripple Carry Adder Circuit using QCA Architecture" Tania Sultana,Rajon Bardhan, Tangina Firoz Bithee, Zinia Tabassum, Nusrat lahan Lisa(2015). In this paper, we propose a new 3-dot based QCA architecture. We also present wiring logics, basic gates and XOR gate using proposed QCA 3-dot cell. All these components are very much efficient to compute basic operations. Moreover, we design a QCA 3-dot based half adder and extend the half adder into a full adder which has least number of QCA cells till now. We also design a powerful and efficient n-bit ripple carry adder applying our new and novel scheme. Our proposed circuits perform much better than the existing ones, e.g., the proposed32-bit ripple carry adder circuit improves 21 % on a mathematical model for probabilistic ripple-carry adders. The model gives explicit expressions for calculating error probabilities of sum and carry bits. The expressions show how errors propagate through the carry, which accumulate and eventually influence the correctness of a ripple-carry adder's outputs.The proposed model is flexible since it only requires mild assumptions on the probability distribution of noise. Hence, in addition to Gaussian,it is applicable to a wide class of distributions. We validate the model through HSPICE simulation. The model is able to predict error-rates of a simulated probabilistic ripple-carry adder with reasonable accuracy. [2]

"An Adiabatic Quantum-Flux-Parametron 8-bit Ripple Carry Adder Using Delay-Line Clocking TaikiYamae"; Naoki Takeuchi; Nao; DOI:10.1109/TASC.2003.3239822. This paper demonstrated several AQFP logic gates with delay-line clocking and demonstrated a phase skipping operation, in which some of the AQFP buffers for phase synchronization are removed to reduce the junction count and energy dissipation. In the present study, we design and demonstrate an AQFP 8-bit ripple carry adder with delay-line clocking to show that delay-line clocking and the phase skipping operation are applicable to large-scale AQFP circuits. The latency of this adder is 960 ps, which is 40% of that for a conventional design. Moreover, due to the phase skipping operation, the junction count is reduced to approximately 70% of that for the conventional design. We find that this adder can operate at up to 4 GHz. The above results indicate that large-scale AQFP circuits can operate with low latency and low junction count by using delay-line clocking and a phase skipping operation.[3]

"Modeling of Probabilistic Ripple-Carry Adder Mark" S. K. Lau, Keck Voon Ling, Yun Chung Chu, and Arun Bhanu (2010). This paper proposes a mathematical model for proba bilistic ripple-carry adders. The model gives explicit expressions for calculating error probabilities of sum and carry bits. The expressions show how errors propagate through the carry, which accumulate and eventually influence the correctness of a ripple-carry adder's outputs. The proposed model is flexible since it only requires mild assumptions on the probability distribution of noise. Hence, in addition to Gaussian, it is applicable to a wide class of distributions. We validate the model through HSPICE simulation. The model is able to predict error-rates of a simulated probabilistic ripple-carry adder with reasonable accuracy. This paper proposes roposed equa tions that iteratively compute error probabilities for the sum and carry bits of a PRCA. We note that sometimes iterative equations may be less helpful than explicit expressions. [4]

VI. PROPOSED METHODOLOGY

The methodology followed in project is as follows:

1. The schematics of basic gates like Inverter, and gate, Xor gate and or gate are designed in the Virtuoso Schematic Editor.
2. The complex circuits like Ripple carry adder (RCA) designed in the Virtuoso Schematic Editor using these smaller gates.
3. Simulated the circuit to ensure that it functions as expected. Cadence tools allow for both functional and timing simulations.
4. The delay, average power consumption, transistor counts are calculated for different circuits.

VII. RESULT AND WORKING MODEL

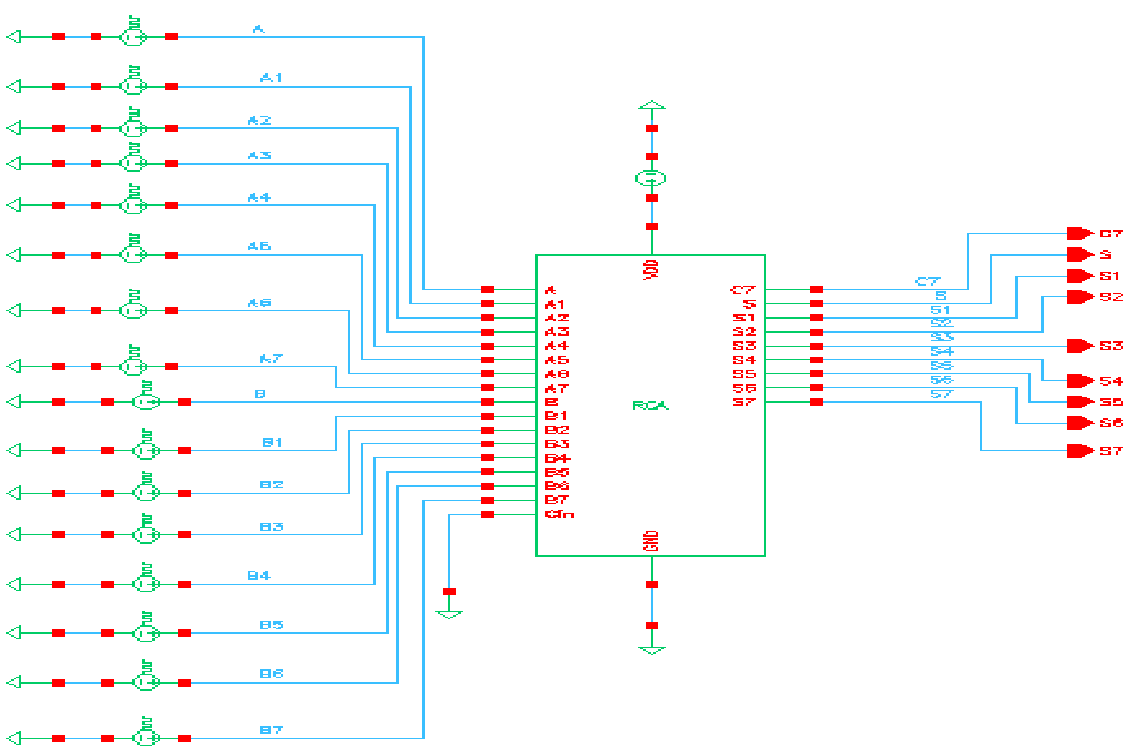

Fig 8. 8-bit Ripplr Carry Adder

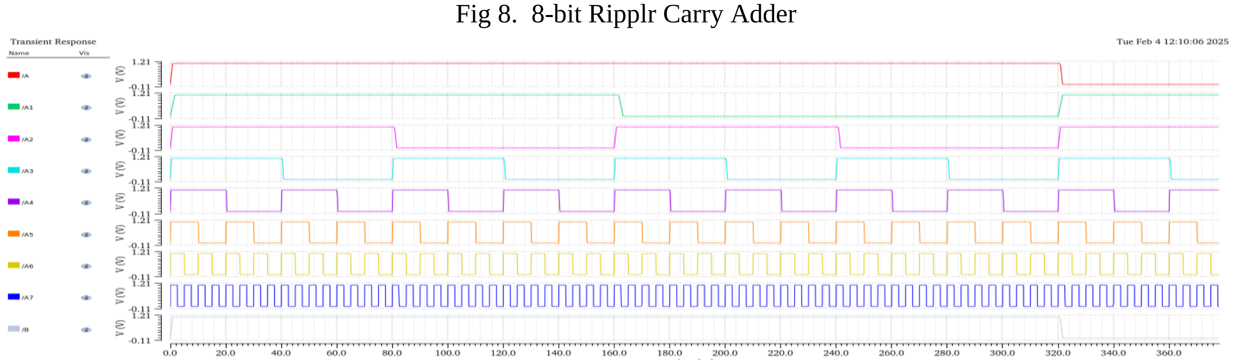

Fig. 9 (1) 8-bit Ripple Carry Adder inputs A0 to A7 waveform

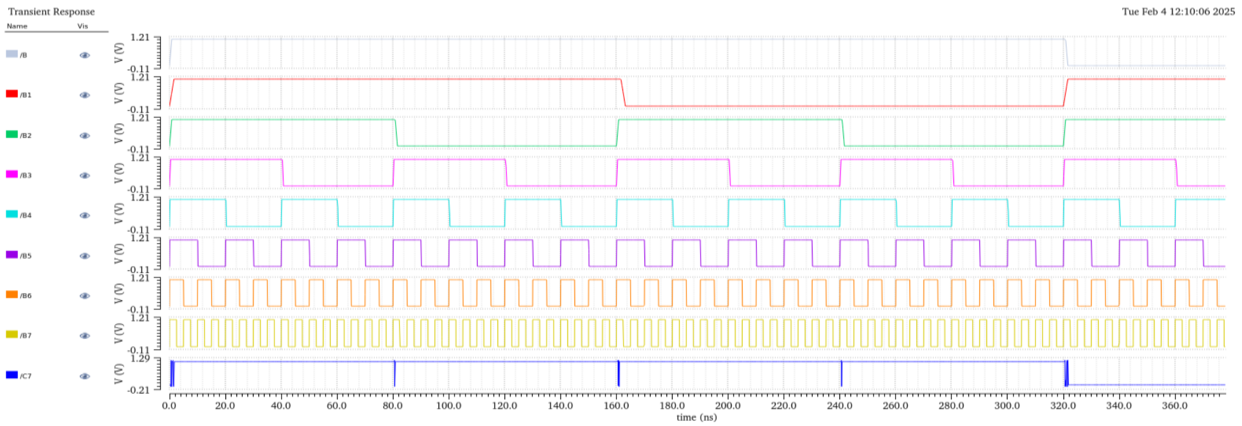

Fig. 10 (1) 8-bit Ripple Carry Adder inputs B0 to B7 waveform

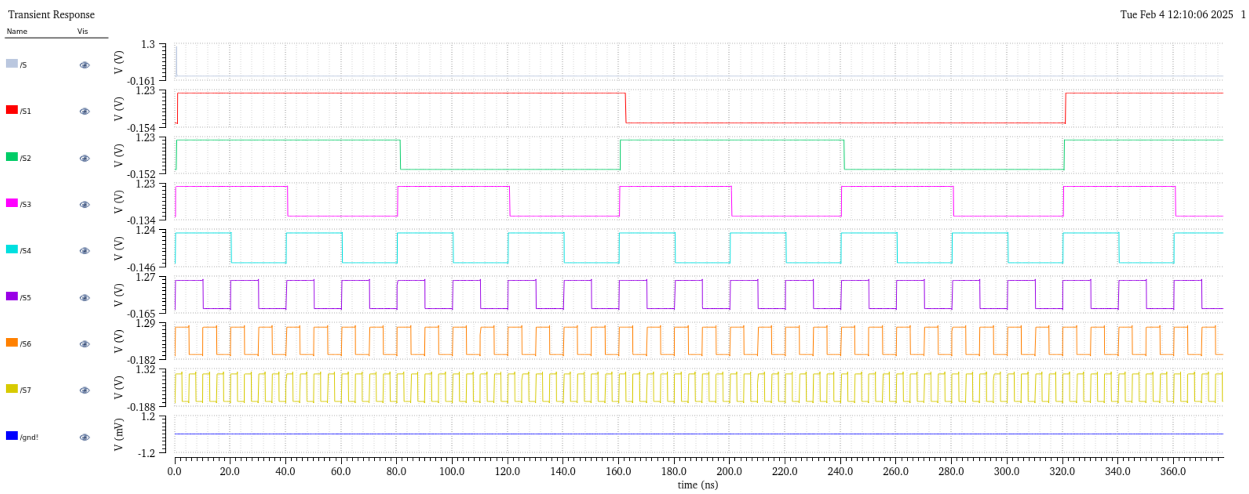

Fig. 11 (1) 8-bit Ripple Carry Adder inputs S0 to S7 waveform

Fig 8. indicates the 8-bit RCA testing which selects the all inputs A0 to A7 and B0 to B7 and
outputs sum and carry of the 8-bit RCA.Fig 9 shows the 8-bit Ripple Carry Adder inputs A0 to A7 waveform, Fig 10. 8-bit Ripple Carry adder inputs B0 to B7 waveform, Fig 10.8-bit Ripple Carry Adder outputs S0 to S7 waveform.

VIII. RESULT AND ANALYSIS

Parameter	RCA 1	RCA 2
No of Transistor	336	288
Power	1.421ns	1.699ns
Delay	302nsec	130ns

IX. CONCLUSION

The comparison between the Ripple Carry Adder-1 (RCA) using 2 xor gates,2 and gates and 1 or gate and Ripple Carry Adder-2 (RCA) using nand gates highlights the trade-offs between simplicity and performance in digital arithmetic circuits. The RCA, with its straightforward design and minimal hardware requirements, is a good choice for applications where speed is not a critical factor. However, its sequential carry propagation results in significant delays, particularly for larger word sizes, making it less suitable for high- performance systems.

On the other hand, the RCA excels in scenarios requiring high-speed computation due to its ability to perform additions using 45nm and reduce carry propagation delays. By saving carry bits for later processing, the RCA effectively minimizes the dependency on previous stages, achieving faster computationusing 45nm.

In conclusion, while the RCA is preferable for simpler,and comparision between RCA1 using 2 xor,2and,1or gates and RCA2 using 9 nand logic gates which shows the comparision delay and average power consumption.The choice between these architectures ultimately depends on the specific design requirements and the trade-offs between speed, area, and power consumption.

REFERENCES

[1] "Design and Analysis of 8-bit ripple Carry Adder using nine Transistor Full Adder", 'G. R. Padmini, 2O. Rajesh, 3K. Raghu, 4N. Megha Sree, 5C. Apurva, 6K saikumar, DOI: 10.1109/ICACCS51430.2021.9441928.

[2] "A Compact Design of n-Bit Ripple Carry Adder Circuit using QCA Architecture" Tania Sultana,Rajon Bardhan, Tangina Firoz Bithee, Zinia Tabassum, Nusrat lahan Lisa(2015).

[3] "An Adiabatic Quantum-Flux-Parametron 8-bit Ripple Carry Adder Using Delay-Line Clocking TaikiYamae"; Naoki Takeuchi; Nao; DOI:10.1109/TASC.2003.3239822.

[4] "Modeling of Probabilistic Ripple-Carry Adder Mark" S. K. Lau, Keck Voon Ling, Yun Chung Chu, and Arun Bhanu (2010).