Energy-Efficient Contention-Free 25-Transistor Single-Phase Clocked Flip-Flop in 90nm CMOS

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***Abstract*—To significantly enhance energy efficiency in sequential digital circuits, this project will develop an ultralow power true single-phase clocked (TSPC) flip-flop using a novel 25-transistor design, expandable to 29 transistors with a reset function. By eliminating redundant charge and discharge cycles, the flip-flop will drastically reduce power consumption. Transistor-level optimization will be utilized to address floating nodes, ensuring a fully static and contention-free operation within 55 nm CMOS technology. This innovative flip-flop design will be a crucial component in various digital systems, particularly in applications where minimizing power consumption is essential, such as battery-operated devices, IoT systems, and wearable technology. Additionally, it will cater to the growing demand for energy-efficient components in large-scale digital infrastructures like data centers and mobile computing platforms, where optimizing power usage is vital for enhancing overall system performance and sustainability.**

***Index Terms*—Ultra-low power, Static, Flip-flop, 45 nm technology.**

1. INTRODUCTION

The rapid expansion of the Internet of Things (IoT) and advancements in processor technology have significantly improved the performance of digital systems. However, as technology evolves, power consumption has become a critical challenge, especially in energy-sensitive applications such as mobile devices, embedded systems, and IoT-based networks. FFs (flip-flops) are fundamental components in sequential logic circuits, playing a key role in data storage, synchronization, and transfer within digital systems. These circuits operate based on clock pulses, which regulate the timing of data processing. However, traditional FF designs suffer from high power consumption due to the two-phase clocking mechanism, where clock inverters continuously toggle states during every clock cycle. This excessive switching activity leads to increased energy loss and reduced system efficiency.

Among various FF types, the D (Data) FF is widely used due to its simplicity and reliability. It features a single input (D) and two outputs (Q and $\bar{Q}$), where the data at the D input is transferred to the Q output on the activation of the clock signal. Since FFs are used extensively in memory elements, registers, and counters, optimizing their power efficiency is essential to enhance overall digital system performance. Recent advancements in low-power FF designs, such as single-phase clocking techniques and transmission gate-based FFs, have significantly reduced energy consumption. These innovationshelp minimize clock distribution power loss, making them highly suitable for modern low-power application.

The demand for energy-efficient digital systems has driven extensive research into optimizing FF design. Techniques such as clock gating, conditional capturing, and pulse-triggered FFs have been introduced to reduce dynamic power consumption and enhance circuit efficiency. Low-power FF designs are particularly beneficial for portable electronic devices, where battery life is a major concern. By improving FF power efficiency, digital circuits can operate more effectively while maintaining high-speed performance. As the need for low-power and high-performance computing grows, optimizing FF architectures will continue to play a vital role in the evolution of modern digital technology.

1.1. Research Objectives

The paper presents a novel flip-flop design by G. Shin that addresses power consumption in digital systems. By eliminating redundant clock transitions and optimizing transistor usage, the design reduces

dynamic power loss and unnecessary transistors. This fully-static, contention-free flip-flop ensures stable operation and is ideal for low-voltage, low-frequency applications, such as IoT devices and energy-efficient processors.

Y. Lee proposed the traditional Single-Edge-Triggered flip-flops, the DET-FF latches data on both clock edges, offering better energy efficiency. The authors introduce a fully static True-Single-Phase-Clocked (TSPC) DET-FF, which overcomes clock overlap issues, ensuring reliable, low-power operation at near-threshold voltages. Implemented in 28nm CMOS, the design is validated through simulations, achieving efficient operation at 0.28V across a wide temperature range while optimizing energy consumption.

H. You addressing power consumption by eliminating redundant pre-charge operations, which are common in traditional TSPC designs. The flip-flop incorporates a retentive mechanism to ensure data retention with minimal power loss, improving energy efficiency. This design reduces dynamic power consumption while maintaining stable performance under low-voltage conditions, making it ideal for low-power digital applications, such as portable electronics and IoT devices.

C.K proposed. the innovative adaptive-coupling configuration reduces redundant transitions and optimizes transistor activity, leading to a 77% energy reduction compared to traditional flip-flops. Implemented in 40 nm CMOS technology, the flip-flop offers high energy efficiency while maintaining reliable performance, making it ideal for low-power, high-performance digital system.

Despite the reduction in transistors, both circuits maintain reliable high-frequency operation. The static version is particularly effective in preventing metastability issues, while the dynamic version is designed to handle race conditions effectively. Additionally, the new designs offer a simplified layout that improves practicality and reduces complexity, making them a more cost-effective solution for VLSI systems. These advancements open up new possibilities for the use of DET-FFs in a wider range of applications, making them more attractive for both practical and economic considerations in digital circuit design.

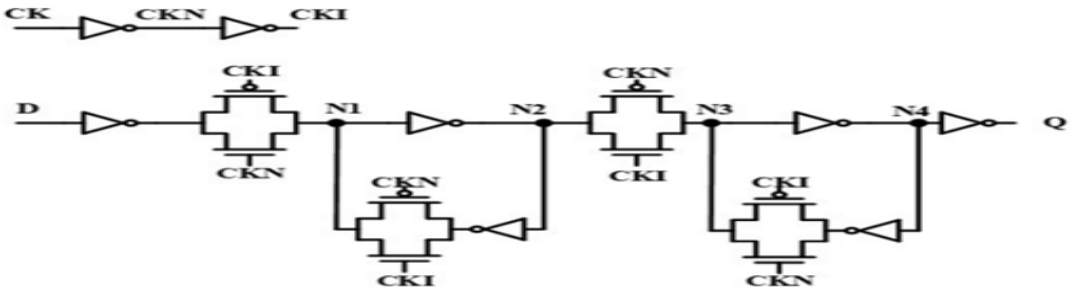
2. EXISTING METHOD

In contemporary digital systems, one of widely used flip-flops is the TGFF. Figure depicts the schematic for it. 1. The TGFF operates without contention and at voltages close to threshold. However, the extensive clock network is its primary drawback. The internal nodes CKI and CKN toggle continuously, with each signal driving four load transistors, leading to significant power consumption.

The need to conserve power while maintaining functionality has driven the evolution of flip-flop designs for low-power circuits. The HFF design, which uses 18 transistors, requires precise transistor width ratios and employs high W/L ratio NMOS transistors for the transmission gate. Because the design is unable to function effectively under low supply voltages, this configuration results in area overhead and low-voltage dysfunction.

Similar to the S2CFF, the SPC-18T FF, a low-power flip-flop, has problems, particularly the redundant toggling at the internal data node when the data remains at "0," which wastes power.

Schematic Of TGFF



Additionally, when the input data undergoes rapid transitions from "1" to "0," the SPC-18T flip-flop (FF)

significant hold time issue. This malfunction prevents the master latch from fully discharging, leading to potential functional failures in critical system operations. Such failures can be detrimental in high-speed circuits where timing accuracy is paramount.

To mitigate these issues, the Redundancy-Eliminated Flip-Flop (REFF) introduces a novel approach by simplifying the inverter phase of the clock signal and generating a new clock signal, CLKB. This modified clock signal aims to enhance the stability and reliability of the flip-flop operation, reducing the likelihood of hold-time violations. However, while REFF resolves some of these concerns, it comes at the cost of increased power consumption and area overhead due to the integration of additional control logic.

One of the primary drawbacks of REFF is the introduction of redundant transitions, which significantly impact power efficiency. Each unnecessary signal transition results in excess energy dissipation, increasing the overall power footprint of the system. In high-performance computing and energy-sensitive applications, such inefficiencies can severely degrade system performance and limit battery life in portable devices. The presence of redundant transitions not only escalates dynamic power consumption but also contributes to unwanted thermal effects,

potentially affecting long-term reliability.

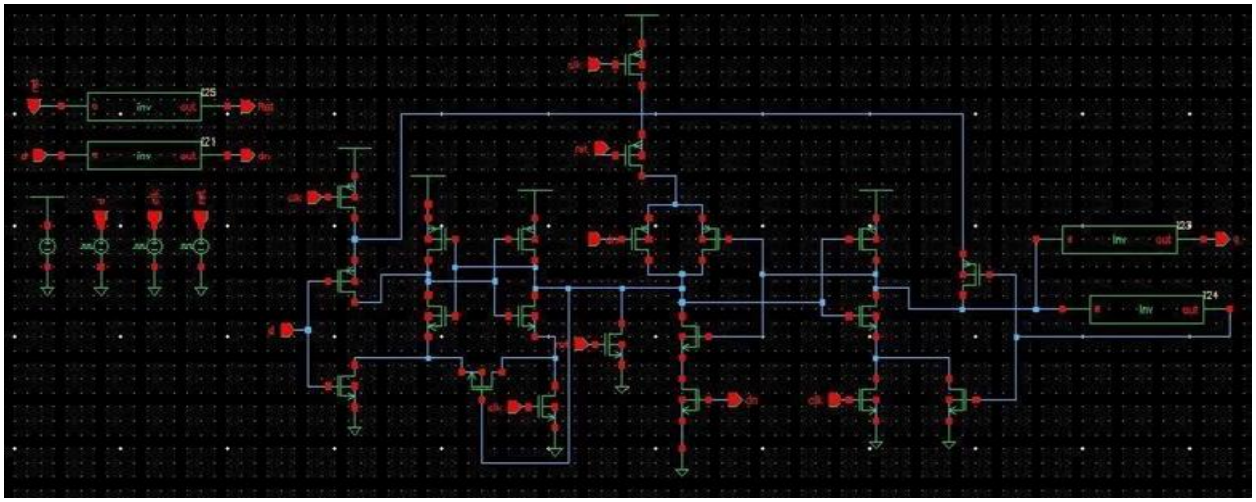


Fig:SchematicforFFwithasynchronous reset

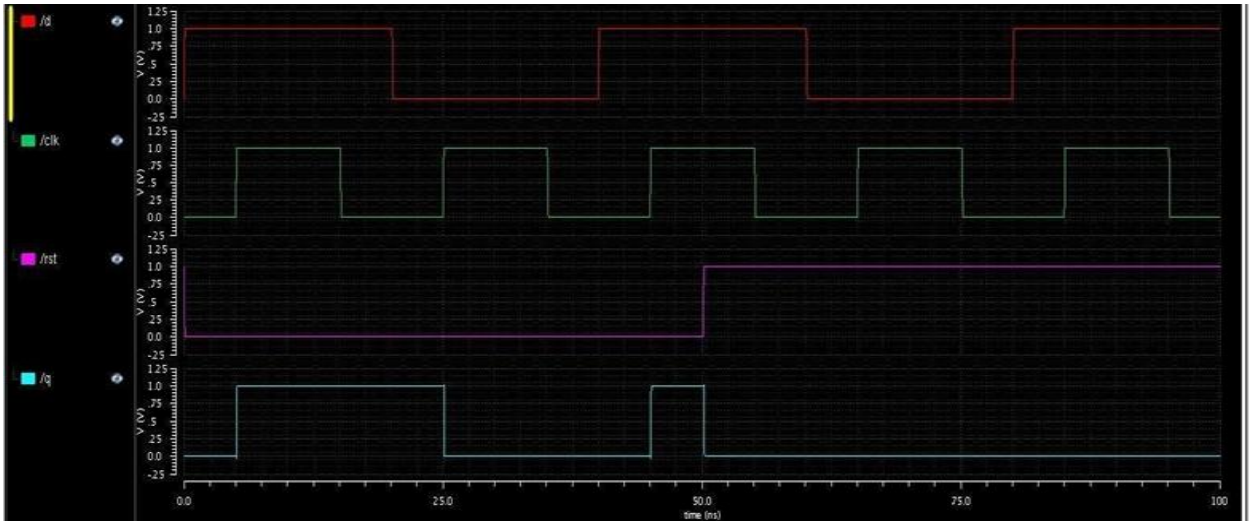
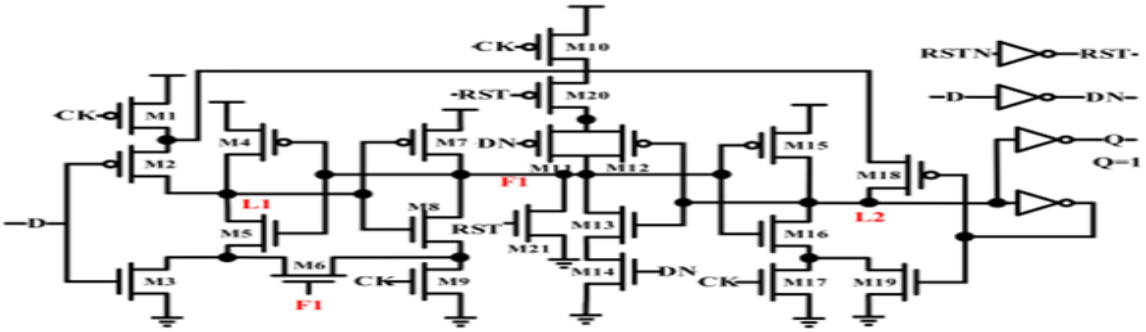


Fig:Waveforms forFFwithasynchronous reset

3. PROPOSED METHOD

The proposed flip-flop (FF)'s structure is described in detail in this section. As the circuit is composed of 25 transistors. It is important to note that in standard cell libraries, the clock signal of the FF typically includes a clock buffer. This clock buffer is used to balance the clock tree and enhance the clock driving capability of the internal FF circuit. However, because it is a common component and has no effect on the FF's functionality or the comparisons that follow, the clock buffer is not included in this discussion. The input data are moved to node L1 or node F1 during the clock's negative phase, but the slave latch's output data are unaffected. . In the recharge path of node F1, an M11 PMOS transistor is inserted as the input sense transistor. It is controlled by the inversion of the input data to prevent charging of node F1 when the input data is '0' during the negative phase of the clock. Without transistor M11, node F1 would be charged to VDD during the negative clock phase and then discharged to GND at the rising edge of the clock, causing unnecessary power consumption. However, when the input data is '1', M11 turns ON, allowing node F1 to be charged to VDD during the negative phase of the clock through the transistors M10 and M11. When the input data is "0," this design aids in eliminating redundant power dissipation.



Schematic Of Proposed Method

Whenever the clock is low and the output data Q is "1," the output data cannot be latched since the insertion of M11 because there is no charge path to node F1.. Because of this, M10 and M12 maintain a charge path to node F1, allowing M16 to remain ON and establishing a loop that correctly latches the output data. Potential internal floating nodes, which could otherwise alter the correct value due to leakage current, are effectively eliminated by the proposed design. The internal nodes always maintain a charge path to VDD or a discharge path to GND when transistors M6, M11, M12, M13, and M14 are inserted, as shown by the colored lines in Fig. 2(a). This is the case regardless of the clock, input data, or output Q states. Consequently, the proposed flip-flop achieves a fully static design and can operate correctly across all frequency ranges while consuming very low power.

When the clock (CK) is low and the input data (D) is 0, node L1 is charged to VDD through transistors M1 and M2, and transistor M8 is turned ON. At the rising edge of CK, node F1 is discharged to GND via M8 and M9. Afterward, transistor M15 is turned ON to charge node L2 to VDD, and then the output Q changes to 0 through the inverter.

The signal DN becomes 0 when CK is low and the input data (D) is 1. Node F1 is charged to VDD through transistors M10 and M11. The voltage at node F1 keeps transistors M5 and M16 ON simultaneously. With the involvement of M5 and M3, node L1 is pulled down to ground. When CK transitions to a high state, M16 and M17 facilitate the discharge of node L2 to ground, leading to the output switching to '1' via the inverter.

To ensure that there is no voltage transfer threshold voltage drop, the charge and discharge paths that each internalnode consists solely of either NMOS or PMOS transistors. This structure ensures a full-range voltage swing, enabling the flip-flop to operate reliably even at near-threshold voltage levels.

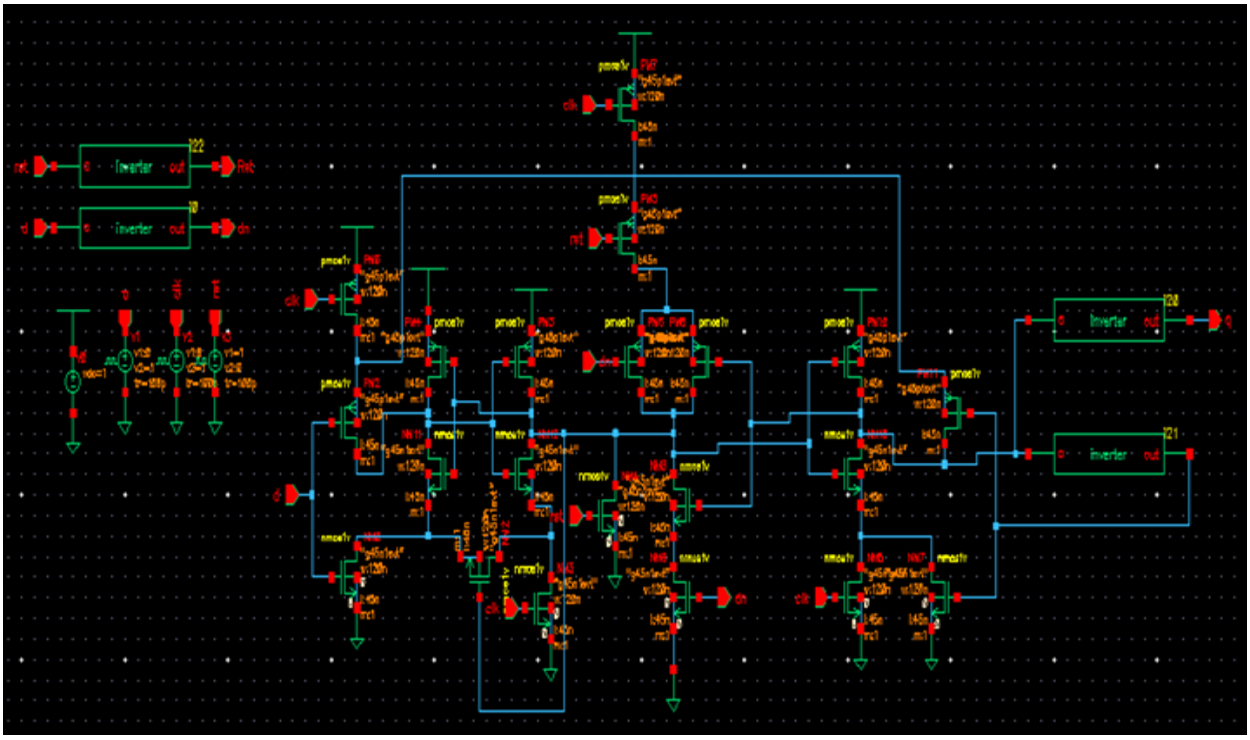


Fig:Schematic of proposed TSPC FF with asynchronous reset.

The transient response of the designed flip-flop at a supply voltage of 0.6 V demonstrates its functionality. As observed in the figure,the internal nodes L1, F1, and L2 remain stable when the input data is constant, confirming the stability of the design at low supply voltages.

Waveforms for proposed FF with asynchronous reset

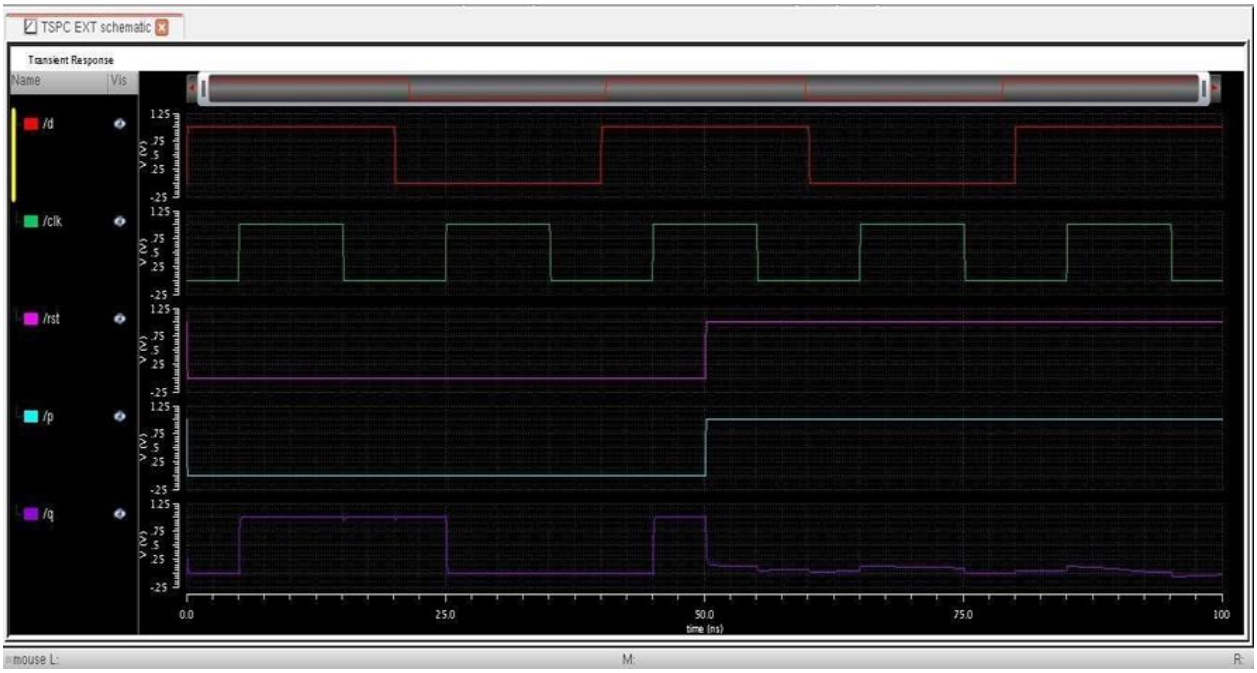


Fig: Waveforms of proposed flipflop

4. REFERENCE CIRCUITS

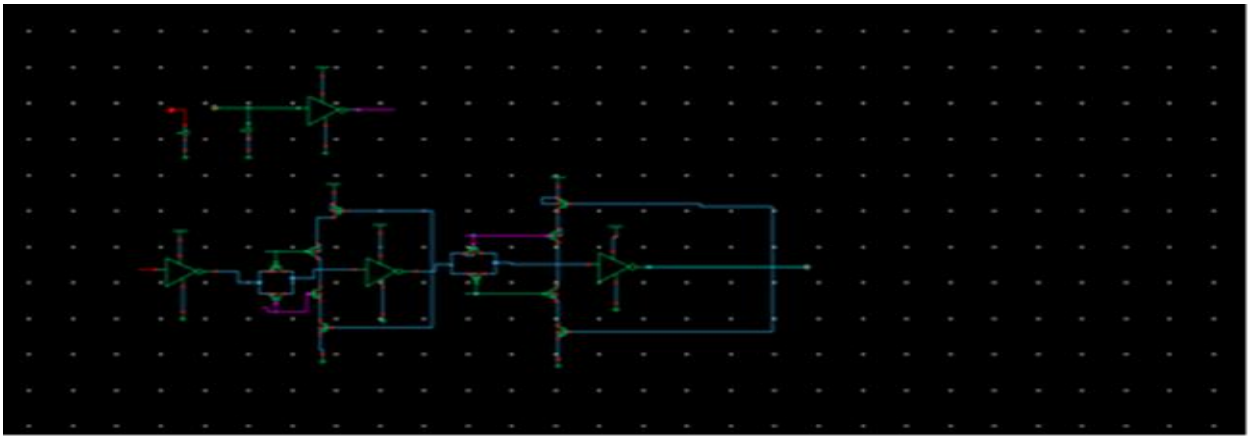
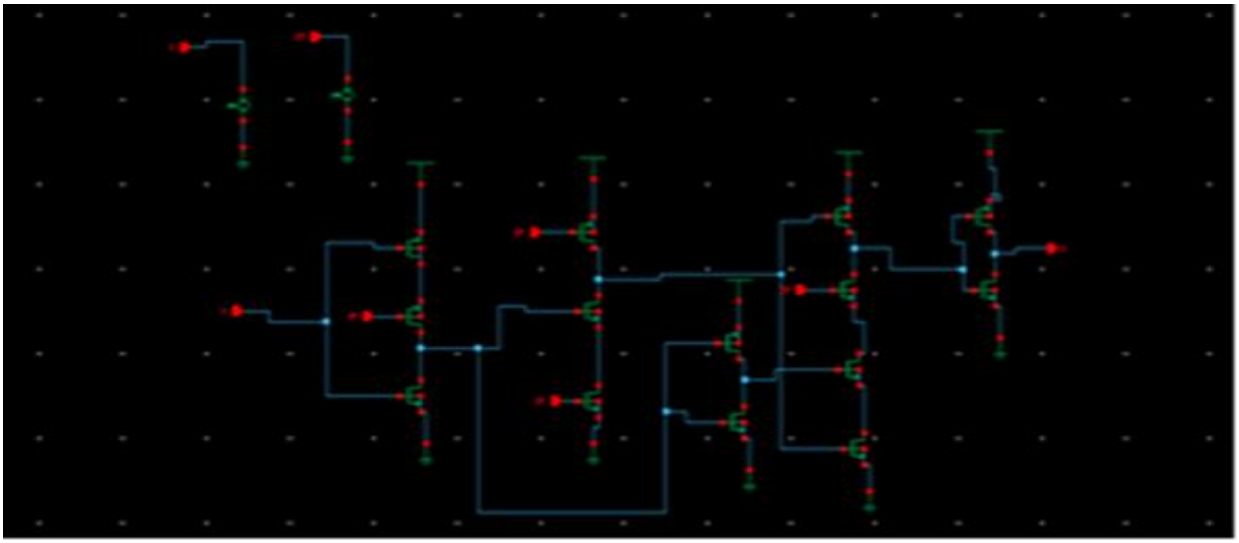


Fig: Transmission GateMaster-Slave

Waveforms Of TG Master Slave FF



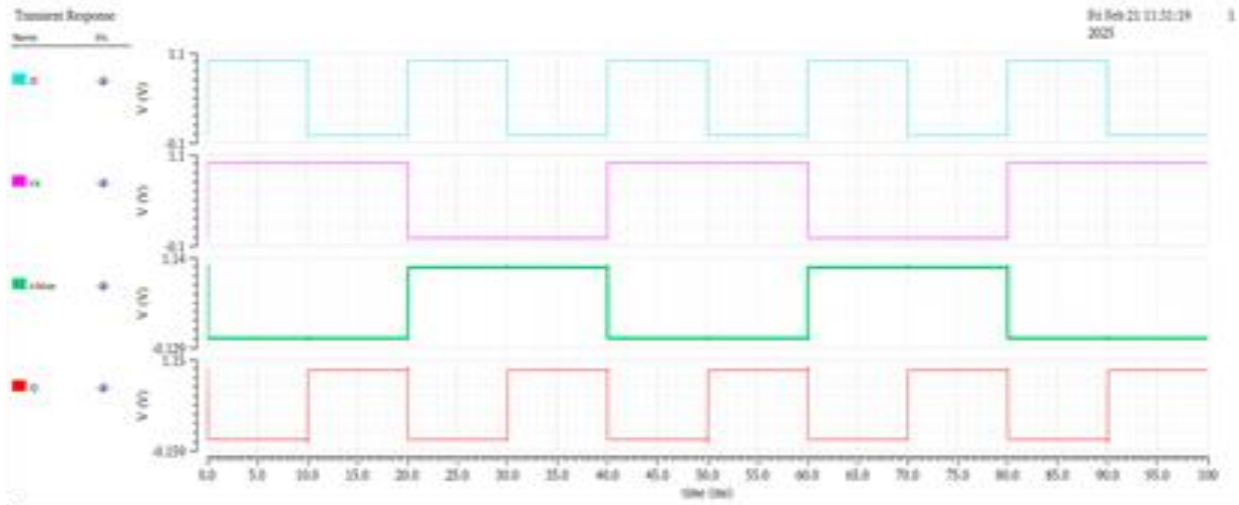
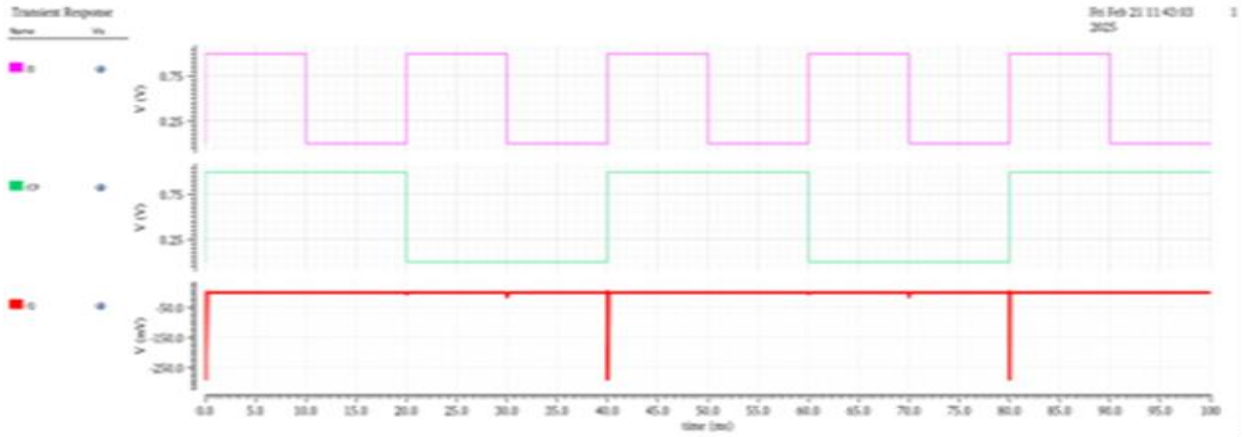


Fig:High Speed Tspc Architecture



Waveforms Of High Speed Tspc FF

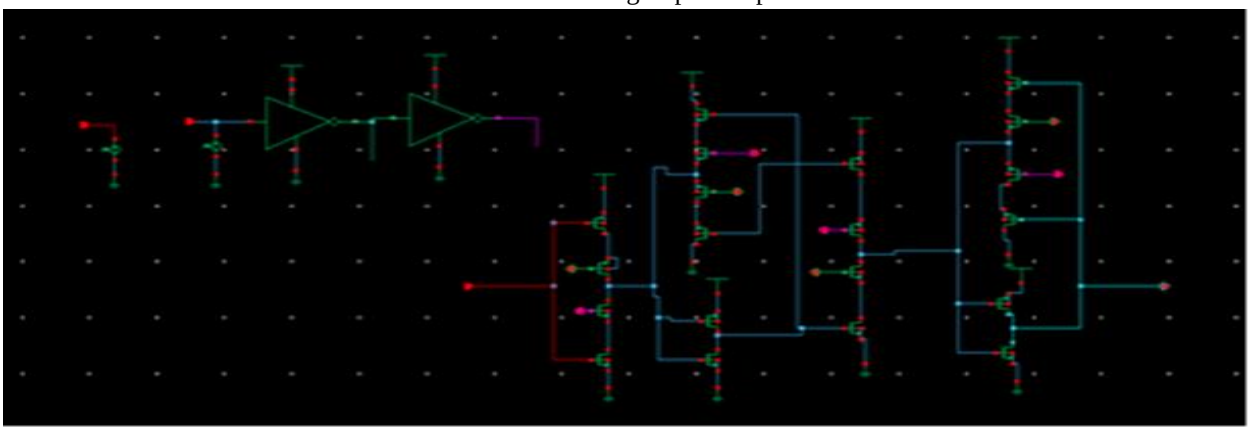
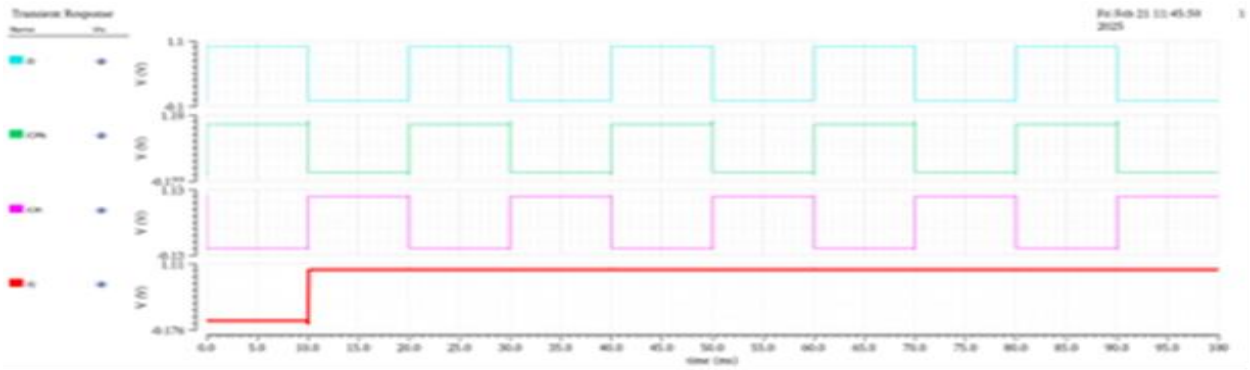


Fig:C^{2}mos Master -Slave Flipflop



Waveforms Of C^{2}mos M -Slave Flipflop

6.COMPARISON TABLE

DESIGN	EXISTED	PROPOSED
AREA	29	26
POWER(ns)	309.9	182.8
DELAY(ns)	5.052	5.065

7.CONCLUSION

A highly energy-efficient, fully stable, conflict-free, genuine single-clocked flip-flop utilizing 25 transistors (29 of which have an asynchronous reset function) is designed for use in digital circuits with low voltage and low frequency. By not requiring

internal nodes to be precharged, this flip-flop uses significantly less power across a variety of supply voltages because it only has four clock loads. In terms of power efficiency, the design outperforms existing flip-flop configurations.The measurement results demonstrate that the proposed flip-flop operates as intended when it is implemented in 45 nm CMOS technology.

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