Analog Layout Design of ADC, DAC & Physical Verification

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***Abstract*— Analog Layout Design is a part of physical design in Analog design flow. In the fabrication process to perform lithography step masks are required to im- plant the desired pattern on the wafer and these masks are nothing but the layouts designed on layout editor. Normally after the circuits are designed and the outputs are verified after simulations, layouts have to be drawn for these circuits so that they can be fabricated. Layouts are nothing but geometrical representation of circuits using different layers and polygons. Layout design is a four-step process i.e. floor plan, placement, routing, and verification. Floor plan is an area estimate, placement is fixing the positions of devices or blocks, routing is the connections between devices or blocks and verification is done by DRC, LVS check. DRC checks whether the layouts designed are according to design rules provided by fabrication companies or not and LVS checks for connectivity, device properties, stamping conflicts, open or short circuits etc. Electro Migration checks whether the specified current is flowing through particular net or not and parasitic extraction is to make sure that the metal parasites are not degrading the circuit performance. Analog Layout design is complex job as there is no perfect automation and also analog circuits are so sensitive to temporal variations. The present work gives a clear idea about the Analog Layout Design and also the issues involved in Analog Layout Design.**

***Index Terms*: DRC, LVS**

I. INTRODUCTION

In the present-day design of extremely complex systems on chip (SoC) featuring multimillion transistor ICs including both digital and analog sections, the level of integration is increasing day to day. Usually, IC designs are divided into two categories depending on the type of circuits or systems handled by the IC. Non-Mixed IC design [1] is one in which it contains purely either analog de- sign or purely digital design but not consists both of them on a single die where as in Mixed IC design [1] it contains both analog and digital designs on a single semiconductor dies. When compared to the Non-mixed IC design the growth rate of mixed IC design is increasing from day to day. The growth rate of IC design is shown in Figure 1.

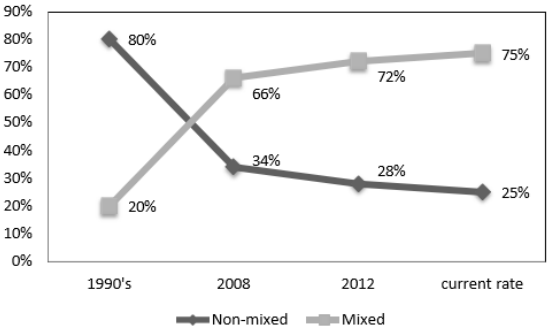

Figure1.1Growth rate of IC design.

In the mixed IC design if the ratio of analog design is compared with the digital design it is like almost 80% is digital and 20% is analog. Though the analog part is typically a small fraction of the whole IC, it introduces a bottleneck in terms of design time due to its complex nature. With the increase in the growth rate of Mixed IC design analog design has gained its own importance because de- sign time required is almost 80% of the total time and passes for success is like trial and error and can be achieved in two to three passes. Apart from these standard cells can be created for digital cells like inverters, buffers, logic gates, and filler cells; tie cells etc. but cannot be created for analog cells and also the specifications for analog designs changes from technology to technology. all the above-mentioned factors analog design has its own importance in IC design.

Layout Design is a part of second step of design flow. After a circuit is designed and its functioning is verified with simulations, layout of the circuit has to be designed. Layout is nothing but geometrical representation of circuit by means of layers and polygons. Layout design is a four steps process Floor plan, Placement, Routing and verification.

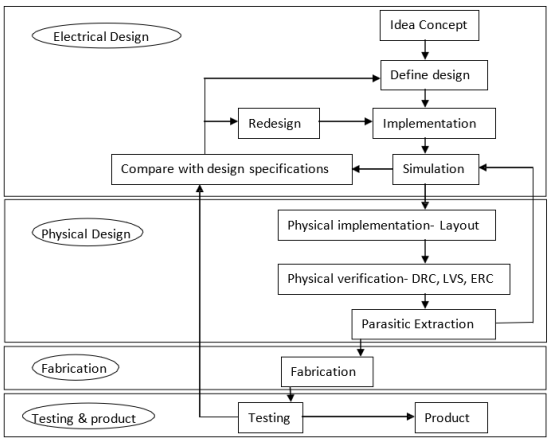

Figure1.2 Flowchart of Analog Design Flow

II. LITERATURE SURVEY

Studies of IC design in the domain of analog designs have shown the lay- out importance in different phases of the circuit like electrical sizing, power consumption, parasitic effects etc. [3], [4]. Although there are different approaches to meet the specifications of the analog circuit designs each of them differs from other as the parasitic resulting from the layouts is not same all the time. The existing device generators are fast in layout flow [5]-[7] but the drawback is the information regarding parasitic are not given by them but to be calculated manually while drawing them and also it can be as accurate as the layout-inclusive [8] flow. Layout generation in analog circuit design still remains a critical bottleneck as this is a manual work. Layout design is a part of physical design in the analog design flow (Refer Figure 1.2) process and this physical design takes care of following factors [9]:

- Minimize the noise coupling on critical signals.
- Matching of differential signal routes and the circuits that are sensitive to process mismatch.
- Minimizing well proximity effects.
- Widening of power rails to enhance current handling capabilities and to minimize voltage drop.

III. LAYOUT DESIGN STEPS &VERIFICATION

Layout in general is geometrical representation of the circuits by means of layers and polygons. As mentioned in Chapter-1 analog layout design is comprised of 4 steps as follows:

i. Floor planning
ii. Placement
iii. Routing and
iv. Verification.

Floor planning is nothing but an area estimate of the circuit. It helps us to create areas of functionality on the entire chip area, determine the connectivity, I/O pad placements and tells us how the routing would be. In this step we plan the position of power rails, position of different blocks depending on connectivity between them, ground connections etc. In general, tentative floor plan for any layout design is as shown in Figure 3.1.

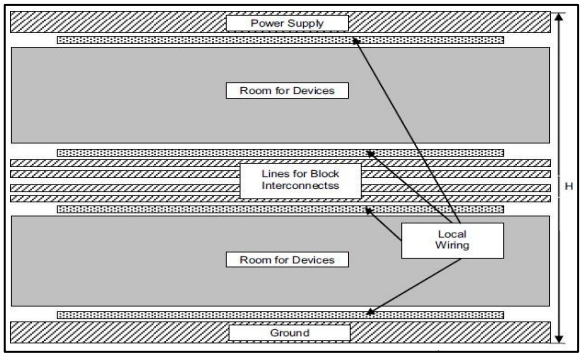

Figure3.1. Tentative floorplan for layout design

Placement is After finishing floor plan placement is the next step. In this step we will nail down the exact positions of all the blocks if it is in top level, all the devices if it is in the block level. While doing placement make sure that enough room space is available for routing and routing becomes easy. Different techniques of placement which are in existence are symmetrical placement, matrix method of placement for multi group of identical devices.

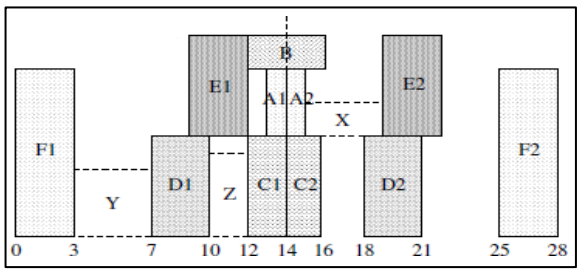

Figure3.2 Fixing the width and height while Placement

Routing After nailing the exact placement of all the devices or blocks we need to wire everything together which is nothing but routing. While routing priority is given first to power and clock nets as they are very critical nets and then route other nets.

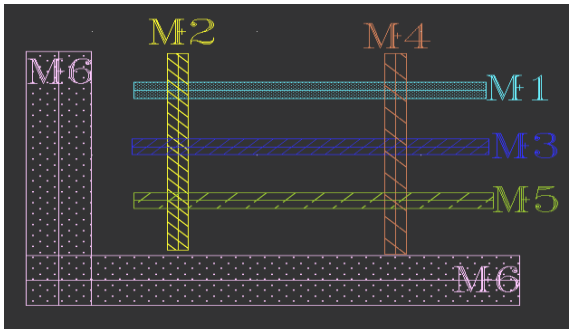

Figure 3.3 Metal orientations while Routing

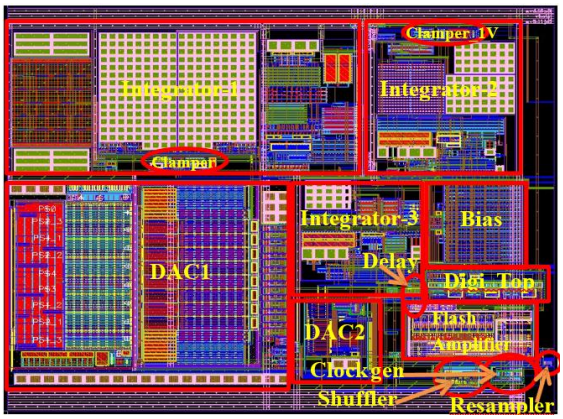

Figure 3.4 Top level Layout of ADC

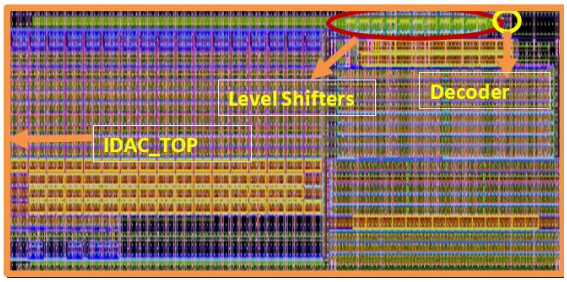

Figure 3.5 Layout of DAC

Verification After the completion of floor plan, placement, routing the next step is to verify our layouts. Layouts drawn are verified by performing DRC, LVS checks. DRC stands for Design Rule Check which is to verify whether the layouts drawn are as per design rules provided by fabrication companies or not. LVS stands for Layout Versus Schematic which cross checks the layout with the schematic.

- Design rule check verifies the following

- Minimum width
- Minimum spacing
- Minimum enclosure
- Minimum extension

- Layout Versus Schematic verifies the following

- Number of Devices or Instances:
- Device Properties
- Connectivity

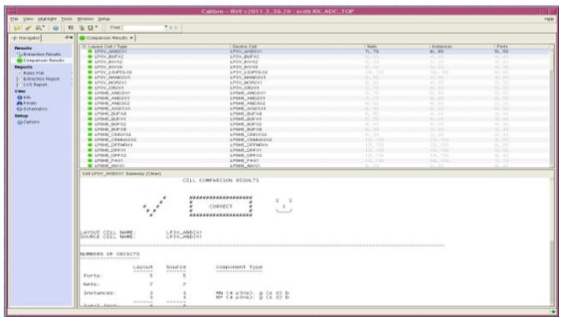

Figure 3.6 LVS check for ADC

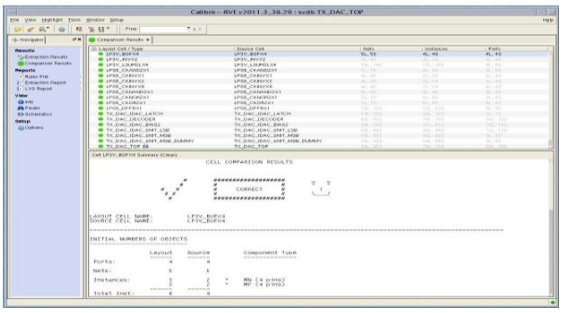

Figure 3.7 LVS check of DAC.

- ERC stands for electrical rule check which verifies the following

- External Connection Definition Rules
- Path Tracing Rules
- Nonfunctional Device Checking Rules
- Specific Connectivity

-EM check Electro migration check verifies whether specified current is passing through particular net or not. In some circuits for some sensitive, critical nets current specification is mentioned and with the change in the width of the metal EM also changes, so for maintaining the specified current in the nets appropriate width is used and care is taken such that no overflow occurs. EM check is performed on nets to make sure that current density is within the specified range.

- Parasitic Extraction is to find the resistance and capacitance of the nets. Parasitic extraction is important because if resistance or capacitance of any net is high it affects the output and can't acquire the simulated results of schematic. For lower metal layers resistance will be high and for higher metal layers resistance will be low so for power nets generally higher metal layers are used to decrease resistance for those nets to reduce parasitic affects.

IV. CONCLUSION

Present work gives an idea about Analog Layout Design and the issues in analog layout design. It helps to create a modular and hierarchically structured design for the generation of a regular and dense layout. Analog Layout design is done in four steps which we have seen in detail in earlier chapters, after completion of each step if we can run DRC and make sure it is clean then we can proceed to next step because after completionof routing phase if devices has to be moved due to n-well spacing or deep n-well spacing or any other issue then all the routing needs to be done again so if we make those spacing errors clean after placement itself at the end the errors that occurs will be of only routing and can be rectified easily.

LVS has to be taken care to prevent short and open circuits. While working on block level, LVS won't be a much issue but as we move on to top level routing gets more complex. If the top-level routing gets short with routing in block levels without our knowledge tracing it out will be a big issue, so try to avoid some metals in block levels so that we can use them in top level. Thus, if we can make sure of the connectivity getting LVS clean will be easy job. Ana- log layout design is like trial-and-error process and we can't make everything clean in a single pass, so we should be able to learn from errors and make it clean in minimum number of passes.
Issues in analog layout design are discussed in earlier Care has to be taken about parasitic effects as our layouts contains all metals, if these parasitic effects are discarded, they can degrade the circuit performance so try to minimize these parasitic effects. Matching of devices has to be as high as possible; the accuracy of the outputs from the matching devices depends on the matching level. Noise is the most critical issue as in mixed signal circuits the noise from digital blocks can affect sensitive analog blocks so proper isolation has to be provided for all blocks to protect from noise.

V. FUTURE SCOPE

Future scope in analog layout design is automation. In any technology digital blocks like decoders, multiplexers, gates etc. are done by automation as their functionality, properties do not change, but the analog blocks can't be done by automation as they are sensitive to outside environment.

Device properties, functionalities change from design to design, because one design may be low power design and other may be high power design. Recently super high threshold voltage devices are also coming to usage which can tolerate high powers also, so in all the designs same devices can't be used as the properties was changed hence automation in analog design is still a bottle neck. Though the entire design can't be done by automation there are some software tools for doing some phases of ana- log design like placement, routing but the disadvantage is those tools are not taking care of power related issues hence partially automation exists in analog design and still needs to be developed.

One more challenge in layout design is migration from one technology to other technology. As the technology changes the device properties, number of metal layers, metal properties, power consumption etc. changes. In migration we can't migrate from 130nm to 16nm directly, it is like migrating to nearby tech node i.e. in 130nm number of metal layers available is five and in 40nm number of metal layers is six so if we can adjust the metal layer properties by modifying library files it can be done to some extent, but this migration is not full-fledged as the number of metal layers increases with the decrease in tech node. In the same tech node migration tends to decrease in number of metal layers, cost reduces if the smaller number of metal layers is used in design and the cost can reduce up too few thousands of dollars. Migration in same tech node can be done by adjusting the one metal layer properties to other metal layer and modifying it accordingly.

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