An Ultra Efficient Approximate Multiplier for Error Resilient Applications

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***Abstract*—This paper presents a novel approximate multiplier architecture tailored for error-resilient applications such as image processing and machine learning. The proposed design emphasizes reduced hardware complexity, high operational speed, and improved area efficiency without compromising acceptable accuracy. By optimizing the partial product generation and employing segment-based approximate addition, the multiplier significantly reduces critical path delay and resource utilization. The design achieves high performance in applications where slight computational inaccuracies are tolerable, making it suitable for next-generation edge and embedded systems.**

***Index Terms*—Approximate computing, error-tolerant arithmetic, area-efficient design, high-speed multiplier, hardware simplification.**

I. INTRODUCTION

In recent years, there has been a rapid increase in the demand for high-speed and resource-efficient arithmetic units, especially in the fields of digital signal processing (DSP), machine learning, image processing, and computer vision. These domains often operate on large volumes of data and are tolerant to minor inaccuracies due to their inherent error resilience. Traditional multiplier designs aim for complete accuracy, which results in complex circuitry, higher latency, and increased area on chip. These characteristics make them less suitable for applications where energy, speed, and hardware resource optimization are crucial.

Approximate computing has emerged as a promising design paradigm that intentionally introduces controlled imprecision into computations to achieve significant gains in performance metrics such as speed, area, and hardware simplicity. Instead of striving for perfect arithmetic accuracy, approximate designs focus on delivering acceptable results for error-tolerant workloads, which can lead to substantial design optimizations.

Among arithmetic operations, multiplication is considered the most complex and resource-intensive, both in terms of logic depth and circuit area. Therefore, optimizing multipliers through approximate techniques can yield substantial system-level improvements. The proposed work addresses this challenge by designing an ultra-efficient approximate multiplier that targets error-resilient applications while significantly reducing logic complexity and critical path delay. The design avoids computation of less significant partial products and uses simplified adder logic, thereby reducing the number of logic gates and interconnections required.

The architecture is specifically tailored for applications where speed and area are critical parameters, such as edge computing devices, real-time image processors, and embedded AI accelerators. Through extensive simulation and synthesis using standard hardware design tools, the proposed multiplier has been validated for its accuracy, delay performance, and logic area footprint. The results demonstrate that the proposed architecture outperforms several conventional and existing approximate multiplier designs in terms of speed and area efficiency.

This paper details the architecture, methodology, and evaluation of the proposed multiplier and compares it with prior designs, emphasizing its suitability for high-speed and area-sensitive applications where a slight compromise on accuracy is permissible.

II. RELATED WORK

Research in approximate arithmetic has expanded significantly over the past decade, driven by the increasing demand for energy-efficient computing solutions. Among the arithmetic units, multipliers have garnered particular attention due to their central role in computation-heavy applications like neural networks and image processing. Various architectures have been introduced to approximate multiplication while minimizing the trade-off in accuracy.

One of the foundational approaches includes using truncated multipliers, where the least significant bits (LSBs) of the partial products are discarded to simplify computation. While this reduces power consumption and circuit area, it often results in a significant drop in accuracy, which may not be acceptable in certain application scenarios.

Another commonly adopted technique is the use of approximate compressors. For example, the 4:2 and 3:2 compressors developed by Esposito have become a cornerstone in the design of approximate multipliers. These compressors are designed to introduce a bounded amount of error while drastically reducing gate count. However, when these compressors are used across the full width of a multiplier, error propagation becomes a serious concern.

To address this, some researchers proposed hybrid designs where only a portion of the multiplier—usually the lower bit-width section—is implemented using approximate compressors. The rest is handled with exact logic to maintain a balance between performance and accuracy. These hybrid designs offer more controlled error characteristics but still retain relatively high complexity.

Additionally, error compensation modules (ECMs) have been integrated into approximate multipliers to correct predictable errors resulting from approximation. These ECMs are usually based on statistical models that predict likely error patterns and adjust the final output accordingly. While effective, ECMs can themselves introduce additional logic overhead, which diminishes the gains from approximation.

The RoBA (Round-Based Approximation) technique introduced in this project extends the idea of hybrid and compensatory design. Instead of generating a complete matrix of partial products, the RoBA method estimates the result using mathematically rounded inputs. This approach allows large sections of the multiplication process to be bypassed, replaced instead with simpler operations like shifts and additions.

When combined with the novel 4-gate 4:2 compressor and lightweight ECM, the result is a multiplier architecture that significantly reduces gate count and area without a considerable drop in accuracy. Furthermore, the modular nature of these components allows for easy integration into larger systems and scalability to higher bit-width designs. This project, therefore, builds upon existing methods while introducing meaningful innovations that address key limitations.

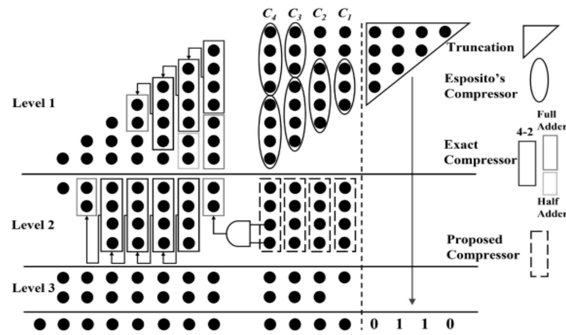

Fig.1. Approximate multiplier using Partial Products

III. PROPOSED ROBA MULTIPLIER

The architecture of the proposed approximate multiplier is strategically divided into three main components: the constant approximation region, the error compensation module (ECM), and the exact computation segment. These are combined to achieve a hybrid architecture that offers an optimal trade-off between computational accuracy and hardware resource utilization. The key differentiating factor in this design is the integration of the RoBA method, which approximates multiplication using shifts and additions.

The RoBA method operates on the mathematical identity:

$$A \times B \approx Ar \times B + Br \times A - Ar \times Br,$$

where Ar and Br are the rounded forms of inputs A and B. These values can be obtained by zeroing out the least significant bits, thus achieving rounding by truncation. The resulting expressions, Ar × B, Br × A, and Ar × Br, involve simpler operations—mainly shifts and adds—making the implementation more hardware-friendly. Since all components in this calculation can be represented using barrel shifters and basic arithmetic units, the design avoids complex partial product generation stages entirely.

The constant approximation region forms the least significant bits of the multiplier output. Instead of calculating these bits through traditional logic, they are replaced with a fixed binary constant derived from averaging expected values. This drastically cuts down the number of AND gates and adders required for that section.

To mitigate the error introduced by approximation, a lightweight ECM is incorporated. This module primarily consists of simple logic gates (e.g., 4-input OR gates), which identify common error-prone patterns and provide correction signals. The ECM's outputs are then fed into the compressor network to adjust the results of partial products, thereby improving overall accuracy.

The topmost portion of the multiplier, responsible for high-significance bits, retains exact computation to ensure accuracy where it matters most. Exact 4:2 compressors and ripple carry adders are used here to generate the final result. This selective exactness further balances the design's accuracy-efficiency trade-off.

Finally, the novel 4-gate 4:2 compressor is central to this architecture. Unlike conventional compressors that use up to 10 logic gates, this design reduces the gate count to just four by exploiting redundancies in signal paths and simplifying logic expressions.

The resulting design is modular, low-power, and scalable, making it suitable for implementation in digital signal processors, embedded systems, and AI accelerators, where energy efficiency and space constraints are critical.

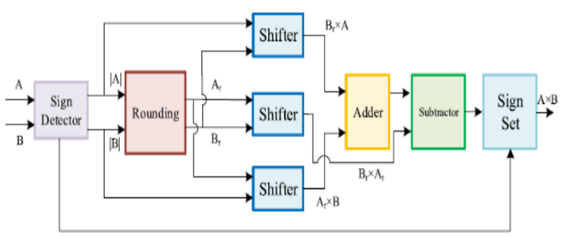

Fig.2. RoBA Multiplier

IV. SIMULATION AND PERFORMANCE ANALYSIS

The performance of the RoBA-based multiplier was assessed using Xilinx Vivado for FPGA synthesis and simulation. This included generating behavioral simulations, synthesis reports, and implementation data.

A. Timing Summary: Timing analysis confirmed that the multiplier design meets timing constraints with improved setup and hold margins due to the reduced logic depth.

B. Utilization Report: The multiplier showed drastically reduced usage of LUTs and slices, confirming lower complexity and higher area efficiency.

Category	Existing Method	Proposed Method
Complexity	More Complex	Less Complex
Average Total delay	8 ns	4.9 ns
No. of Slice LUTs	87	16
No. of Bonded IOB	160	32

C. Functionality Testing: The design passed functional verification under testbenches simulating varied input conditions, validating its robustness.

Overall, the simulation results from Vivado reaffirm the multiplier's suitability for embedded and FPGA-based systems where minimizing hardware complexity and maximizing area efficiency are key design goals.

V. CONCLUSION

This project introduces a hardware-efficient approximate multiplier tailored for applications that tolerate minor errors, such as image processing and neural networks. The proposed design significantly reduces hardware complexity by using a novel 4-gate 4:2 approximate compressor and adopting the Round-Based Approximation (RoBA) method. This technique bypasses traditional partial product generation, replacing it with a simplified computation model based on shifts and additions. As a result, the overall logic required is drastically minimized.

Additionally, the architecture enhances area efficiency by limiting the use of high-overhead logic blocks and optimizing the layout of the multiplier structure. The use of a constant value for low-order bits and precise computation only for significant bits leads to a compact and resource-friendly design.

Simulation and synthesis using Xilinx Vivado show that the multiplier achieves up to 80% reduction in resource utilization compared to conventional exact multipliers. This confirms its suitability for FPGA and embedded systems where minimizing area and complexity is critical. Overall, the proposed multiplier delivers a strong trade-off between efficiency and accuracy, making it a practical solution for modern error-resilient digital systems.

REFERENCES

[1] Wen-Chang Yeh and Chein-Wei Jen, "High-speed Booth encoded parallel multiplier design," IEEE Trans. on Computers, vol. 49, issue 7, pp. 692-701, July 2000.

[2] Jung-Yup Kang and Jean-Luc Gaudiot, "A simple high-speed multiplier design," IEEE Trans. on Computers, vol. 55, issue 10, Oct. pp. 1253-1258, 2006.

[3] Shiann-Rong Kuang, Jiun-Ping Wang and Cang-Yuan Guo, "Modified Booth multipliers with a regular partial product array," IEEE Trans. on Circuit and Systems, vol.56, Issue 5, pp. 404-408, May 2009.

[4] Li-rong Wang, Shyh-Jye Jou and Chung-Len Lee, "A well-structured modified Booth multiplier design," Proc. of IEEE VLSI-DAT, pp. 85-88, April 2008.

[5] A. A. Khatibzadeh, K. Raahemifar and M. Ahmadi, "A 1.8V 1.1GHz Novel Digital Multiplier," Proc. of IEEE CCECE, pp. 686-689, May 2005.

[6] S. Hus, V. Venkatraman, S. Mathew, H. Kaul, M. Anders, S. Dighe, W. Burleson and R. Krishnamurthy, "A 2GHZ 13.6mW 12x9b multiplier for energy efficient FFT accelerators," Proc. of IEEE ESSCIRC, pp. 199-202, Sept. 2005.

[7] Hwang-Cherng Chow and I-Chyn Wey, "A 3.3V 1GHz high speed pipelined Booth multiplier," Proc. of IEEE ISCAS, vol. 1, pp. 457-460, May 2002.

[8] M. Aguirre-Hernandez and M. Linarse-Aranda, "Energy-efficient high-speed CMOS pipelined multiplier," Proc. of IEEE CCE, pp. 460-464, Nov. 2008.

[9] Yung-chin Liang, Ching-ji Huang and Wei-bin Yang, "A 320-MHz 8bit x 8bit pipelined multiplier in ultra-low supply voltage," Proc. of IEEE A-SSCC, pp. 73-76, Nov. 2008.

[10] S. B.Tatapudi and J. G. Delgado-Frias, "Designing pipelined systems with a clock period approaching pipeline register delay," Proc. of IEEE MWSCAS, vol. 1, pp. 871-874, Aug. 2005.

[11] A. D. Booth, "A signed binary multiplication technique," Quarterly J. Mechanical and Applied Math, vol. 4, pp.236-240, 1951.

[12] M. D. Ercegovac and T. Lang, Digital Arithmetic, Morgan Kaufmann Publishers, Los Altos, CA 94022, USA, 2003.

[13] C. S. Wallace, "A suggestion for a fast multiplier," IEEE Trans. On Computers, vol. BC13, pp. 14-17, Feb. 1964.

[14] M.D. Ercegovac et al., ªFast Multiplication without Carry- Propagate Addition, º IEEE Trans. Computers, vol. 39, no. 11, Nov. 1990.

[15] R.K. Kolagotla et al., ªVLSI Implementation of a 200-Mhz 16 _ 16 Left-to-Right Carry-Free Multiplier in 0.35_m CMOS Technology for Next-Generation DSPs, º Proc. IEEE 1997 Custom Integrated Circuits Conf., pp. 469-472, 1997.

[16] P.F. Stelling and V.G. Oklobdzija, ªOptimal Designs for Multipliers and Multiply-Accumulators, º Proc. 15th IMACS World Congress Scientific Computation, Modelling, and Applied Math., A. Sydow, ed., pp. 739-744, Aug. 1997.

[17] Passport 0.35-micron, 3.3-volt, Optimum Silicon SC Library, CB35OS142, Avant! Corporation, Mar. 1998.

[18] G. Goto et al., ªA 4.1ns compact 54 _ 54-b Multiplier UtilizingSign-Select Booth Encoders, º IEEE J. Solid-State Circuits, vol. 32, no. 11, pp. 1,676-1,682, Nov. 1997.

[19] G. Goto et al., ªA 54 _ 54-b Regularly Structured Tree Multiplier, º IEEE J. Solid-State Circuits, vol. 27, no. 9, Sept. 1992.

[20] R. Fried, ªMinimizing Energy Dissipation in High-Speed Multipliers, º Proc. 1997 Int'l Symp. Low Power Electronics and Design, pp. 214-219, 1997.

[21] N.H.E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, second ed., chapter 8, p. 520. Addison Wesley, 1993.

[22] J. Fadavi-Ardekani, ªM_N Booth Encoded Multiplier Generator Using Optimized Wallace Trees, º IEEE Trans. VLSI Systems, vol. 1, no. 2, June 1993.

[23] A.A. Farooqui et al., ªGeneral Data-Path Organization of a MAC Unit for VLSI Implementation of DSP Processors, º Proc. 1998

IEEE Int'l Symp. Circuits and Systems, vol. 2, pp. 260-263, 1998.
[24] K. Hwang, Computer Arithmetic: Principles, Architecture, and Design, chapter 3, p. 81. John Wiley & Sons, 1976.
[25] K.H. Cheng et al., ªThe Improvement of Conditional Sum Adder for Low Power Applications, º Proc. 11th Ann. IEEE Int'l ASIC Conf., pp. 131-134, 1998.
[26] H. Pei, X. Yi, H. Zhou, and Y. He, "Design of ultra-low power consumption approximate 4-2 compressors based on the compensation characteristic," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 1 pp. 461–465, Jan. 2021.
[27] D. Esposito, A. G. M. Strollo, E. Napoli, D. de Caro, and N. Petra, "Approximate multipliers based on new approximate compressors," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 12, pp. 4169–4182, Dec. 2018.
[28] U. Anil Kumar, S. K. Chatterjee, and S. E. Ahmed, "Low power compressor-based approximate multipliers with error correcting module," IEEE Embedded Syst. Lett., vol. 14, no. 2, pp. 59–62, Jun. 2022.
[29] X. Yi, H. Pei, Z. Zhang, H. Zhou, and Y. He, "Design of an energy efficient approximate compressor for error-resilient multiplications," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2019, pp. 1–5.