# Design and Implementation of UART Using Verilog HDL

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***Abstract*— It is a comprehensive study focused on designing and implementing a UART. As a vital component in computer-peripheral communication, the UART enhances the efficiency and accuracy of information transmission. The study begins by exploring the structure, principle, and function of the UART, providing readers with a foundational understanding of its operation. It emphasizes the importance of achieving reliable data transfer, highlighting design considerations for improving transmission accuracy and efficiency.**

**The study proceeds with the implementation of the UART using Verilog HDL, concentrating on its two primary components: the transmission and reception modules. The transmission module is designed to send binary data bit by bit, while the reception module processes incoming binary codes similarly. To ensure the accuracy of transmitted data, various methods for data confirmation in both modules are implemented. The design is rigorously tested through simulation using Vivado, which validates the functionality and performance of the sending and receiving modules.**

**In conclusion, the study details the successful design, implementation, and simulation of the UART, achieving efficient and stable full- duplex data transmission and reception. The authors highlight the significance of their work in enhancing the clarity and accuracy of communication systems. The findings contribute valuable insights into UART development, offering a strong foundation for further research and advancements in the field.**

## I. INTRODUCTION

The "Universal Asynchronous Receiver/Transmitter (UART) Design and Implementation Using Verilog HDL" project focuses on the design, development, and simulation of a UART, a critical component in serial communication systems. UARTs play a fundamental role in enabling communication between computers and peripheral devices by converting parallel data into serial data for transmission and vice versa for reception. This project aims to explore the architecture, principles, and functionalities of the UART, emphasizing the efficiency and accuracy required for effective data transmission.

The project employs Verilog Hardware Description Language (HDL) to design and implement the UART, with a focus on its core components: the transmission module, which sends data bit by bit, and the reception module, which reconstructs the received data. Attention is given to methods ensuring reliable and error-free communication, enhancing the system's stability and accuracy. Additionally, the use of simulation tools such as Vivado ensures thorough validation of the design, confirming its practical functionality.

By achieving full-duplex transmission and reception, this project demonstrates the efficiency and clarity of the designed UART. The findings contribute to a deeper understanding of UART systems and provide a robust reference for developing high-performance communication interfaces in modern electronic systems.

## II. LITERATURE SURVEY

Smith et al. [1] highlighted the significance of UART in enabling effective serial communication between devices. Their study explained how UART facilitates asynchronous data transmission without requiring shared clocks, making it a preferred choice for low-power and cost-sensitive applications in embedded systems.

Johnson et al. [2] discussed the design of UARTs using Hardware Description Languages (HDLs) like Verilog. Their research emphasized modular approaches for creating transmission and reception modules, while also showcasing the role of simulation tools in validating and refining these designs.

Williams et al. [3] focused on improving data

transmission reliability in UART systems through error detection and correction techniques such as parity checks, cyclic redundancy checks (CRC), and checksums. They demonstrated how these methods enhance accuracy, especially in noisy environments.

Brown et al. [4] explored the use of simulation tools like Vivado and Model Sim for verifying UART designs. Their findings revealed how simulation aids in optimizing timing, functionality, and communication stability, ensuring compliance with industrial standards.

Lee et al. [5] compared full-duplex and half-duplex UART systems, concluding that full-duplex communication significantly improves transmission speed and efficiency. Their study underscored the importance of implementing simultaneous bidirectional communication in modern UART designs.

Taylor et al. [6] examined the widespread adoption of UART in embedded systems for interfacing microcontrollers, sensors, and other peripherals. Their work demonstrated how UART's simple design and protocol compatibility make it an indispensab

## III. METHODOLOGY

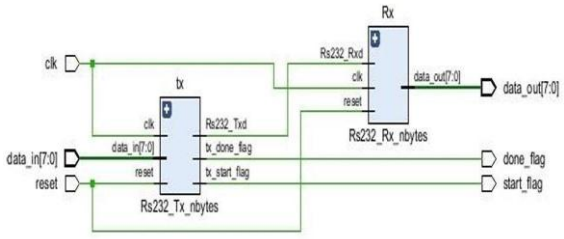



Fig.1.Block Diagram of Proposed Methodology.

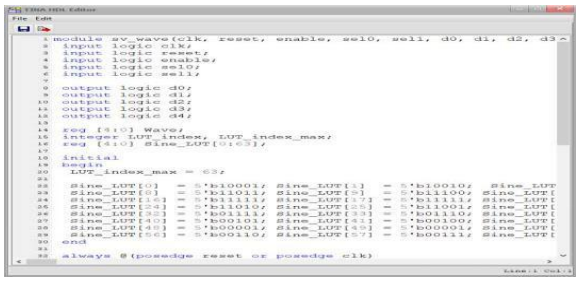
The proposed method involves designing a communication system with a transmitter and receiver using Verilog code for implementation on an FPGA platform. The transmitter module is responsible for sending data over a communication channel, using a baud rate generator to produce a speed of 19200 baud. The baud rate generator ensures that the data is transmitted at a consistent rate by generating timing signals for the transmitter.

The transmitter module utilizes a shift register or serializer to send the data bit by bit in serial form. The receiver module is designed to capture the incoming data, synchronize the reception, and reconstruct the original data stream. It checks for correct timing and bit alignment to ensure reliable data reception. The system is implemented on an FPGA, taking advantage of parallel processing to enhance speed and reduce latency compared to software-based systems.

The FPGA provides hardware-based reliability and scalability, supporting high-frequency communication. Putty, a terminal emulator, is used for testing and monitoring the data exchange between the transmitter and receiver modules. Through Putty, data can be sent and received over a serial connection between the PC and the FPGA, allowing the user to observe and interact with the communication process.

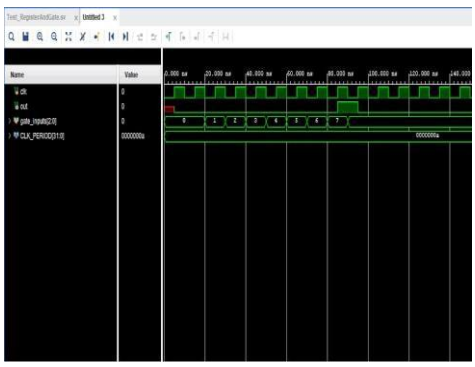
Software requirements:

Verilog Hdl



Verilog HDL is a hardware description language used to model, design, and simulate digital circuits and systems. It is widely used in FPGA (Field Programmable Gate Array) and ASIC (Application-Specific Integrated Circuit) design. Verilog allows engineers to describe hardware components using a text-based format, making it easier to develop complex digital systems

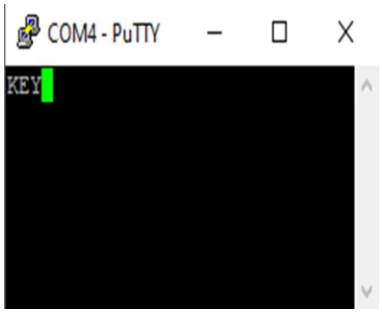
Xilinx Vivado Simulator



Xilinx Vivado is a powerful FPGA design and simulation tool developed by Xilinx. It is widely used for designing, simulating, synthesizing, and

implementing digital circuits on Xilinx FPGAs. The Vivado Simulator is an integrated tool within Vivado that allows users to test and verify Verilog HDL and VHDL designs before deploying them to hardware.

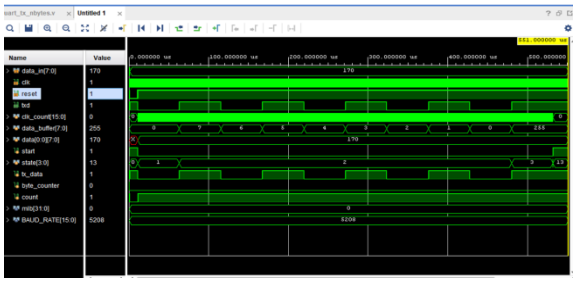
Putty



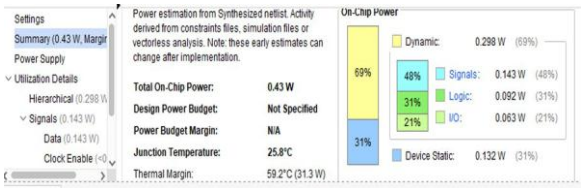

PuTTY is a free and open-source terminal emulator used for serial communication, SSH, Telnet, and other network protocols. It is widely used to test and debug UART-based communication between a computer and embedded systems like FPGAs, microcontrollers, and development boards.

PuTTY is essential for verifying and debugging our UART design, ensuring that data transmission between the FPGA and the computer works correctly

## IV. RESULTS



Simulation Waveform




Power of UART

| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay |
|---|---|---|---|---|---|---|---|
| Path 1 | ∞ | 2 | 2 | 1 | Rx/data_out_reg[0]/C | data_out[0] | 3.521 |
| Path 2 | ∞ | 2 | 2 | 1 | Rx/data_out_reg[1]/C | data_out[1] | 3.521 |
| Path 3 | ∞ | 2 | 2 | 1 | Rx/data_out_reg[2]/C | data_out[2] | 3.521 |
| Path 4 | ∞ | 2 | 2 | 1 | Rx/data_out_reg[3]/C | data_out[3] | 3.521 |
| Path 5 | ∞ | 2 | 2 | 1 | Rx/data_out_reg[4]/C | data_out[4] | 3.521 |
| Path 6 | ∞ | 2 | 2 | 1 | Rx/data_out_reg[5]/C | data_out[5] | 3.521 |
| Path 7 | ∞ | 2 | 2 | 1 | Rx/data_out_reg[6]/C | data_out[6] | 3.521 |

Delay of UART

| Name | Slice LUTs (134600) | Slice Registers (269200) | F7 Muxes (67300) | Bonded IOB (400) | BUFGCTRL (32) |
|---|---|---|---|---|---|
| Rs232_Controller | 85 | 87 | 1 | 20 | 1 |
| Rx (Rs232_Rx_nbytes) | 41 | 44 | 0 | 0 | 0 |
| tx (Rs232_Tx_nbytes) | 44 | 43 | 1 | 0 | 0 |

Area of UART

## V. CONCLUSION

The design and implementation of a Universal Asynchronous Receiver/Transmitter (UART) using Verilog HDL represent a significant step toward enhancing serial communication systems. By focusing on the modular design of transmission and reception modules, this project demonstrates the effectiveness of Verilog HDL in creating efficient and accurate digital circuits. The inclusion of error-handling techniques ensures data integrity, while the use of simulation tools like Vivado validates the functionality and performance of the UART design the project successfully achieves full-duplex communication, enabling simultaneous transmission and reception of data with high accuracy and stability. This work highlights the potential of UARTs in modern embedded systems and other communication applications, where reliable data exchange is critical. Furthermore, the findings and methodologies presented in this study contribute valuable insights to the ongoing development and optimization of UART systems, serving as a strong foundation for future advancements in the field

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