A Quadruple Multilevel Inverter for Small Scale PV Applications

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Abstract: **Two-stage power conversations are required to interface the PV systems to the grid or industrial loads. Firstly, high-gain DC-DC conversion allows each stage to operate at its optimal efficiency point, maximizing overall energy conversion efficiency. Secondly, the inverter stage ensures that the generated AC power is synchronized, stable, and conforms to grid standards, maintaining power quality. From an economic perspective, avoid cost implantation for the DC-DC conversation for small-scale PV systems on the distribution side. This paper presents an efficient nine-level quadruple multilevel inverter (MLI). The proposed MLI works on the concept of the Switched Capacitor (SC) technique. The SCMLI switches level shifting PWM technique is adopted for better turn on and off. The proposed SC Multilevel Inverters are particularly attractive for applications with high-quality AC output waveforms, reduced voltage stress, and improved power conversion efficiency with a fewer component.**

1. INTRODUCTION

Solar photovoltaic (PV) power systems offer a range of important benefits that contribute to sustainable energy generation, grid stability, environmental conservation, and economic growth [1]. Grid-connected solar PV systems harness sunlight to generate electricity without emitting greenhouse gases or pollutants. They provide a clean and renewable energy source, contributing to efforts to mitigate climate change and reduce reliance on fossil fuels.Solar PV systems help reduce carbon emissions, air pollution, and water consumption associated with traditional fossil fuel-based electricity generation. Thus, using solar PV systems improves air quality, protects ecosystems, and mitigates the impacts of global warming [2].

Small-scale photovoltaic (PV) power generation, often referred to as distributed solar energy, plays a crucial role in the global energy landscape and offers numerous benefits. Distributed photovoltaic (PV) power generation refers to installing solar photovoltaic systems on rooftops, buildings, or other small-scale locations, often close to the point of consumption [3].Small-scale PV systems enable energy generation at or near the point of consumption, reducing the need for long-distance electricity transmission. This decentralized approach enhances energy security and grid resilience [4].Generating electricity near where it is consumed minimizes transmission and distribution losses that typically occur when electricity is transported over long distances through power lines.

Multilevel inverters can be integrated with energy storage systems to provide grid stabilization and the capability to store excess solar energy for later use. Distributed PV systems with multilevel inverters can be integrated into innovative grid frameworks, enabling real-time monitoring, remote control, and demand response [5].Diode-clamped (neutral-point clamped), flying capacitors, and cascaded H-bridge inverters are viable MLI. Diode clamped [6] MLI have lower voltage stress on switches compared to traditional two-level inverters and simplicity of control and modulation. Fewer power semiconductors are needed compared to some other multilevel topologies. However, the disadvantages are a limited number of voltage levels. Reduced efficiency at lower modulation indices and requires voltage balancing among the capacitors. Flying Capacitor [7] Inverters have higher voltage levels than diode-clamped inverters and reduced switch voltage stress. Improved efficiency at lower modulation indices compared to diode-clamped inverters. The disadvantages of FC are the complexity of capacitor voltage balancing, increased component count and cost due to multiple capacitors, and limited power handling capacity due to capacitor voltage ratings. Cascaded H-Bridge Inverters [8] has the highest voltage levels among the discussed topologies. Improved output waveform quality, better efficiency across modulation indices, and flexibility to handle high power levels through the series connection of H-bridge modules are possible. Limitations with CHB

include an increased number of power semiconductor switches, leading to higher costs and more complex control and modulation algorithms. Voltage balancing among the H-bridge modules is much more difficult.

Active research is undertaken on the PV system's Switched Capacitor Multilevel Inverters (SCMLI). A SCMLI utilizes switched capacitors to generate multiple voltage levels for converting DC power to AC power [9]. Multilevel inverters, including those with switched capacitors, are used to improve the quality of the AC output waveform, reduce voltage stress on power devices, and enhance power conversion efficiency in various applications.In [10-11], studies presented five-level output voltage with a gain of two. The design of the seven-level multilevel inverter based on the SC technique is addressed in [12]. The SC technique MLI approach for PV systems is extended by [13] for a nine-level output voltage.

2. SYSTEM CONFIGURATION

Broadly, two categories are available to interface the grid or load to the PV system

A. Two-stage grid interfaced PV system:

A two-stage photovoltaic (PV) system is a configuration in which the PV power generation is split into two distinct stages or subsystems. Each stage performs a specific function to optimize efficiency, power quality, or system performance. A two-stage PV system involves a Maximum Power Point Tracking (MPPT) stage. The primary function of this stage is to extract the maximum available power from the PV panels under varying environmental conditions, such as changing sunlight intensity and temperature. MPPT is achieved through specialized power electronics that control the voltage and current supplied to the PV panels to ensure they operate at their optimal operating point.

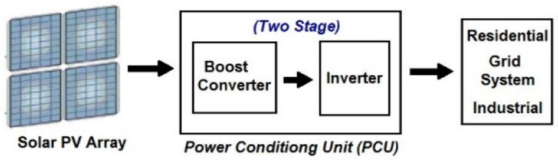

Fig.1 Schematic structure of the two-stage PV system

B. Single-stage grid interfaced PV system:

In this case, a well-operated multilevel inverter can opt to deliver power to the AC load. Multilevel inverters provide high-quality sinusoidal output voltage with reduced harmonics. It helps improve power quality by minimizing voltage distortions and reducing the potential for grid disturbances. Multilevel inverters can achieve higher efficiency than traditional two-level inverters, especially in medium and high-power applications. This efficiency enhancement contributes to improved energy conversion and reduced losses. Reduced Multilevel inverters generate lower EMI due to their advanced switching techniques, contributing to a cleaner and quieter electrical environment. Multilevel inverters can regulate the output voltage more accurately, which is beneficial for maintaining voltage stability in the distribution network, especially during grid voltage fluctuations. Distributed PV power generation can be smoothly integrated into the grid using multilevel inverters. The ability of multilevel inverters to generate high-quality AC power aligns well with grid requirements. Multilevel inverters have reduced voltage stress on power semiconductor devices, which can extend the inverter's lifespan and improve its reliability.

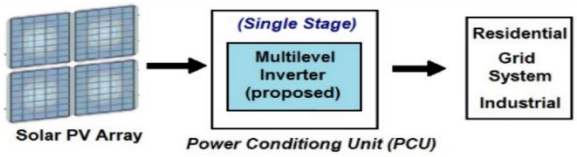

Fig.2 Schematic structure of the single-stage PV system

3. PROPOSED NINE LEVELS OF MLI TOPOLOGY

A SCMLI uses a combination of capacitors and power switches to create a staircase-like waveform by connecting capacitors in different configurations. Multiple voltage levels can be generated at the output by selectively charging and discharging the capacitors and connecting them in series or parallel. These voltage levels approximate a sine wave, resulting in a higher-quality AC waveform than traditional two-level inverters. The switching pattern for nine levels of MLI for both positive and negative levels is depicted in Fig.3.

Positive Voltage Levels:

Mode 1: In this mode, only the g_1, g_6, and g_{10} switches are triggered to obtain V_{out} =0. At the same time, Capacitor C_1 charges by turning on the g_3, g_4, g_5, and g_7 switches.

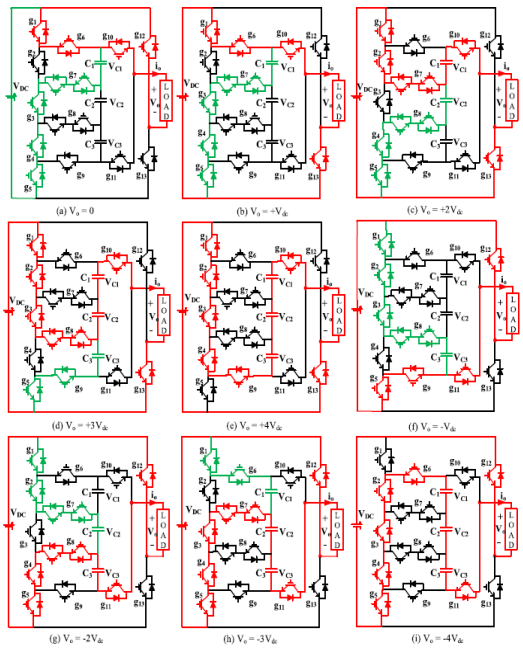

Fig.3 Operating modes of the proposed nine-level output voltage topology

Mode 2: In this state, to obtain $+V_{dc}$ as the output voltage level, switches g_1, g_6, g_{10}, and g_{13} are triggered. Similarly, there were no alters in the operation of the capacitor C_1 switches. In this duration, C_1 charges up to V_{dc} and capacitors C_2 and C_3 in floating mode.

Mode 3: In this case, switches g_1, g_2, g_7, g_{10}, and g_{13} are turned on, and capacitor C_1 is connected in series to the input PV source, so $+2V_{dc}$ is available as output voltage. During this mode, capacitor C_2 is charged by turning on the g_4, g_5, and g_8 switches, and capacitor C_3 is in a floating condition.

Mode 4: In this mode, to get the output voltage as $3V_{dc}$, the charged capacitors C_1 and C_2 are connected in series with the input PVsource by triggering the switches g_1, g_2, g_3,g_8, g_{10}, and g_{13}. Simultaneously, C_3 is charged to V_{dc} by turning on the $g_5$and g_9 switches.

Mode 5: To achieve $+4V_{dc}$ output voltage level, capacitors (C_1, C_2, and C_3) are connected in series to the input PV source by triggering g1, g2, g3, g4, g9, g10, and g13 switches.

Negative Voltage Levels:

Mode 1: To obtain - V_{dc} output voltage, g5, g_9, g_{11}, and g_{12} switches are triggered. At the same time, g_1, g_2, g_3, and g_8 switches are turned on to charge capacitor C_3. During this time, capacitors C_3 and C_1 are in floating mode.

Mode 2: The g_4, g_5, g_8, g_{11}, and g_{12} switches are triggered in this state. To yield a $2V_{dc}$ output voltage, capacitor C_3 is connected and cascaded to the input PV source.In this case, capacitor C_2 charges to V_{dc} by turning on the g_1, g_2, and g_7 switches, and capacitor C_1 is in floating mode.

Mode 3: In this mode, g_3, g_4, g_5, g_7, g_{11}, and g_{12} are triggered, and capacitors C_2 and C_3 in series input PV source to get - $2V_{dc}$ output voltage level. At the same time, C_1 is charged by turning on the g1 and g6 switches.

Mode 4: For-4Vdc output voltage level, the switches g_2, g_3, g_4, g_5, g_6, g_{11}, and $g_{12}$are turned on so C_1, C_2 and C_3 in series with the PV source.

Level Shifted Pulse width modulation (LS-PWM):

Level-Shift Pulse Width Modulation (LS-PWM) is a modulation technique used in power electronic systems to generate variable-width pulse signals that control the switching of semiconductor devices (typically power transistors or IGBTs) in voltage source inverters, converters, and other switching applications. It is primarily employed in applications like motor drives, uninterruptible power supplies (UPS), and power factor correction systems. LS-PWM is designed to reduce voltage stress on switching devices and improve overall efficiency. Traditional Pulse Width Modulation (PWM) involves alternately switching a voltage source inverter's high-side and low-side switches to generate an AC waveform with variable voltage and frequency. However, this method can lead to high-voltage transients across the switches during transitions, which can stress the devices and cause efficiency losses.

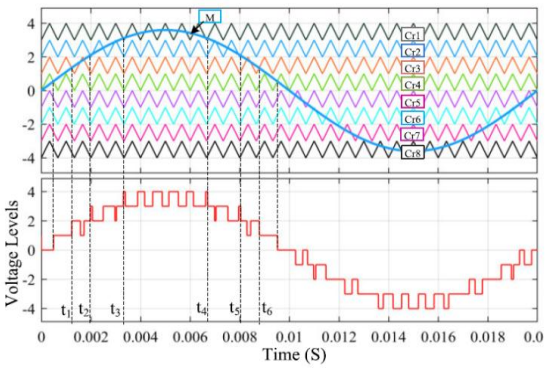

Fig.4a. Level Shifted Pulse Width Modulation.

In LS-PWM, an additional set of switches and diodes are added to the inverter configuration. This additional circuitry shifts the voltage levels at the inverter output, reducing the voltage stress on the main switches.LS-PWM generates pulse signals for

both high-side and low-side switches while considering the shifted voltage levels. This technique reduces the voltage stress across the main switches, enhancing their reliability and efficiency. LS-PWM inherently balances the voltages across the switches, which is especially important in multilevel inverter topologies. This balance further contributes to reduced stress on the components. The gate signal pattern for triggering the switches is shown in Fig. 4b.

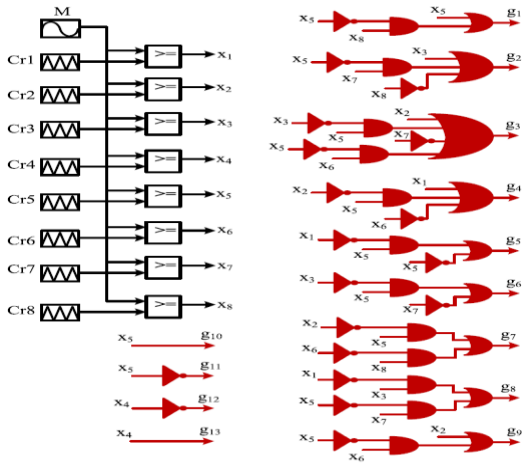

Fig. 4b. Gate signal pattern for triggering the switches

4. SIMULATION RESULTS

The performance of the proposed PV-based 9-level MLI converted is assessed under different conditions.

Case 1: Constant PV source and balanced load:
In this scenario, a balanced RL load of 100 ohms and 120mH is connected to the power system network. The simulation responses under this condition, such as output voltage, load current, and each capacitor voltage, are shown in Figs. 5 (a-d) respectively.

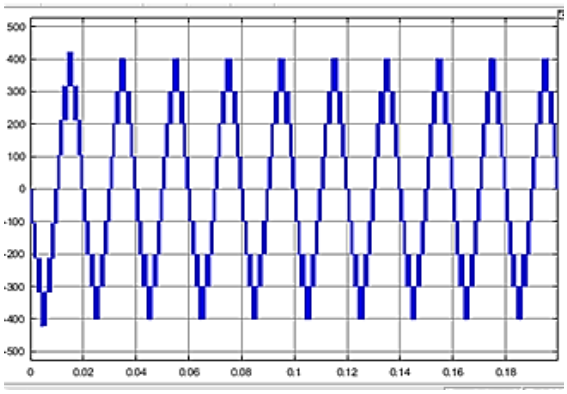

Fig.5a Output voltage

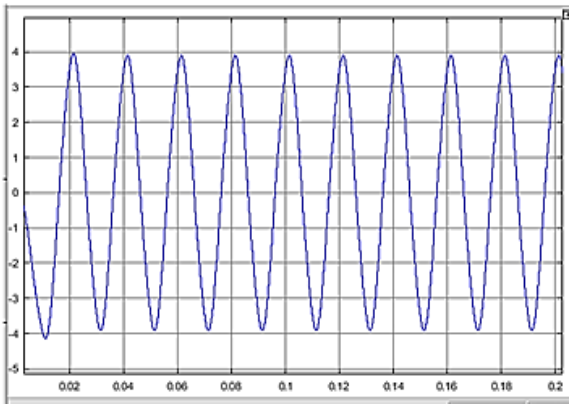

Fig.5b Load current

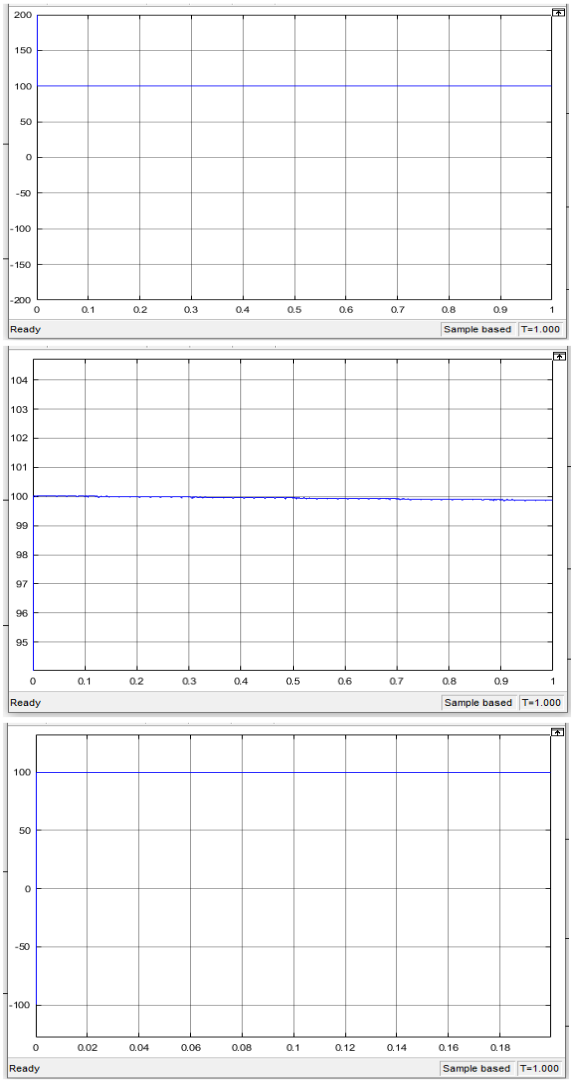

Fig.5c Capacitor Voltages (Vc_1, Vc_2 and Vc_3)

PV produces a constant voltage of 100V, and each capacitor charges up to 100V, so the output voltage response confirms that the proposed method provides balanced nine-level output voltages. The total harmonic distortion (THD) of the load voltage shows that the harmonic content in the output voltage is 14%.

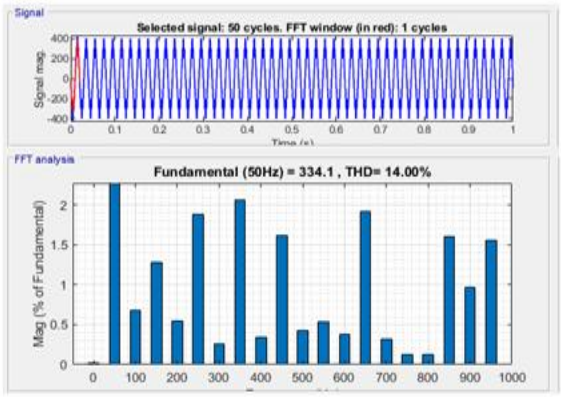

Fig.5d THD plot of the output voltage

Case 2: Constant PV source and unbalanced load:
An unbalanced load is connected to the power system network in this scenario. The simulation responses under this condition, such as output voltage, load current, and each capacitor voltage, are shown in Figs. 6 (a-c).

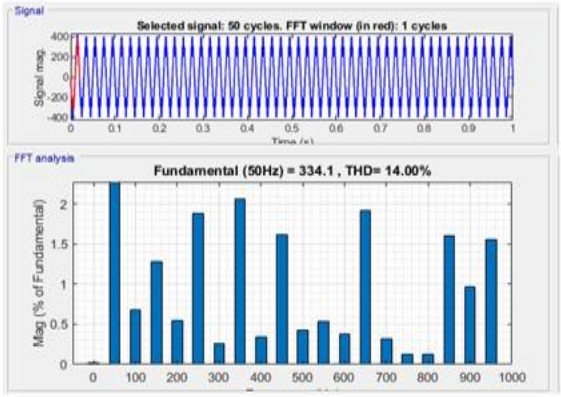

Fig.6a Output voltage

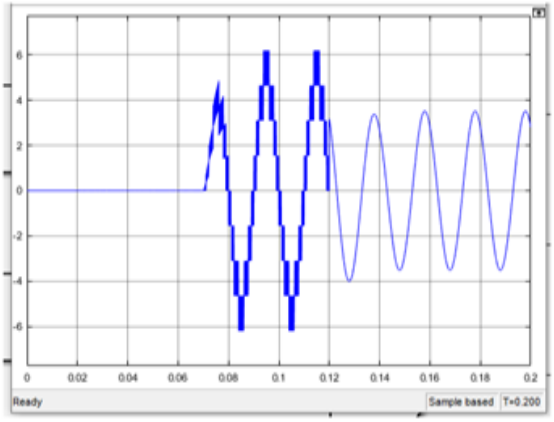

Fig.6b Load current

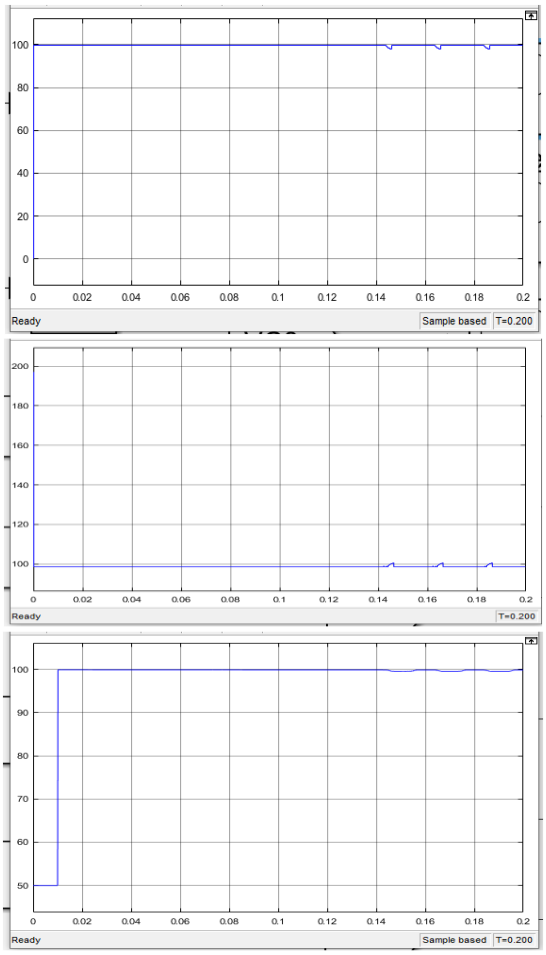

Fig.6c Capacitor Voltages (Vc_1, Vc_2 and Vc_3)

This unbalanced load is considered a no load, a 50-ohm resistive load, and 50 ohms plus 100mH inductive load during different time sequences. The proposed system has a stable 400V as the nine-level voltage level, even for the unbalanced load condition.

Case 3: Variable PV source: The output voltage and current are identified under dynamic input PV voltage changes conditions. The simulation responses in this scenario, such as output voltage, load current, and each capacitor voltage, are shown in Figs. 7(a-c).

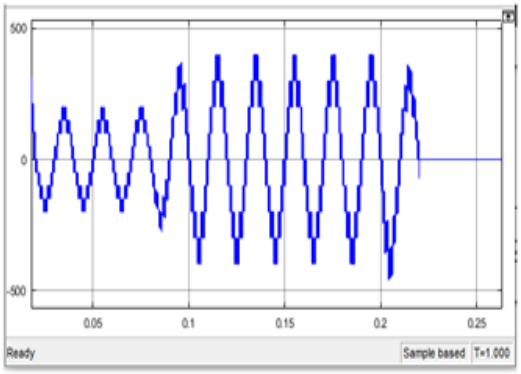

Fig. 7a Output Voltage

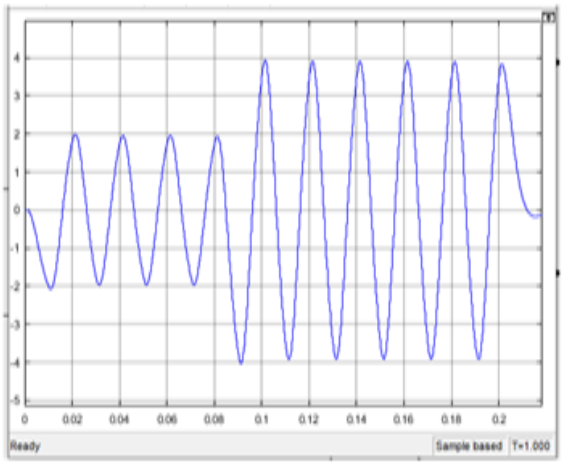

Fig. 7b Load Current

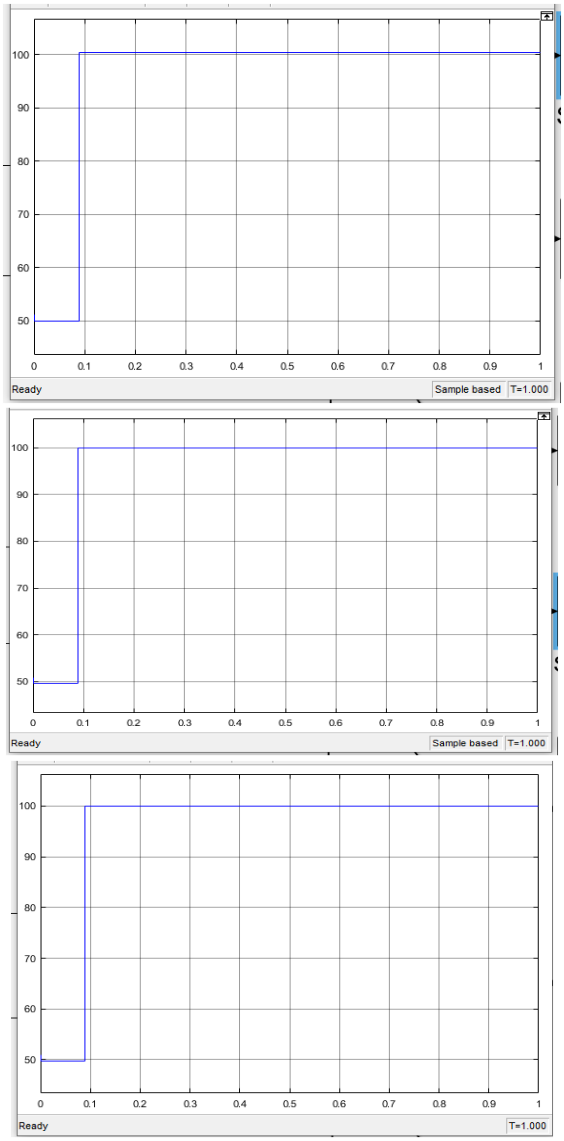

Fig.7c Capacitor Voltages (Vc_1, Vc_2 and Vc_3)

In this condition, the PV voltage changes from 50V to 100V, and the proposed method exhibits a 400V balanced nine-level output voltage. According to input voltage changes, capacitor voltages change quickly and settle at 100V.

5. CONCLUSION

This paper presents a switch capacitor technique based on nine-level quadruple MLI for small-scale solar PV systems. The proposed SCMLI converter provides better transient-free nine-level output voltage levels for constant input source and balanced load like by varying load types (no load, resistive load, and RL loads), and even variable input source and constant load operating conditions. The observed voltage, current, and total harmonic distortion (THD) waveforms provided valuable insights into the inverter's behavior under different scenarios. The harmonic content of the output voltage is also of considerable value of 14%. For the efficient operation of SCMLI switches, the level-shifting PWM technique is adopted over the popular traditional PWM techniques.

Overall, the study confirms that the proposed SCMLI topology effectively enhances power quality and efficiency while maintaining stability across different load and operating conditions. These findings highlight the inverter's suitability for small-scale PV applications and provide a foundation for further optimization in terms of efficiency, control strategies, and grid integration.

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