A Hybrid PWM Method for Capacitor Voltage Balancing To Enhance T-Type NPC Inverter Performance

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Abstract: **Recent years have seen a surge in research into grid-tied multilevel inverters (MLIs) fed by solar photovoltaic (PV) because of their unique characteristics in comparison to two-level voltage source inverters (VSIs). The reduction of total harmonic distortion (THD), dc-link voltage imbalance problems, power loss reduction, and thermal stress mitigation are all difficult aspects of maintaining the power quality of MLIs, and they are all greatly impacted by the pulse width modulation (PWM) technique.**

A modified hybrid PWM approach that includes a modified modulating signal and a modified carrier signal is presented in this study to address the aforementioned power quality issues. The suggested and current PWM approaches are compared utilizing a variety of modulation index modifications and under various circumstances. For the power quality evaluation a grid-tied, three-phase, three-level T-type neutral point clamped (NPC) inverter is used. Compared to current PWM techniques, the suggested hybrid PWM delivers a lower output line voltage THD of 25.57% and a peak-to-peak dc-link capacitor voltage difference of 11.8 V. Additionally, the suggested hybrid PWM technique offers less thermal stress than current PWM systems by lowering the power switches' switching and conduction losses.

MATLAB/Simulink and PLECS simulation environments are used to compare the suggested hybrid PWM approach with the current one. A smaller-scale prototype created in our research lab is used to further validate the suggested hybrid PWM approach.

Index Terms: **T-type neutral point clamped inverters, multilevel inverters, voltage source inverters, dc-link voltage imbalance, pulse width modulation, and total harmonic distortion.**

INTRODUCTION

Several benefits over two-level voltage source inverters (VSIs) have led to the widespread use of multilevel inverters (MLIs) in medium-to-high voltage applications and renewable solar photovoltaic (PV) systems. This includes reduced EMI, reduced filter size, reduced harmonic distortions, improved output waveform quality, etc. [1],[2].The three main topologies for MLIs are neutral point clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge inverter (CHB)[3],[4],[5]. NPC inverters are among the topologies with some attractive characteristics over alternative topologies, which make them a wise option for solar PV systems that are connected to the grid. These characteristics include improved output voltage and current quality, flexibility, increased efficiency and the capacity to handle voltage. However, under some situations T-type NPC inverters a partial variation of the NPC inverter topology can outperform the NPC inverters in terms of efficiency [6]. Despite being well-established and offering appealing power quality, NPC inverters still have several difficult problems and potential for development. Total harmonic distortion, power loss, thermal stress, and imbalanced neutral point voltage are the main obstacles. The used PWM techniques are crucial to overcoming these obstacles.

Therefore, using a suitable and carefully managed PWM approach may enhance the inverter's ability to balance voltage, reduce power loss, reduce thermal stress, and reduce harmonic distortion. To address these issues, a number of enhanced PWM methods and control algorithms have been put forth in the literature [7], [8], [9], [10], [11], [12], [13], [14], [15], and [16]. In [7], the nested T-type NPC inverter is subjected to a sinusoidal pulse width modulation technique (SPWM) to balance the voltage of the dc-link capacitor. Because of its simplicity, the SPWM technique is thought to be the simplest method for multilayer inverters. However, this technique's high THD, low power loss, and dc-link voltage balancing

performance are significant disadvantages. For NPC inverters, space vector pulse width modulation (SVPWM) is used, and it is contrasted with SPWM in [8]. The data collected demonstrated that, in terms of THD, the SVPWM technique outperforms the SPWM technique. A thorough comparison of the performance of a sinusoidal PWM, a third harmonic injected PWM (THPWM), and a five-level diode clamped inverter is carried out in [9]. In [10], the effectiveness of different medium voltage power converter designs and their control strategies in boosting grid integration efficiency for solar PV power plants is evaluated. In the literature, various PWM techniques—including SPWM, CSVPWM, THPWM, trapezoidal PWM (TRPWM), and sixty-degree PWM (SDPWM)—are compared for performance. Bus clamping PWM is SDPWM based on the discontinuous modulating signal The two most popular and effective PWM approaches for lowering switching loss among BCPWM techniques are sixty-degree and thirty-degree BCPWM. For medium voltage grid-tied converters, [11] examines the third harmonic injected SDBCPWM and TDBCPWM approaches. They were demonstrated to greatly lower switching losses and enhance the converter's output quality. A modified modulating signal-based PWM method is provided in [12] to enhance the power quality of motor driving applications using NPC inverter-based solar PV systems. By producing symmetrical and balanced gate pulses, it was also demonstrated to reduce torque ripple, switching losses, conduction losses, and THD. In [13], a three-level NPC inverter is used for both active shunt filtering and solar PV integration to the distribution grid as part of a new current controller PWM scheme with a neutral point balancing technique. A new step-up switch capacitor-based converter is added to a grid-tied seven stage NPC inverter in order to balance the dc-link capacitor voltages [14]. The system becomes complicated and large due to the need for a separate control mechanism for the new converter. A hybrid PWM approach is put out in [15] by fusing nearest level and space vector PWM. Modulation for an NPC inverter with five levels. The hybrid PWM balances the imbalanced dc-link voltages and provides reduced THD at the fundamental frequency. In [16], a unique single-phase grid-tied five-level NPC converter is proposed using a multicarrier phase disposition PWM approach. It is demonstrated that the suggested converter balances the dc-link split capacitors and enhances the power quality of the grid current. However, this topology's utilization of more power switches than traditional topologies is a significant disadvantage. PWM approaches are suggested in various literature to provide certain benefits with respect to a desired concern [17], [18]. Nevertheless, none of them can address every issue at the same time. A three-level T-type converter is used in [17] to propose a carrier-based discontinuous PWM approach for neutral point potential balancing. Nevertheless, the inverter's THD and power loss are not taken into account. A new PWM technique is presented in [18] to lower the three phase, three level T-type NPC inverters' common mode voltage by roughly 50%. This lowers the inverters' higher voltage stress and leakage current. Nevertheless, compared to other PWM systems now in use, the output voltage's overall harmonic distortion is noticeably larger. Multi carrier PWM, phase shifted PWM, and level shifted PWM are carrier-based PWM techniques that are becoming more and more common in order to enhance the power quality of multilevel converters [19], [20]. Other variations of phase-shifted PWM include alternate phase opposite disposition PWM, phase opposite disposition PWM, and phase disposition PWM. Depending on the application, using various PWM approaches in multilayer converters has certain benefits and drawbacks. For the NPC inverters, a comparison study using these PWM approaches was conducted in [21] and [22]. The term hybrid PWM technique refers to a combination of modulation techniques that can combine their benefits. In order to balance the dc-link voltages and reduce the lower order harmonics for NPC inverters, a hybrid modulation approach that combines selective harmonic mitigation and elimination is provided in [23]. This method's primary challenge is the intricate nonlinear equations that require several approaches to solve. For grid-tied T-type NPC inverters, a hybrid PWM system that combines space vector PWM and selective harmonic elimination PWM is examined in [24]. This method produces a seamless and rapid transition, which is ideal for grid-tied inverter applications. Nevertheless, there is no neutral point voltage balancing system in place. This work proposes a well-balanced hybrid PWM approach that consists of a modified modulating signal and a carrier signal in order to mitigate the aforementioned limitations of multilevel inverters. The following are the primary characteristics of the suggested hybrid PWM technique:

- It lowers the overall harmonic distortion of the inverter's output line voltage
- It enhances the dc-link capacitor's ability to balance voltage by decreasing the voltage differential between peeks
- It lowers the power switches' switching and conduction losses
- It minimizes the overall power loss, which lowers junction temperature and lessens thermal stress Notably, despite the fact that several PWM approaches and control algorithms have been put out in various literatures, they all add complexity to the system and necessitate the use of extra circuits for hardware implementation. On the other hand, altering the modulating and carrier signals is a somewhat simple way to address the important issues with power quality.

Furthermore, it may be implemented on hardware without the need for extra circuitry, and the behavior of the altered signals is known and predictable.

II. TOPOLOGY ADOPTED INVERTER

Fig. 1 shows a grid-tied three-phase 3-L T-type neutral point clamped inverter.

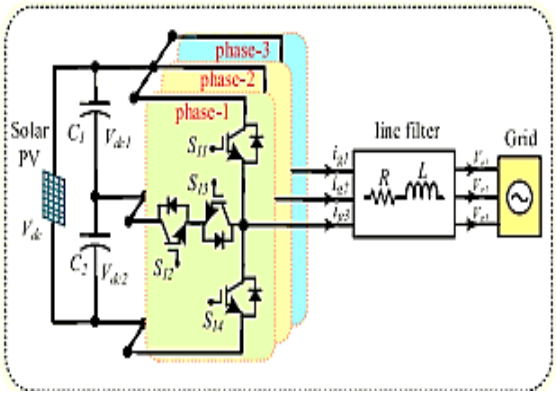

Figure 1: Grid-tied, three-phase, three-level T-type NPC inverter architecture powered by solar PV

Two dc-link capacitors (C1, C2) are employed at the input side of the inverter, which receives its power from a solar PV. The twelve power switches that make up the inverter are S11, S12, S13, S14, S21, S22, S23, S24, S31, S32, S33, and S34. Four power switches are required for per phase. It is definitely forbidden to turn on switch pairs S11, S13, and S12, S14 simultaneously in order to prevent inverter failure because they are known to be each other's opposites. To reduce the harmonics of the current and line voltage, an RL line filter is used to connect the inverter's output side to the grid.

III. STRATEGY FOR CLOSED-LOOP CONTROL

A common grid-connected d_q reference frame-based closed-loop control approach for the chosen inverter architecture, which may provide the grid with both active and reactive power, is shown in Fig. 2. In order to match with the grid voltage reference frame, the three-phase AC current and voltage signals are transformed into D (direct) and Q (quadrature) components, which stand for active and reactive power, respectively. By sensing the grid voltage (V_g) and grid current (ig), respectively, the phase locked loop (PLL) calculates the α and β values with phase angle of the voltage and current. I_d and i_q, which stand for the measured direct and quadrature axis components of the grid current, respectively, can be utilized to independently manage the active and reactive power. The measured errors are then supplied to the PI controller after id and i_q are compared with the reference quantities i^*_d and i^*_q, respectively. Three phase reference signals are created at the output by converting the two reference signals (M_d and M_q) that are collected in the d_q frame to the abc frame. The suggested modulating signal of the hybrid PWM approach is then created by further altering these reference signals.

Section V outlines the suggested modulating signal's creation process. The twelve gate pulses required for the accepted three phase, three level T-types NPC inverter are then generated by comparing the suggested modulating signal and carrier signal.

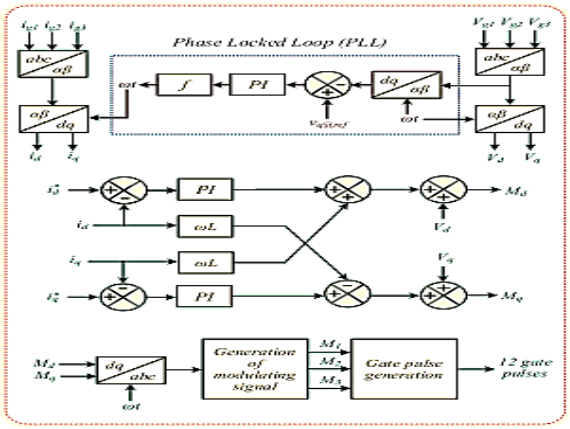

Figure 2: Closed-loop control approach for the selected inverter configuration

IV. DEVELOPMENT OF CURRENT PWM METHODS

Every PWM approach now in use that can be used with MLIs has advantages and disadvantages

depending on how it is used. SPWM [7], CSVPWM [8], THPWM [9], and SDPWM [10] are the most popular PWM approaches utilized with MLIs. The most popular and straightforward PWM method for MLIs is SPWM. THPWM and CSVPWM are well known for enhancing power quality and reducing lower order harmonics. Conversely, as compared to other PWM approaches, the SDPWM technique is highly effective at lowering the switching loss.

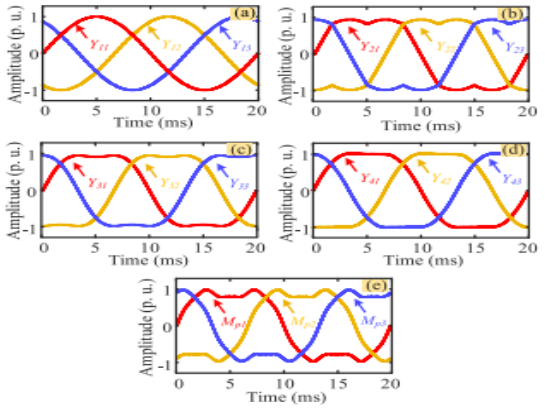

Figure3. Shows the modulating signals for the suggested hybrid PWM approach, SPWM, CSVPWM, THPWM, and SDPWM.

The mathematical formulation of a few well-known PWM schemes is shown in Table 1. Even though these methods provide balanced power quality performance, PWM technique modification allows for even greater performance improvement. This entails altering both the carrier signal and the modulating signal. Figure 3 shows the modulating signals for the suggested improved hybrid PWM technique as well as the current SPWM, CSVPWM, THPWM, and SDPWM techniques.

V.DEVELOPMENTOFTHE PROPOSED HYBRID PWM TECHNIQUE

The core of the suggested hybrid PWM approach consists of the carrier signal and the modified modulating signal. The procedures for creating the suggested modified carrier signal, modulating signal, and gate pulses needed for the power switches are briefly explained in this section.

A. PRODUCING THE SIGNAL MODULATION

Three sinusoidal signals with varying amplitudes and a triangle signal are combined to create the suggested modified modulating signal. Figure 4 shows how the suggested modified modulating signal, Mp, is generated. Initially, three times the fundamental frequency is used to capture a sinusoidal signal (P) so that:

$P = A \sin(3\,\omega\, t)$ ---------- (1)

Where the signal's amplitude is denoted by A and its angular frequency by ω. With the help of the sinusoidal signal (P),

Table 1: Mathematical depiction of several PWM methods

PWM Technique	Mathematical Representation
SPWM [7]	$Y_1 = A\sin(\omega t + \theta)$ $[Y_{11} \quad Y_{12} \quad Y_{13}] = [Y_{1_{\theta=0^\circ}} \quad Y_{1_{\theta=-120^\circ}} \quad Y_{1_{\theta=120^\circ}}]$
CSVPWM [8]	$Y_2 = \frac{2}{\sqrt{3}}\{A\sin(\omega t+\theta)\} - \frac{1}{2}\{\max(Y_{11},Y_{12},Y_{13})\}$ $+\frac{1}{2}\{\min(Y_{11},Y_{12},Y_{13})\}$ $[Y_{21} \quad Y_{22} \quad Y_{23}] = [Y_{2_{\theta=0^\circ}} \quad Y_{2_{\theta=-120^\circ}} \quad Y_{2_{\theta=120^\circ}}]$
THPWM [9]	$Z = cA\sin(\omega t+\theta)$ $Y_3 = A\sin(\omega t+\theta) + Z$ $[Y_{31} \quad Y_{32} \quad Y_{33}] = [Y_{3_{\theta=0^\circ}} \quad Y_{3_{\theta=-120^\circ}} \quad Y_{3_{\theta=120^\circ}}]$
SDPWM [10]	$Y_4 = \frac{2}{\sqrt{3}}[A\sin(\omega t+\theta)] + \frac{1}{2\pi}[A\sin(3\omega t+\theta)]$ $+\frac{1}{60\pi}[A\sin(9\omega t+\theta)] + \frac{1}{180\pi}[A\sin(15\omega t+\theta)]\ldots$ $[Y_{41} \quad Y_{42} \quad Y_{43}] = [Y_{4_{\theta=0^\circ}} \quad Y_{4_{\theta=-120^\circ}} \quad Y_{4_{\theta=120^\circ}}]$

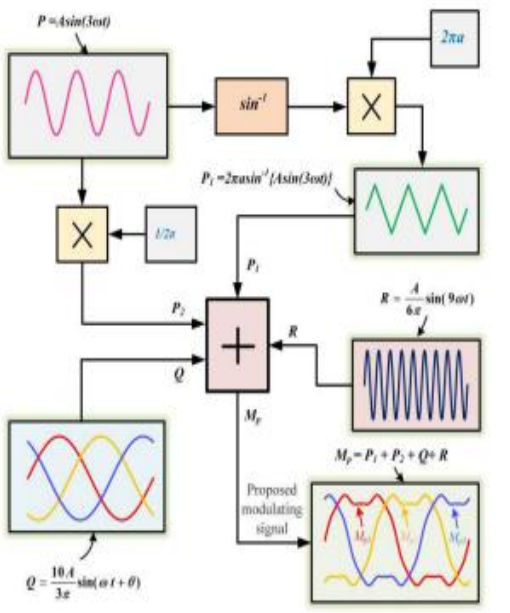

Figure 4: The suggested hybrid PWM technique's modulating signal generating process

The result is a triangle signal (P1), which can be written as follows:

$P_1 = 2\pi a \sin^{-1}\{A \sin(3\omega t)\}$ ---------- (2)

Where the amplitude constant is denoted by a. After that, a different version of the signal (P) is produced in the manner described below:

$P_2 = A/2\pi \sin(3\omega t)$ ---------- (3)

A three-phase sinusoidal signal (Q) is then captured in such a way that:

$Q = 10A/3\pi \sin(\omega t + \theta)$ ---------- (4)

$[Q_1\ Q_2\ Q_3] = [Q_{\theta=0°}\ Q_{\theta=-120°}\ Q_{\theta=120°}]$----------- (5)

Where the signal's phase difference, Q, is defined by θ. Next, a second sinusoidal signal (R) is produced that has a frequency nine times greater than the fundamental, as follows:

$R = A/6\pi \sin(9\omega t)$ ---------- (6)

Finally, the previously built signals P1, P2, Q, and R are added to create the suggested modified modulating signal (MP) as follows:

$Mp = P1 + P2 + Q + R$ ---------- (7)

$[M_{p1}\ M_{p2}\ M_{p3}] = [M_{p\theta=0°}\ M_{p\theta=-120°}\ M_{p\theta=120°}]$ ---------- (8)

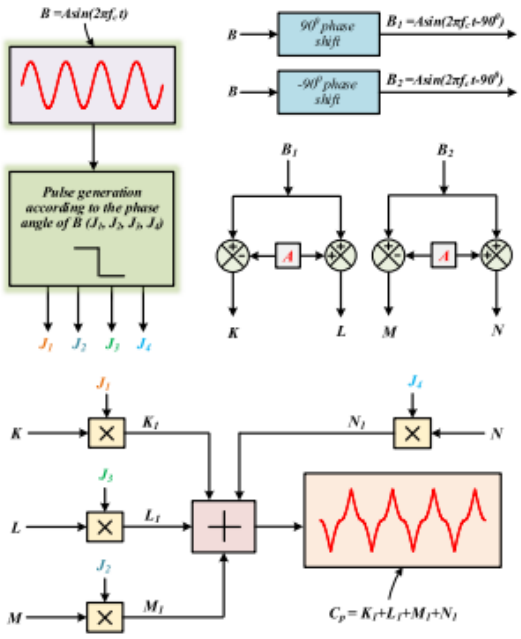

FIGURE 5: The carrier signal generation process of the suggested hybrid PWM approach

B. Creating the signal for the carrier

A sinusoidal signal is used to create the suggested modified carrier signal by making some adjustments to it. Figure 5 shows the suggested carrier signal's development process. In order to create the suggested carrier signal, a sinusoidal signal (B) is first taken into consideration in the manner described below:

$B = A \sin(2\pi fct)$ ---------- (9)

Where, respectively, A and fc stand for the signal's amplitude and carrier frequency. Next, using the sinusoidal signal (B), two intermediate signals (B1 and B2) are created in the manner described below:

$B1 = A \sin(2\pi fct + 90°)$ ---------- (10)

$B2 = A \sin(2\pi fct - 90°)$ ---------- (11)

Now, four pulse signals J1, J2, J3, and J4 are determined from the signal's phase angle (B) as follows:

$$B = \begin{cases} J_1; & if\ 0^0 \le \theta < 90^0 \\ J_2; & if\ 90^0 \le \theta < 180^0 \\ J_3; & if\ 180^0 \le \theta < 270^0 \\ J_4; & if\ 270^0 \le \theta < 360^0 \end{cases}$$ -------- (12)

In this case, θ represents the signal's (B) phase angle. The following is the generation of the four intermediate level shifted signals (K, L, M, and N):

$K = B_1 - A$ ---------- (13)

$L = B_1 + A$ ---------- (14)

$M = B_2 - A$ ---------- (15)

$N = B_2 + A$ ---------- (16)

The signals K1, L1, M1, and N1 are then created by multiplying the newly created level shifted signals (K, L, M, and N) by the previously created pulse signals (J1, J3, J2, J4).

$K_1 = KJ_1$ ---------- (17)

$L_1 = LJ_3$ ---------- (18)

$M1 = MJ_2$ ---------- (19)

$N1 = NJ4$ ---------- (20)

Lastly, the suggested carrier signal, Cp, of the hybrid PWM approach is created by adding the discrete signals (K1, L1, M1, and N1) together.

$Cp = K1 + L1 + M1 + N1$ -------- (21)

C. CREATING THE PULSES OR GATE

The suggested hybrid PWM approach is made up of the modulating signal from Figure 4 and signal from Figure Fig. 6 shows the block diagram depiction of the gate pulse generation process using the suggested modified hybrid PWM technique. The suggested modulating signal and the suggested carrier signal are compared in order to produce the gate pulses for the IGBTs. Two carrier signals (Carrier1 and Carrier2) are required for S_{11}, S_{12}, S_{13}, and S_{14}, respectively, in order to generate a three level output for each phase. Fig. 7 shows the gate pulse generation for IGBTs (S_{11}, S_{12}, S_{13}, and S_{14}) for a carrier signal of 0.8 kHz. The IGBT S_{11} is activated when the amplitude of Carrier1 is less than Mp1. If not, the IGBT S_{11} is not in use. Likewise, the IGBT S_{12} is activated when the amplitude of Carrier2 is less than M_{p1}.

Table 2 shows the IGBTs' switching states for a single phase.

State	S_{11}	S_{12}	S_{13}	S_{14}	Output
P	ON	ON	OFF	OFF	$V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{dc}/2$

The corresponding IGBTs for S11 and S12 are S13 and S14, respectively. This implies that when S11 and S12 are switched on, S13 and S14 must be turned off. Table 2 lists the IGBTs' switching states for a single phase. Positive, neutral, and negative states are denoted by the letters P, O, and N, respectively.

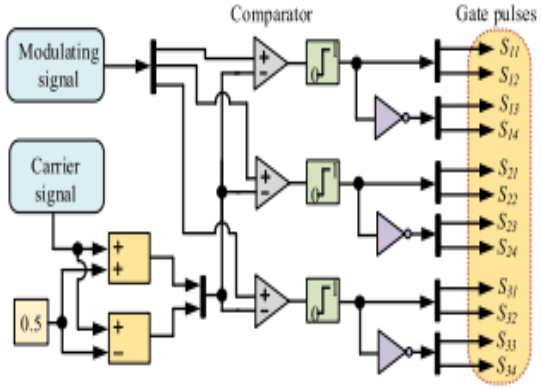

Figure 6 shows how the chosen topology generates gate pulses.

D. THE PROPOSED HYBRID PWM TECHNIQUE'S MOTIVATION AND FINDING PROCEDURE

The primary driving forces behind the suggested improved PWM methodology are the drawbacks of the current PWM methods, which include excessive THD, power loss that causes thermal stress, and issues with capacitor voltage balancing. The gate pulses used to switch the power semiconductor switches are what mitigate THD, power loss, and capacitor voltage balancing issues. In contrast to the gate pulses of current PWM approaches, which guarantee reduced THD, power loss, and balanced capacitor voltages, the gate pulses produced by the suggested improved PWM technique are symmetric and balanced. Only when the suggested modified carrier and modulating signal are used in tandem can these gating signals be produced. When creating the gating signals for the NPC inverter, a series of systematic steps are used to generate the suggested hybrid PWM methodology. The PWM technique's main component, the gate pulse generating process, greatly regulates all performance factors, including THD, power losses, heat distribution, and capacitor voltage balancing issues.

Figure 7 shows how the suggested hybrid PWM approach generates gate pulses for a single phase Figure 7 shows how the suggested hybrid PWM approach generates gate pulses for a single Figure 7 shows how the suggested hybrid PWM approach generates gate pulses for a single phase

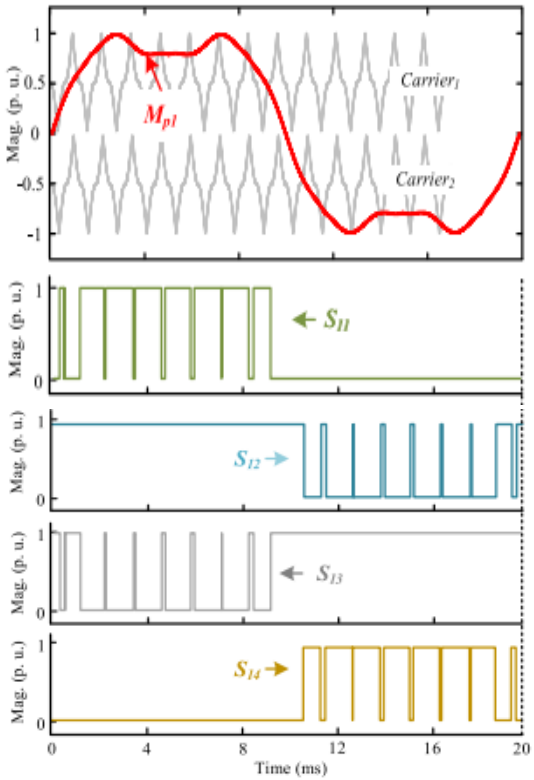

Figure 7 shows how the suggested hybrid PWM approach generates gate pulses for a single phase.

The MLIs' overall enhanced performance is a result of optimized and balanced gate pulses. Therefore, the pulse sequences under the conventional PWM technique are initially examined in order to produce the enhanced modified modulating and the carrier signals. Table 3 shows the charging patterns of the dc-link capacitors using the SPWM approach as well as the examined gate pulse sequences for the six IGBTSs (S_{11}, S_{12}, S_{21}, S_{22}, S_{31}, and S_{32}). Since SPWM is the most straightforward modulation scheme among the conventional techniques, it is used here. In this instance, a low frequency carrier signal (about 50 Hz) is employed to make it simple to see the IGBTs' switching states. The opposites of SX3 and SX4, respectively, are SX1 and SX2. Therefore, it is adequate to analyze just two IGBTs from each inverter leg. This means that 720 likely switching sequences and six IGBTs need to be examined. Nonetheless, a few frequent and recurring switching sequences are examined in this instance. It is evident from the switching sequences that certain

sequences—1, 3, 5, 7, 10, and 13—are in charge of maintaining the capacitor voltages at a steady level. It may be possible to reduce the dc-link capacitor voltage fluctuation problem by repeating these steps. The suggested carrier signal is created using the procedure shown in Fig. 5 following the analysis of the pulse sequences. The suggested carrier signal's structure facilitates the supporting switch's on/off sequence. The suggested modulating signal, shown in Fig. 4, must then be developed. In this instance, the generation concept is borrowed from earlier works in which the creation of THPWM and SDPWM procedures mirrored the construction of modulating signals by adding a few odd harmonic signals.

TABLE 3. Examining how the capacitor voltages behave under various switching configurations

Switching sequence	Switching states of the IGBTs						Behavior of the capacitor voltages: charging (↑), discharging (↓), constant (–)	
	S_{11}	S_{12}	S_{21}	S_{22}	S_{31}	S_{32}	V_{C1}	V_{C2}
1	OFF	ON	OFF	OFF	ON	ON	–	–
2	ON	ON	OFF	OFF	OFF	ON	↑	↓
3	ON	ON	OFF	OFF	OFF	OFF	–	–
4	OFF	ON	OFF	ON	OFF	OFF	↑	↓
5	OFF	ON	ON	ON	OFF	OFF	–	–
6	OFF	OFF	ON	ON	OFF	ON	↓	↑
7	OFF	OFF	ON	ON	ON	ON	–	–
8	OFF	OFF	OFF	ON	ON	ON	↑	↓
9	OFF	ON	OFF	ON	ON	ON	↓	↑
10	ON	ON	OFF	OFF	ON	ON	–	–
11	ON	ON	OFF	OFF	OFF	ON	↑	↓
12	ON	ON	OFF	ON	OFF	OFF	↓	↑
13	OFF	OFF	ON	ON	OFF	OFF	–	–

The suggested PWM technique's harmonic signal amplitude constant is extremely sensitive since it has a direct impact on the IGBTs' gate pulse pattern.

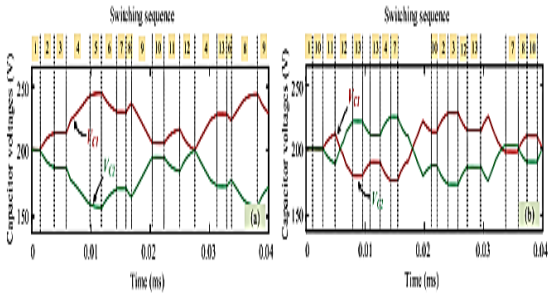

Figure 8: DC-link capacitor voltage response for various switching sequences using (a) SPWM and (b) the suggested hybrid PWM methods

There is a possibility that the amplitude will surpass the specified value A as additional odd harmonic signals with various frequency are introduced. The modulating signal's amplitude is the primary factor in this situation, and it is changed as follows to guarantee an intermediate flattened top signal that may produce symmetric and balanced gating signals:

Amp. of $M_P \leq$ Amp. of P_1 + Amp. of P_2 + Amp. of Q + Amp. of R ---------- (21)

Where P_1, P_2, Q, and R are the intermediate signals, respectively, as previously mentioned, and MP is the suggested modulating signal. The amplitude of M_P is unquestionably less than A at phase angles of 0, 180, and 360, however it is represented as follows at phase angles of 90 and 270:

$$\begin{aligned} &Amp.\ of\ M_P \\ &= \pm\left\{A\left(\frac{10}{3\pi} - 2\pi a - \frac{1}{2\pi} + \frac{1}{6\pi}\right)\right\} \\ &= \pm\left\{A\left(\frac{10}{3\pi} - 0.02\pi - \frac{1}{2\pi} + \frac{1}{6\pi}\right)\right\} \quad [a = 0.01] \\ &= \pm 0.892A \end{aligned}$$

MP's amplitude is smaller than A's. The amplitude constants are chosen so that the defined amplitude A is precisely matched by the maximum amplitude of M_P, which is obtained between 0◦ and 90◦ phase angle. Figures 8(a) and 8(b) show the response of the dc-link capacitor voltages for various switching sequences under SPWM and the suggested hybrid PWM approach, respectively. High dc-link voltage fluctuation results from the SPWM technique's repetition of constant voltage sequences after two or more sequences, which provides the capacitors more opportunity to charge or discharge. Therefore, the capacitor voltage difference will be reduced if the constant sequences may be repeated after each charge or discharge sequence.

VI. COMPARISON AND ANALYSIS OF PERFORMANCE

The findings of simulations and experiments are used to compare the performance of the suggested modified hybrid PWM technique with the current PWM techniques in terms of THD, capacitor voltage balance, power loss, and thermal stress.

A.SIMULATION RESULTS

Figure 9(a) and Figure 9(b) show the output line voltage (unfiltered) and the output line voltage's harmonic spectrum under the suggested improved hybrid PWM approach, respectively. The unfiltered THD of the inverter line voltage is 25.57%. Figure 9(c) and Figure 9(d) show the three-phase grid current and its harmonic spectrum under the suggested hybrid PWM, respectively. Since THD must be less than 5% in accordance with IEEE-519, the reported grid current THD of 1.12% is acceptable. Figures 10(a), 10(b), 10(c), 10(d), and 10(e) show the peak-to-peak dc-link capacitor voltage difference

under the current SPWM, CSVPWM, THPWM, and SDPWM approaches as well as the suggested hybrid PWM technique. The peak-to-peak capacitor voltage difference under SPWM, CSVPWM, THPWM, SDPWM, and the suggested hybrid PWM approach is 16.9 V, 1.8 V, 5.7 V, and 8.8 V smaller than that of the current PWM techniques, respectively, as shown in Fig. 10. Accordingly, in terms of capacitor voltage balancing performance, the suggested hybrid PWM technique outperforms the current SPWM, CSVPWM, THPWM, and SDPWM, which are 28.7 V, 13.6 V, 17.5 V, 20.6 V, and 11.8 V, respectively. The SPWM technique records the largest peak-to-peak capacitor voltage difference, whereas the suggested hybrid PWM technique records the smallest. Figure 10 makes it clear that the suggested hybrid PWM technique reduces the peak-to-peak capacitor voltage difference by 16.9 V, 1.8 V, 5.7 V, and 8.8 V, respectively, compared to the current PWM strategies. In terms of capacitor voltage balancing performance, the suggested hybrid PWM technique outperforms the current SPWM, CSVPWM, THPWM, and SDPWM, respectively. Unfiltered THD of the inverter output line voltage provided by the suggested hybrid PWM approach and the current PWM techniques, respectively, against modulation index variation (0.6~1.4), was displayed in the bar graph of Fig. 11(a). Likewise, Fig. 11(b) shows the peak-to-peak dc-link capacitor voltage difference produced by the suggested hybrid PWM technique and the current PWM techniques against modulation index variation (0.6~1.4).

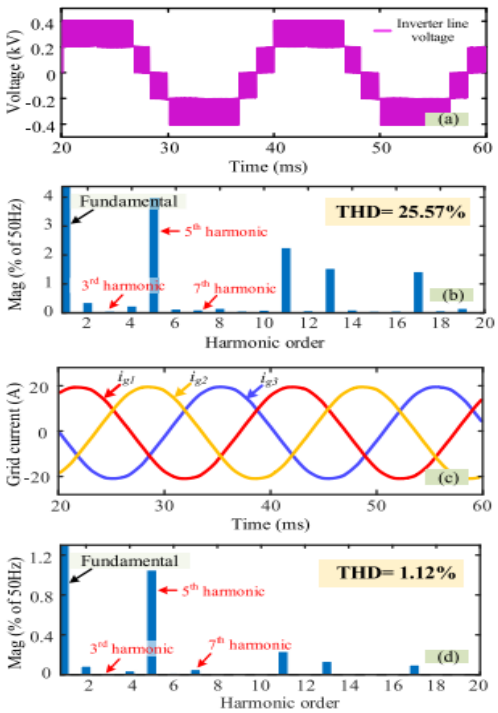

Figure 9 shows the grid current (c), inverter output line voltage (b), and grid current total harmonic distortion (THD) spectrum under the suggested hybrid PWM approach.

Table 4 shows a comprehensive breakdown of the peak-to-peak dc link voltage difference and the inverter output line voltage THD (unfiltered) between the suggested hybrid PWM technique and the current PWM techniques. The suggested hybrid PWM technique's THD of the inverter output line voltage against the modulation index 0.6, 0.8, 1, 1.2 and 1.4 are 43.42%, 34.01%, 25.57%, 21.56% and 21.22%, respectively.

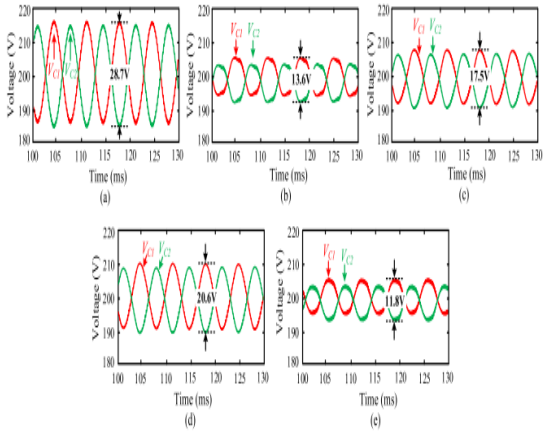

Figure 10: Difference in voltage across a dc-link capacitor under SPWM, CSVPWM, THPWM, SDPWM, and the suggested hybrid PWM approaches.

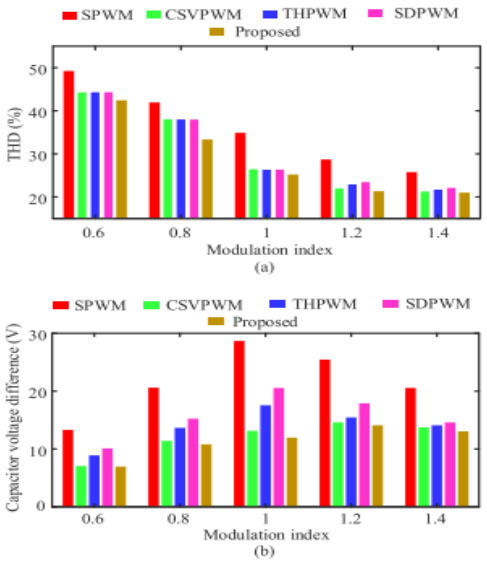

Figure 11 shows a comparison of the suggested hybrid PWM approaches, SPWM, CSVPWM, THPWM, and SDPWM, against modulation index variation in terms of (a) inverter output line voltage THD and (b) gap in capacitor voltage.

43.42%, 34.01%, 25.57%, 21.56%, and 21.22%, in that order, is less than the current SPWM, CSVPWM, THPWM, and SDPWM methods. Compared to the current PWM methods, the suggested hybrid PWM provides 9.32%, 1.05%, 0.94%, and 0.97% lower inverter output line voltage THD at modulation index 1. fortunately the suggested hybrid PWM technique achieves a smaller peak-to-peak capacitor voltage difference than the current PWM techniques, with values of 7.1 V, 10.4 V, 11.8 V, 13.7 V, and 13.1 V, respectively, against modulation indexes of 0.6, 0.8, 1, 1.2, and 1.4. In comparison to the current SPWM, CSVPWM, THPWM, and SDPWM techniques, the suggested hybrid PWM methodology provides 6.6 V, 0.2 V, 2.1 V, and 3 V less capacitor voltage difference, respectively, when the modulation index is 0.6. The suggested hybrid PWM reduces the capacitor voltage differential by 10.1 V, 0.8 V, 3.4 V, and 4.9 V for modulation index 0.8, respectively, compared to the current PWM methods. Similarly, Table 4 makes it evident that the suggested hybrid PWM technique produces a smaller capacitor voltage differential for modulation index 1, 1.2, and 1.4, respectively, than the current PWM strategies. Figure 12 shows a sketch of the power loss and thermal distribution of the suggested hybrid PWM approach for the phase-1 IGBTs (S11, S12, S13, and S14). Infineon Technologies' IKW50N65F5 IGBT and diode are used in PLECS simulation software to compute the power loss and junction temperature of the IGBTs.

To determine the power loss and junction temperature, the characteristic curve from the chosen model is inserted into the PLECS block set. The power losses of S11, S12, S13, and S14 are 42.25 W, 1.94 W, 1.94 W, and 42.25 W, respectively, which represent 48%, 2%, 2%, and 48% of the phase-1 total power loss, as shown in Fig. 12(a). Therefore, the outer switches (S11 and S14) use higher power loss for each phase than the inner switches (S12 and S13), per se. Conversely, Fig. 12(b) shows the junction temperature of the IGBTs (S11, S12, S13, and S14) for two operation cycles.

TABLE 4. Peak-to-peak capacitor voltage variation and THD for various PWM schemes in relation to modulation index variation.

PWM technique	THD (%) of inverter output line voltage (unfiltered) with the variation of modulation indices (0.6-1.4)					Capacitor voltage difference (V) with the variation of modulation indices (0.6-1.4)				
	0.6	0.8	1	1.2	1.4	0.6	0.8	1	1.2	1.4
SPWM [7]	49.25	41.95	34.89	28.71	25.77	13.7	20.5	28.7	25.4	20.7
CSVPWM [8]	44.46	38.22	26.62	22.15	21.47	7.3	11.2	13.6	14.6	13.5
THPWM [9]	44.49	38.19	26.51	23.11	21.89	9.2	13.8	17.5	15.3	14.1
SDPWM [10]	44.5	38.17	26.54	23.64	22.31	10.1	15.3	20.6	17.8	14.6
Proposed	43.42	34.01	25.57	21.56	21.22	7.1	10.4	11.8	13.7	13.1

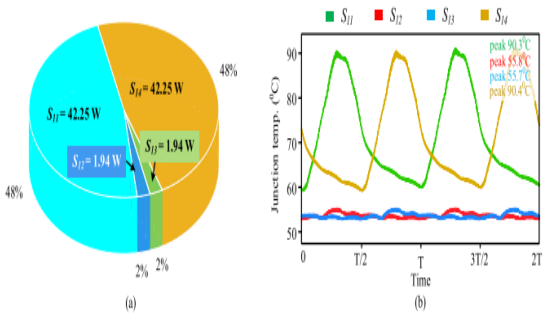

Figure 12 shows the suggested hybrid PWM approach for IGBTs (S11, S12, S13, S14) in terms of (a) power loss and (b) heat distribution.

PLECS simulation program uses the IKW50N65F5 IGBT and diode from Infineon Technologies to calculate the power loss and junction temperature of the IGBTs. To determine the power loss and junction temperature, the characteristic curve from the chosen model is inserted into the PLECS block set. The power losses of S_{11}, S_{12}, S_{13}, and S_{14} are 42.25 W, 1.94 W, 1.94 W, and 42.25 W, respectively, which represent 48%, 2%, 2%, and 48% of the phase-1 total power loss, as shown in Fig. 12(a). As a result, the outer switches (S_{11} and S_{14}) lose more power for each phase than each of the inner switches (S_{12} and S_{13}). Conversely, Fig. 12(b) shows the junction temperature of the IGBTs (S_{11}, S_{12}, S_{13}, and S_{14}) for two operation cycles. Phase 1 IGBTs (S_{11}, S_{12}, S_{13}, and S_{14}) experience peak temperatures of 90.3◦, 55.8◦, 55.7◦, and 90.4◦, in that order. As shown in Fig. 12(b), the outer switches (S_{11} and S_{14}) experience higher junction temperatures and thermal stress than the inner switches (S_{12} and S_{13}), respectively. Conduction loss (CL) and switching loss (SL) are thought to be the inverter's two main power losses. Figure 13-15 uses a 3D graph to illustrate the switching loss (SL), conduction loss (CL), and total power loss (TL) between SPWM, CSVPWM, THPWM, SDPWM, and the suggested hybrid PWM approaches versus modulation index variation (0.6~1).

High power loss results from the inverter operating at a high power rating when the modulation index is close to 1. For modulation indices 0.6, 0.7, 0.8, 0.9, and 1, the suggested hybrid PWM approach has a total power loss (TL) of 191.6 W, 223.1 W, 240.1 W, 259.4 W, and 278.3 W, respectively. This is less than the other SPWM, CSVPWM, THPWM, and SDPWM systems now in use. As illustrated in Figs. 13–15, the suggested hybrid PWM technique outperforms the SPWM technique by 10.87% in

terms of switching loss (SL), 2.69% in terms of conduction loss (CL), and 3.6% in terms of total loss (TL). In a similar vein, the suggested hybrid PWM technique outperforms both CSVPWM and THPWM strategies by about 2.73% in terms of overall loss.

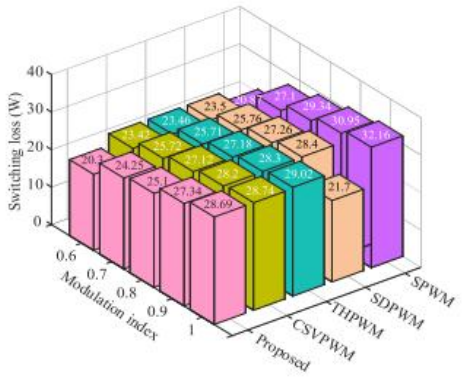

FIGURE 13. Comparing switching losses across several PWM methods in relation to modulation index variation.

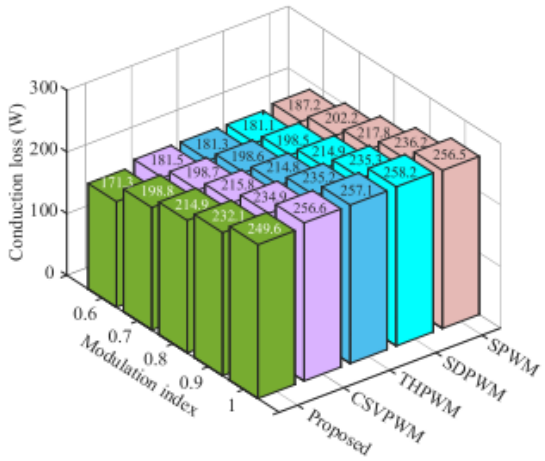

Figure 14 compares the conduction losses of several PWM approaches in relation to variations in the modulation index.

In contrast, the suggested hybrid PWM outperforms the SDPWM technique for modulation index 1 by 24.4% in terms of switching loss (SL), 3.33% in terms of conduction loss (CL), and 0.57% in terms of total loss (TL). The SDPWM technique is thought to be the most effective way to lower the inverter's switching loss [11]. Therefore, when modulation index 1 is used, switching loss is significantly lower in the SDPWM technique than in the suggested hybrid PWM technique. Nonetheless, the suggested hybrid PWM approach exhibits superior switching loss (SL) results as the modulation index decreases. Therefore, it is certain that the suggested hybrid PWM technique will perform better than the current SPWM, CSVPWM, THPWM, and SDPWM strategies, respectively. Figures 16 and 17 show the close-loop reference current responses for active and reactive power under the suggested hybrid PWM approach, respectively. Figure 16(a), Figure 16(b), and Figure 16(c) show the voltage and current waveforms for unity, lagging, and leading power factor, respectively. Only resistive load is applied when the power factor is at unity (3.25 kW, i^*_d = -20 A, i^*_q = 0 A), This maintains the current and voltage in the same phase. A capacitive load is applied at the leading power factor (3.25 kVAR, i^*_d = 0 A, i^*_q = -20 A). Where current leads the voltage by 90◦.Conversely, an inductive load with a voltage lead current of 90◦(3.25 KVAR, i^*_d = 0 A, i^*_q = 20 A) is applied at lagging power factor Figure17.llustrates the step reactions of the inverter when active and reactive power are applied using the suggested hybrid PWM approach. There are two step shifts at 60 and 120 ms, respectively. First, the grid receives reactive power. There is no phase difference between the grid voltage and grid current; instead, the grid current follows the reference grid current (20 A).

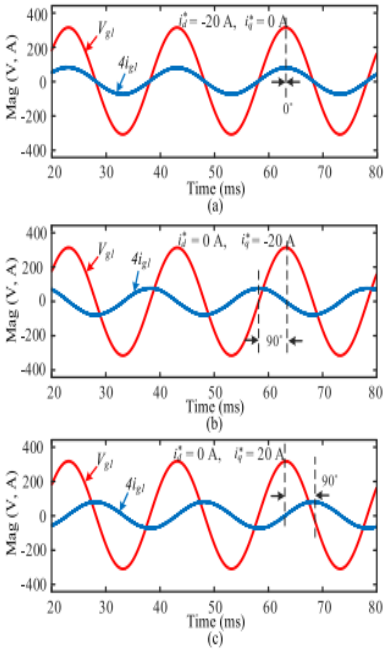

Figure 16 shows the waveforms of grid voltage and current at (a) unity, (b) leading, and (c) lagging power factor.

The first step shift occurs at 60 ms when reactive electricity is applied to the grid via an inductive load. As a result of applying both active and reactive power simultaneously, the grid current changed to 28.26 A, as was to be expected. The second step shift occurs at 120 ms when reactive power is applied to the grid via a capacitive load. With the same amount of active

and reactive power applied, the grid current this time changed to 28.26 A. d. As seen in Fig. 17(a), following the second step shift, the grid current is 45◦ ahead of the grid voltage. As can be observed in Fig. 17(b), the controller tracks the reference grid current for the step changes within 2ms.

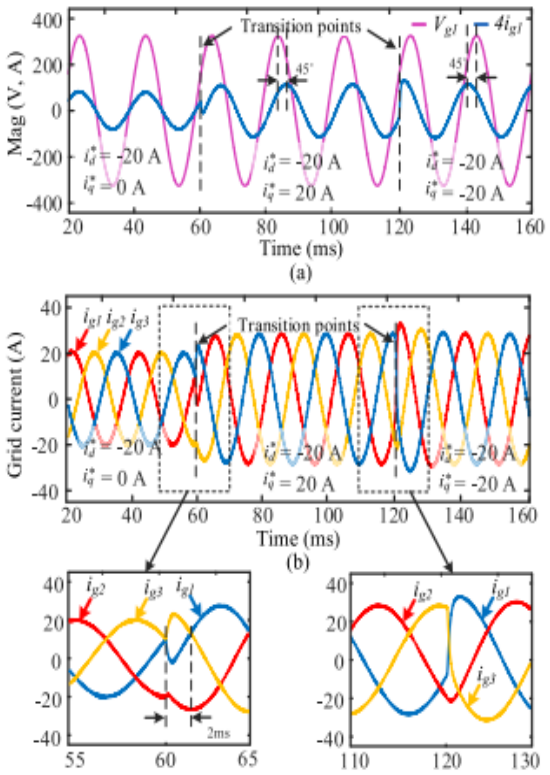

Figure 17. Step responses of the inverter when active and reactive power are applied using the suggested PWM technique (a) single phase grid voltage and current (b) three phase grid current.

VII. CONCLUSION

In this study, a hybrid PWM approach that combines a modified modulating signal and a modified carrier signal is proposed to enhance the grid-tied T-type NPC inverter's performance. The suggested modified hybrid PWM technique offers a peak-to-peak dc-link capacitor voltage difference of 11.8 V and an unfiltered output line voltage THD of 25.57%, respectively, which are lower than the current SPWM, CSVPWM, THPWM, and SDPWM techniques. Additionally, the suggested hybrid PWM technique has a total power loss of 278.3 W, which is an improvement over the current SPWM, CSVPWM, THPWM, and SDPWM strategies by 3.6%, 2.73%, 2.74%, and 0.57%, respectively. Thus, by reducing the junction temperature produced by power loss, the suggested hybrid PWM approach can lessen the thermal stress of the power switches. According to an experimental laboratory prototype, the overall harmonic distortion of the output line voltage and the dc-link capacitor voltage difference produced under the suggested improved hybrid PWM technique are 28.29% and 17.2 V, respectively, which strongly support the simulation results. Lastly, it can be concluded that the suggested hybrid PWM technique outperforms other PWM techniques already in use in the field of solar PV supplied grid-tied applications due to the good agreement between simulation and experimental results.

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