Design And Performance Analysis of Voltage Controlled Oscillator

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***Abstract*—This paper presents the design and performance analysis of a CMOS Voltage-Controlled Oscillator (VCO) implemented using Cadence Virtuoso with the GPDK 90nm technology node. The VCO is a critical component in phase - locked loops (PLLs), and RF communication systems, requiring high- frequency stability and. In this work LC-Cross coupled VCO was employed to achieve compact design. The fundamental operation of VCO involves converting the input voltage into a corresponding frequency output allowing the dynamic frequency adjustments based on control voltage. The analysis focuses on optimizing the VCO's parameters to achieve desired metrics, such as Stability, Linearity while ensuring minimal power consumption. The results validate the effectiveness of the GPDK 90nm process for high-frequency analog design and establish a baseline for future optimizations in VCO architectures.**

***Index Terms*—CMOS, CADENCE VIRTUOSO, LINEARITY POWER CONSUMPTION, STABILITY and VCO.**

I. INTRODUCTION

In the rapidly evolving field of integrated circuit (IC) design, a comprehensive understanding of semiconductor processes and devices is essential, particularly in analog and mixed-signal domains, where close interaction among process, device, and circuit levels significantly influences overall performance. In digital circuits, MOS transistors are commonly treated as simple switches; however, in analog designs, a deeper understanding of their behavior is critical due to their multiple roles as amplifiers, capacitors, and switches [1], [2]. This necessitates careful consideration of second-order effects, particularly in advanced nanometer-scale technologies where short-channel effects, leakage currents, and threshold voltage variations increasingly affect circuit functionality [3].

As CMOS scaling continues, variability in device parameters due to manufacturing tolerances and environmental fluctuations—such as temperature and supply voltage changes—has become a major challenge in ensuring reliable circuit performance. In highly integrated systems, increased device density also results in significant parasitic coupling, leading to interference and degradation of analog signal quality, [5]. Among the most critical components in such systems is the voltage-controlled oscillator (VCO), which is essential in phase-locked loops (PLLs), frequency synthesizers, and clock/data recovery systems [1], [6]. The performance of a VCO is defined by its tuning range, gain (Kvco), phase noise, linearity, and power consumption, all of which must be carefully optimized based on the target application. VCOs are generally categorized into two primary topologies: LC VCOs and ring oscillators. LC-based designs provide superior phase noise performance owing to high-Q resonant tanks but require larger area and higher power, whereas ring VCOs are compact and energy-efficient, albeit at the cost of greater phase noise and limited tuning linearity.

Numerous techniques have been proposed to enhance the noise performance and tuning characteristics of VCOs. For example, the gm/ID methodology has been successfully applied to design low-phase-noise LC VCOs in nanoscale CMOS [3]. Theoretical models such as those developed by Hajimiri and Lee [4], along with studies on monolithic CMOS implementations [5], have contributed significantly to our understanding of phase noise behavior and optimal topology selection. Advanced solutions, including digitally controlled oscillators for millimeter-wave applications and machine learning-based VCO optimization [9], further highlight the ongoing innovation in this domain.

This paper presents the design and comparative analysis of multiple VCO topologies using 90nm CMOS technology. Simulations are carried out in LTSpice to assess performance metrics such as frequency tuning, power efficiency, and phase noise. The impact of biasing schemes, transistor sizing, and parasitic elements is thoroughly analyzed to identify the most suitable topology for integration into modern, high-performance analog and RF systems.

II. DESIGN PROCEDURE

The methodology for designing the LC cross-coupled VCO begins with defining key design specifications, including the target frequency range, tuning bandwidth, phase noise requirements, and power consumption constraints. Using these specifications, initial component values for the LC tank circuit—comprising on-chip spiral inductors and varactor diodes—are calculated to set the desired oscillation frequency. A cross-coupled NMOS transistor pair is selected to provide the required negative resistance to sustain oscillations, and a constant current source is used for biasing. The schematic is developed in Cadence Virtuoso using the chosen technology PDK, and the design is initially verified through DC and transient simulations to ensure proper startup and oscillation. Frequency tuning is evaluated by sweeping the varactor control voltage. Periodic steady-state (PSS) and phase noise (PNOISE) simulations are performed to analyze the oscillator's phase noise characteristics. Once the schematic meets performance goals, the layout is created with attention to symmetry, parasitic minimization, and noise isolation. Parasitic extraction is carried out, followed by post-layout simulations to validate performance under realistic conditions. Finally, the design undergoes DRC and LVS checks to ensure manufacturability and correctness.

Table 1: Component Specification

Supply voltage	1.8 V
Bias current	1 mA
PMOS	W= 320nm, l=200nm
NMOS	W=160nm, l=100nm
LC tank	L= 100pH, C= 50fF
Load capacitance	180 fF

III. IMPLEMENTED DESIGN

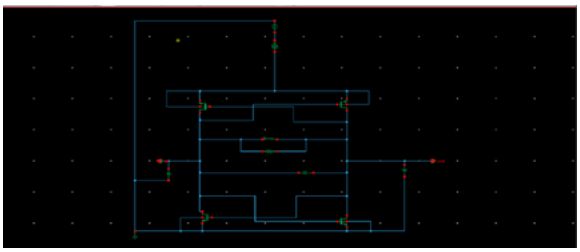

Fig 1. LC-VCO Schematic

The schematic shown is a differential LC Voltage-Controlled Oscillator (VCO) circuit designed using CMOS technology in Cadence Virtuoso. The core of the oscillator comprises a cross-coupled pair of NMOS transistors at the bottom and a cross-coupled pair of PMOS transistors at the top, forming a positive feedback loop essential for sustaining oscillations. The LC tank circuit is formed by two inductors and capacitors placed between the cross-coupled nodes, determining the oscillation frequency based on the resonance of the LC network. Biasing is provided through a current source (Ibias) from the top, ensuring controlled current flow through the circuit. The gates of the cross-coupled NMOS transistors are driven by differential inputs, and the output is taken differentially from the drain nodes of the cross-coupled pairs. This topology is commonly used for its symmetry and good phase noise performance. The schematic also shows parameterized MOSFET devices (with specified widths, lengths, and multiplicities) and tuning capacitors, likely used to enable frequency tuning via varactors or external control voltage (Vctrl). This makes it suitable for use in RF applications like PLLs and communication systems.

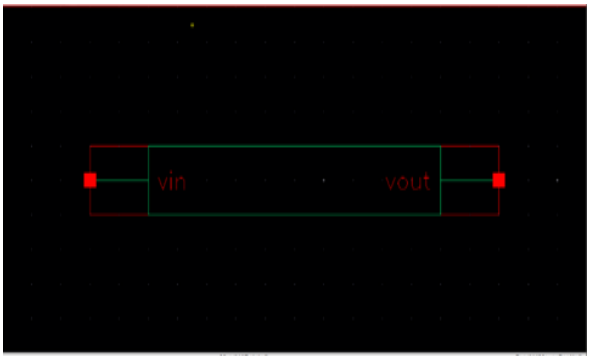

Fig 2. LC-VCO Symbol

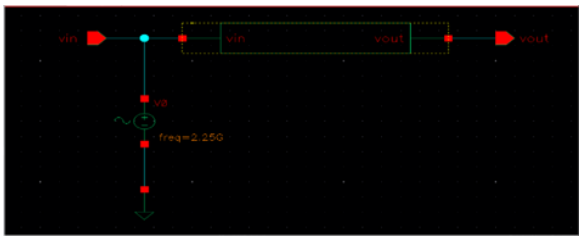

Fig 3. Schematic testbench

IV. RESULTS AND DISCUSSIONS

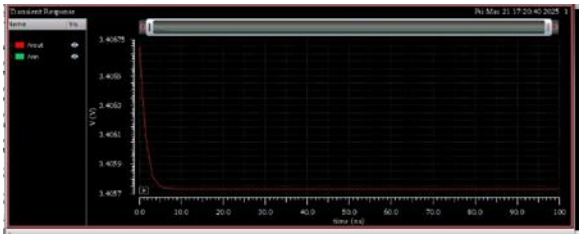

Fig 4. Transient Analysis

The simulation output shown above is the transient response of the VCO circuit in Cadence Virtuoso. The graph displays the voltages at the input (/vin) and output (/vout) over a 100 ns time window. Both signals appear flat and settle quickly, indicating no sustained oscillation is occurring. The output voltage (/vout) drops slightly and stabilizes around 3.4057 V, showing transient behavior.

Fig 5. Frequency Output

The frequency output plot in the above figure shows a VCO oscillating at approximately 37.37 GHz, as indicated by the simulation marker. This corresponds to the expected operation within the reported tuning range of 30.5 GHz to 40.4 GHz. The result confirms that the oscillator not only starts up properly but also reaches the desired operating frequency. This validates the design's suitability for high-frequency, wideband RF systems.

V. CONCLUSION

In this project, a successful LC Cross-Coupled Voltage-Controlled Oscillator (VCO) was designed, implemented, and simulated using Cadence Virtuoso with the 90nm GPDK technology. The circuit utilized a differential cross-coupled NMOS structure with an on-chip spiral inductor and accumulation-mode MOS varactors to achieve high oscillation frequency tunability and low phase noise.Through carrying out extensive simulations, significant performance parameters such as oscillation frequency, tuning range, output swing, power consumption were compared. Cross-coupled architecture proved useful in producing sufficient negative resistance to serve tank losses, thus providing continuous oscillations with improved startup margins. 90nm process technology provided a best compromise among speed, area, and power consumption and therefore the design can be adapted in modern wireless communication systems.

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