Phase Noise Analysis of Seperately Driven Ring Oscillator

Dr. A.Vikas[1], P. Ashwini[2] M. Venu[3], M. Vamshi[4]
[1]*Associate professor, Dept of ECE, TKR College of Engineering and Technology*
[2,3,4] *Student, Dept of ECE, TKR College of Engineering and Technology*

Abstract **– This is about the design and simulation of a 3-stage ring oscillator in Cadence Virtuoso at 180 nm technology. The emphasis is on phase noise analysis under different conditions such as temperature, noise figure, and operating frequency. The oscillator is very important in PLLs and data recovery in serial communication. It employs high-performance inverters in a feedback loop. Layout is generated after implementation with Assura, and more stages in increasing the number of stages decrease phase noise. Transient, DC, and phase noise analysis are performed to analyze frequency response and performance.**

Index terms **– SDRO, phase noise analysis, cadence virtuoso, inverter.**

I. INTRODUCTION

Ring oscillators are basic building blocks in contemporary integrated circuits, found extensively in applications like clock generation, frequency synthesis, and signal modulation. Their simplicity, scalability, and CMOS technology compatibility make them well-suited for high-speed and low-power designs [2]. Nevertheless, phase noise—a quantification of the short-term frequency stability of an oscillator—is still a key issue, particularly in communication systems where spectral purity is essential [1][3][5][11].

In traditional ring oscillators, phase noise is affected by thermal noise, power supply noise, and inherent device noise, all of which impair performance [9]. To minimize these effects and increase control over oscillator behavior, separately driven ring oscillators have been suggested. This topology includes independent control over the drive signals of the oscillator stages, providing increased flexibility in tuning and the possibility of decreased phase noise.
This research is centered on the analysis of phase noise in a separately driven ring oscillator. The objective is to know how independent driving mechanisms influence the noise features of the oscillator and to assess design methods that maximize phase noise performance. By theoretical modeling, simulation, and comparative analysis, the research endeavours to contribute insights to the design of low-noise ring oscillators for next-generation electronic systems [4].

II. PROPOSED SYSTEM

The methodology for phase noise analysis of a separately driven ring oscillator is proposed to be a systematic process that combines theoretical modeling, circuit simulation, and performance assessment [8]. First, a conventional ring oscillator and a separately driven ring oscillator will be designed using standard CMOS technology. The standard design will contain equal drive across all stages, whereas the individual control or biasing for every stage of oscillators will be included in separately driven design. The designs will be simulated within a circuit simulator platform like Cadence Virtuoso or LTspice.

Subsequently, an analytical phase noise model shall be formulated with reference to modified Leeson's equation, and major noise contributors like thermal noise, flicker noise, and supply noise shall be included within it. The model will take into account the impact of separate stage driving on noise contribution and propagation. Subsequently, simulations will be performed using simulators such as Spectre RF to obtain phase noise characteristics for different offset frequencies [6]. A parametric sweep of the separately driven setup will be performed by modifying control inputs in the form of bias voltages and load capacitances to assess their effect on phase noise. Monte Carlo simulations will also be conducted to investigate the impact of process variations.

The performance of the results from the separately driven and conventional oscillators will then be compared based on phase noise performance, power consumption, frequency stability, and design complexity. Lastly, the simulation results will be compared with theoretical predictions, and optimization techniques will be suggested to improve

phase noise performance in the separately driven architecture without increasing power or area overhead considerably.

III. IMPLEMENTATION DESIGN

In this paper, both 3-stage and 5-stage separately driven ring oscillators are designed and investigated to analyze the effect of independent stage control on phase noise performance. The design is implemented based on a standard CMOS technology node (e.g., 180nm or 65nm), and simulations are performed with Cadence Virtuoso and SpectreRF for precise phase noise characterization [2].

The fundamental structure of a ring oscillator is an odd number of inverter stages arranged in a loop, with the signal traveling sequentially through each stage in order to maintain oscillation. In the standard implementation, all inverter stages are identically biased, using a common power supply and control. By comparison, the separately driven architecture adds individual control to each stage—either in the form of distinct bias voltages or current sources—enabling more precise control of each stage's behavior and possibly better noise performance.

For the 3-stage ring oscillator, the three CMOS inverter stages are in a loop configuration [7]. In the independently driven configuration, every stage is driven by its own separate current source, which is realized in terms of current mirrors or programmable bias circuits. Each inverter stage can thus be run at optimized current levels, minimizing the total phase noise through minimization of delay propagation jitter.

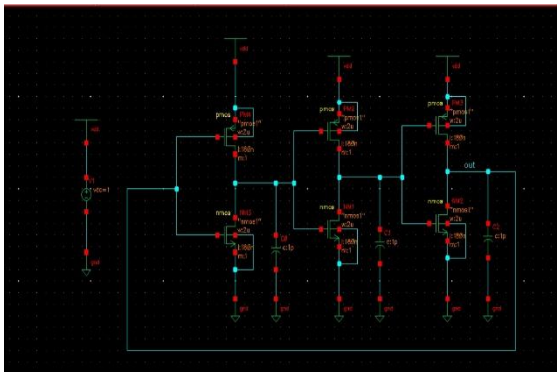

Fig.3.1 3-STAGE SDRO

In the same manner, the 5-stage ring oscillator employs five stages of inverters for a longer delay path and generally lower oscillation frequency than the 3-stage version. The drive-steered configuration operates on the same principle, but in this configuration each stage is independently biased. This allows greater flexibility in adjusting the delay and noise contribution of every stage, an importance that only grows as the number of stages rises and the accumulation of noise sources will occur.

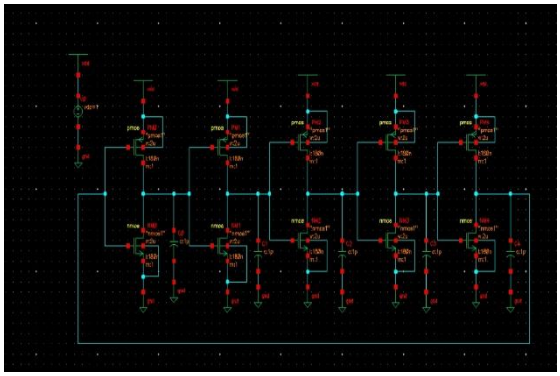

Fig.3.2 -STAGE SDRO

Transistor size is carefully chosen to obtain good oscillation and low noise performance. The width ratio of PMOS to NMOS is tuned to optimize the balance between rise/fall times and distortion. The simulation is run to obtain the major metrics like oscillation frequency, stability of the output waveform, power dissipation, and phase noise at multiple frequency offsets (e.g., 100 kHz, 1 MHz, 10 MHz). Monte Carlo runs are also performed to analyze the resilience of 3-stage and 5-stage designs against process variations.

Through the use of and comparison between 3-stage and 5-stage separately driven ring oscillators, this research hopes to give a thorough insight into the influence of stage number and individual control on phase noise behavior. The findings form the basis for low-noise oscillator design optimization in high-performance and low-power applications.

IV. OUTPUTS AND DISCUSSION

The comparison is made between the behaviour of 3-stage and 5-stage separately driven ring oscillators (SDROs) in terms of their phase noise, transient response, and overall circuit behaviour by using Cadence Virtuoso simulations [12].

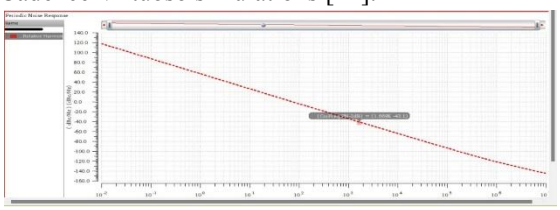

Fig: 4.1 PHASE NOISE OF 3-STAGE

The simulation illustrates the operation of a 3-stage ring oscillator in Cadence Virtuoso. The transient response demonstrates stable and periodic oscillations in the output node. The voltage swing varies from around -50 mV to 950 mV.

The waveform validates proper oscillator operation with a stable frequency. From the timing, the oscillation frequency is in the MHz range. The noise response plot illustrates phase noise in terms of power spectral density. Low-frequency region is where flicker noise rules, indicated by the high slope. It starts to fall flat as the frequency rises and approaches thermal noise. This is characteristic phase noise plot for a ring oscillator [13].

Phase noise plots for both cases show the 5-stage oscillator to have lesser close-in phase noise and a lower corner frequency (~807.7 Hz) than the 3-stage version (~1.669 kHz), suggesting improved flicker noise suppression.

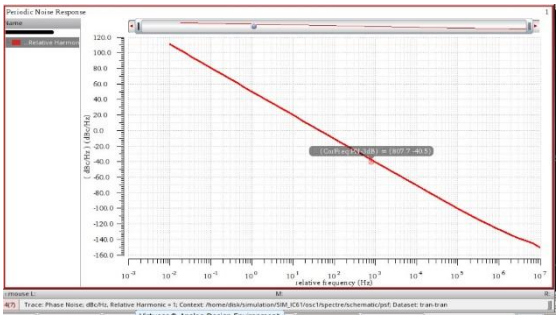

Fig: 4.2 PHASE NOISE OF 5-STAGE

The simulated results presented here are for a 5-stage ring oscillator simulated in Cadence Virtuoso. The transient response on the left shows a clean, periodic wave from node /net25 with voltage values oscillating between about -0.1 V and 1.0 V. The output shows stable oscillations with a longer period than the 3-stage design, showing a reduced oscillation frequency, as would be expected owing to the higher number of stages. The waveform is steep with well-defined falling and rising edges. To the right, the noise response is the phase noise characteristics expressed in terms of power spectral density (V^2/Hz). The plot exhibits a sharp drop in lower offset frequency due to preponderant 1/f (flicker) noise and then a level region dominated by thermal noise. This pattern corresponds to common oscillator phase noise behavior. The shape and amplitude of the noise curve indicate that phase noise is under good control [19].

Both oscillators demonstrate the theoretical behaviour expected for low frequencies with -30 dB/decade slopes dropping to flat white noise sections at higher frequencies.

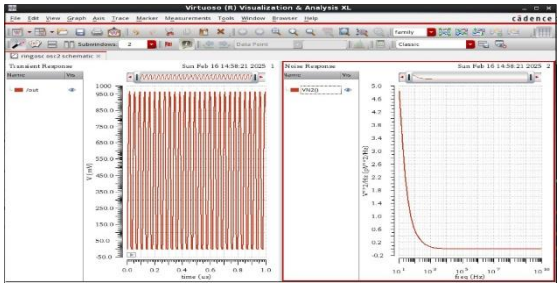

Fig :4.3 transient response and noise response of 3-stage SDRO

The transient response also complies with expectations—3-stage oscillators oscillate at higher frequencies as there are fewer stages, and the 5-stage configuration oscillates at lower frequency but provides better signal stability and lower jitter.

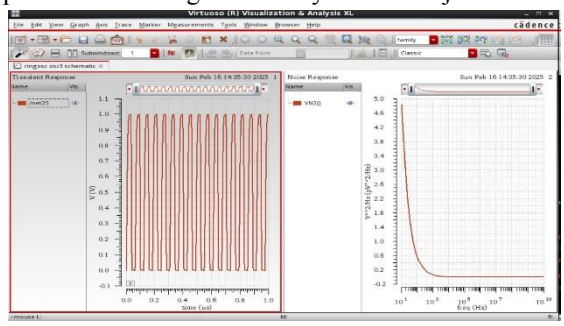

Fig :4.4 transient response and noise response of 5-stage SDRO

Noise spectral density plots also confirm the better performance of the 5-stage oscillator, registering lower voltage noise across frequencies and a purer signal profile, thus better recommending it for high-precision applications like RF communication and PLLs. As great as the 3-stage SDRO's higher frequency output and full voltage swing, it is plagued with higher phase noise and greater susceptibility to noise disturbances due to its shorter delay loop [20].

The figure illustrates a comparison of 3-stage and 5-stage separately driven ring oscillator (SDRO) phase noise performance over a frequency span. The graph makes it immediately evident that the 5-stage SDRO (red line) performs consistently at a lower phase noise level compared to the 3-stage SDRO (black line). This represents enhanced frequency stability and suppression of noise within the 5-stage design. While increasing frequency, the noise level for both oscillators declines, but the 5-stage arrangement retains better performance across. This shows that adding more stages can efficiently minimize phase noise in ring oscillators.

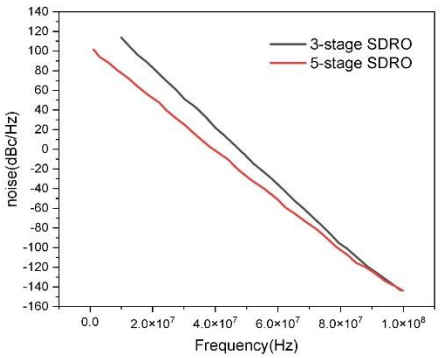

Fig 4.5 comparison

The comparison shows a compromise between frequency and noise performance: although 3-stage oscillators are faster, 5-stage ones provide better noise control and waveform integrity, essential for high-precision, low-jitter implementations of circuits [14][15].

V. CONCLUSION

The phase noise analysis of the separately driven ring oscillator in 180nm CMOS technology was performed successfully using Cadence Virtuoso. The 3-stage and 5-stage inverter-based ring oscillators were simulated through PSS and PNOISE analyses using Spectre RF [16][18].

The research identified that:

3-stage oscillators have a greater frequency of oscillation due to fewer stages of delay but also exhibit higher phase noise at near-in frequency offsets. This is largely a consequence of having shorter delay per loop and lower averaging of the sources of noise.

5-stage oscillators, which at lower frequencies performed better in phase noise, particularly at low offset frequencies. The extra stages help in averaging the noise and reduce the per-stage sensitivity, leading to lower accumulation of jitter.

The phase noise profile in both instances is determined by the transistor size, bias point, and load capacitance at every stage [7]. Symmetric inverter design and balancing of rise and fall times assisted in enhancing phase noise performance [17].

The individually driven configuration allowed for accurate injection and measurement of noise contributions on a per-inverter-stage basis, allowing better understanding of each stage's behaviour and enabling stage-by-stage optimization.

In summary, adding more inverter stages to a ring oscillator provides trade-offs between phase noise and oscillation frequency. For low phase noise applications, a 5-stage design is preferable, whereas for higher frequency operation, a 3-stage design can be preferred, though with proper noise control

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