VLSI Realization of Area Efficient Carry Select Adder

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***Abstract*-This paper presents an optimized approach to datapath logic design in VLSI systems by replacing Ripple Carry Adders (RCA) in Carry Select Adders (CSLA) with Binary to Excess-1 Converters (BEC). This substitution significantly enhances speed and reduces power usage and it also reduce the area, addressing key challenges in modern chip design. As VLSI continues to scale, managing power, delay, and area becomes critical. The proposed method supports compact, energy-efficient layouts suitable for high-speed digital systems. Implemented using CMOS technology and described in HDL, the design aligns with current trends in automated digital design, while supporting greater performance in embedded and applications.**

Keywords: **RCA, BEC, CSLA, etc…**

1.INTRODUCTION

In today's digital world, the efficiency of core components like arthimatic units plays a critical role in determining the overall performance, power consumption, and space requirements of electronic systems. Among these components, adders are fundamental, forming the backbone of many operations in processors, embedded systems, and signal processing units. One of the faster options available is the carry select adder (CSLA), which improves speed by calculating outcomes in parallel for different carry-in values[1][2]. However, this speed gain often comes at the cost of increased hardware usage, as traditional CSLA designs duplicate multiple blocks, leading to a larger silicon area.

To overcome this issue, researchers have explored various techniques aimed at making CSLAs more compact without compromising their performance. In this work, we present an efficient VLSI design of a modified CSLA that uses binary to excess-1 code (BEC) logic along with streamlined structural optimizations to reduce unnecessary circuit duplication. The result is a design that consumes less area and power, while still maintaining fast operation. Using standard CMOS process technology, the proposed adder has been designed, implemented, and analyzed. The results show that the new approach is well-suited for applications where both speed and compactness are key considerations [4][5].

2.DESIGN PROCEDURE

RIPPLE-CARRY ADDER:

The ripple carry adder is a team of simple adders—called full adders—linked together in a straight line. Each one takes care of adding a pair of bits (one from each number) and a carry that might come from the person (adder) before them[6].

Here's how the ripple effect works:

- The first adder starts the process. It adds the lowest bits and generates a sum and possibly a carry.
- That carry is passed to the next adder, like a whisper down the line.
- The next adder takes its own pair of bits and that carry, adds them up, and passes on the new carry.

Carry Select Adder:

A Carry Select Adder [6]is a specialized adder design used to speed up binary addition by reducing the delay caused by carry propagation. Instead of waiting for the carry from the previous bit position, the CSLA anticipates both possible outcomes.

It works by using two separate ripple carry adders in parallel:

- One adder performs the sum assuming the carry-in is 0.
- The other adder does the same calculation assuming the carry-in is

BINARY TO EXCESS ONE CONVERTER:

As stated above the main purpose is to use BEC with replace of the RCA with cin=1 in order of the regular CSLA. To replace the *n*-bit RCA, an *n*+*1*bit BEC is required. A structure and the function table of a 4-b BEC are shown in Figure and Table 1.

The core operation of a Carry Select Adder (CSLA) can be achieved by incorporating a 4-bit Binary to Excess-1 Converter (BEC) along with a multiplexer, as illustrated in Figure 4.4. In this configuration, one set of inputs to the 8:4 multiplexer consists of the bits (B3, B2, B1, B0), while the other set comes from the BEC. Out comes to be calculated in parallel. the value of the carry-in signal (Cin), the multiplexer selects between the BEC output and the original input bits.

The significance of using BEC logic becomes particularly evident in designs involving wide-bit adders, where it contributes to a notable reduction in silicon area[1][10]. Below this explanation, the Boolean logic equations for the 4-bit BEC are provided, using standard logical operators such as NOT (~), AND (&), and XOR (^).

X0=~B0
X1=B1^B0
X2=B2^(B0&B1) ----------(4.1)
X3=B3^(B0&B1&B2)

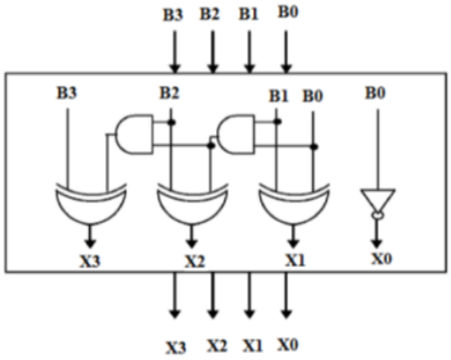

Fig:1. 4 bit BEC

CALCULATION:

Let us consider 1011 as the input for the 4 bit BEC and the output should be 1100.by substituting the above input values in the above equations. We have

X0 =~B = ~1 = 0
X1 = B0^B1 =1^1=0
X2 = B2^ (B0&B1) = 0^1 =1
X3 = B3^ (B2&B1&B0) = 0^1 =1

Therefore the output value for 1011 input is obtained as 1100 which is the binary excess 1 value of input. Where B0B1B2B3 are the inputs for the 4 bit BEC and X0X1X2X3 are the outputs.

3. IMPLEMENTING DESIGN

Carry Select Adders (CSLAs) are widely used in digital systems where fast arithmetic operations are essential—such as in processors or real-time embedded applications. They improve speed over conventional adders by calculating possible outcomes for both scenarios of the carry-in bit (0 and 1) simultaneously. However, this dual-path approach increases hardware usage, as it typically involves duplicating adders[1][7].

To address this, designers often replace one of the duplicate adders with a Binary to Excess-1 Converter (BEC). A BEC is a compact circuit that efficiently adds 1 to a binary number. This strategy eliminates the need for two complete adders, saving space and reducing power consumption while maintaining high-speed performance[11][12].

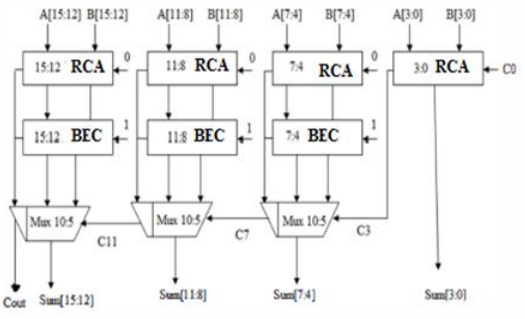

Fig: 2. Carry Select Adder Using Binary to Excess One Converter

The process works as follows:

1. Divide the Input: Large binary numbers are split into smaller blocks to be processed in parallel.
2. Perform Addition Assuming Carry-In is 0: Each block is first added using a Ripple Carry Adder under the assumption that the carry-in is 0. Generate Alternative Result Using BEC: The result of the initial addition is passed through the BEC, which produces the output for the case where carry-in is 1.
3. Select the Correct Output: A multiplexer (MUX) chooses between the original adder output and the BEC output based on the actual carry-in from the previous block.
4. Combine Results: The final result is assembled by linking together the selected outputs from each block.

This design significantly reduces the required silicon area because the BEC is more compact than a full second adder. It strikes an effective balance between speed and resource efficiency, making it a popular solution for space-constrained, high-speed digital circuits.in conclusion, integrating a BEC into a Carry Select Adder design is a smart optimization that enhances efficiency while maintaining

performance—ideal for systems where both speed and resource conservation are crucial.

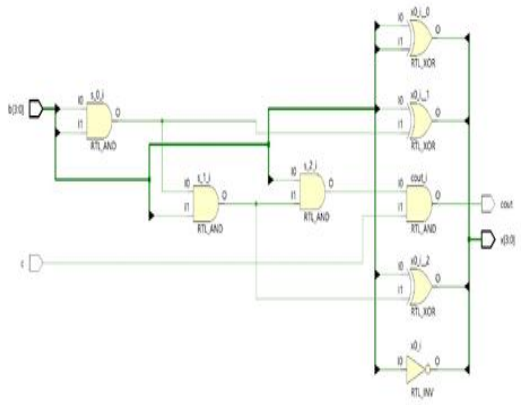

Fig:3. Schematic diagram of BEC

4.SOFTWARE USED

XILINX ISE

Xilinx ISE (Integrated Software Environment) is a comprehensive toolset designed for the development of digital systems using Xilinx FPGAs (Field Programmable Gate Arrays) and CPLDs (Complex Programmable Logic Devices). It supports various design input methods including schematics, hardware description languages (HDLs) like Verilog and VHDL, and custom modules. In schematic-based design, components are represented by graphical symbols and connections by wires.

This tool suite allows designers to complete the full design cycle, from initial entry to final device configuration. The major phases in the design process include:

1. Design Entry
2. Synthesis and Implementation
3. Simulation and Functional Verification
4. Device Testing and Deployment

Designs can be specified in a number of ways using ISE, such as through schematics or HDL code. In this context, we focus on a design flow that employs Verilog HDL exclusively.

- Xilinx Inc., “Xilinx ISE Design Suite User Guide,”[Online].Available:https://www.xilinx.com

5.RESULTS AND DISCUSSION

The proposed designs were implemented using Xilinx tools. Our Area-Efficient Carry Select Adder (CSLA) demonstrates excellent performance in terms of power consumption. Significant energy savings are achieved because each sum operation requires only a single XOR and inverter gate[1][5], while each carry-out operation needs just one AND and one OR gate, following logic optimization and partial circuit sharing. Through hardware reuse, the design also minimizes the occurrence of glitches. Furthermore, the reduction in power consumption becomes more pronounced as the input bit-width increases.

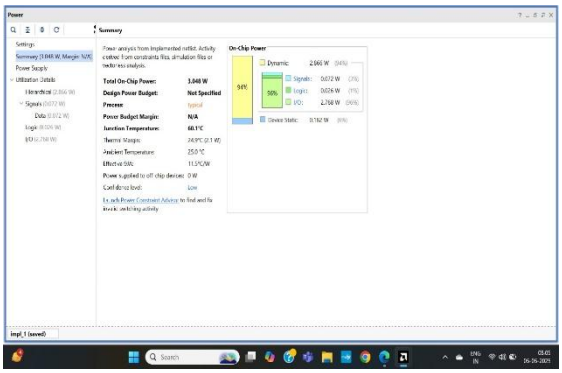

Fig:4. RCA power

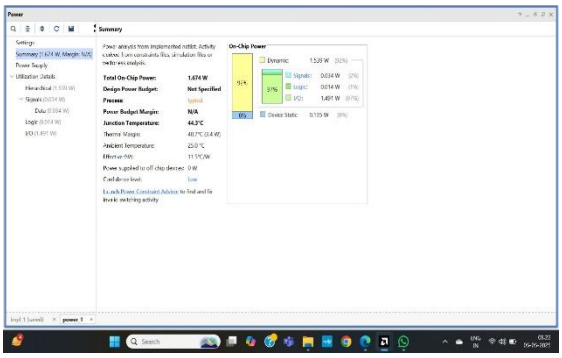

Fig:5. BEC power

Although the conventional carry select adder shows better speed performance, the delay in the proposed design increases only slightly due to the shared logic circuits, which somewhat lengthen the parallel path. Nevertheless, the proposed area-efficient CSLA maintains a partially parallel structure similar to that of traditional CSLAs, and the delay growth trend remains consistent as the input size scales. Simulations were conducted to compare the delay performance of both designs for input widths of 4, 8, and 16 bits [9][10].

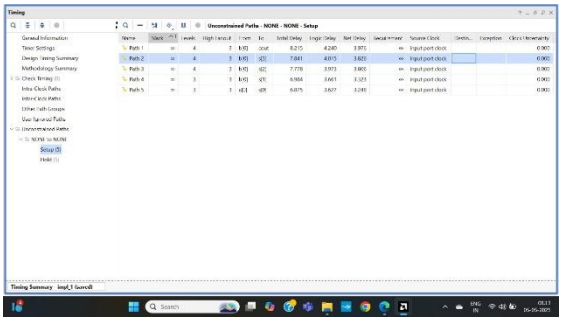

Fig:6. RCA Delay

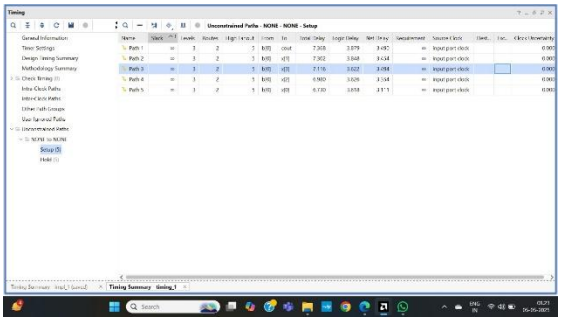

Fig:7. BEC Delay

6.CONCLUSION

Addition is the most frequent and utilized arithmetic function on microprocessor, digital signal processor, particularly digital computers. Moreover, it is a basis for synthesis all other arithmetic functions. Hence, in terms of economic implementation of an arithmetic logic unit, the adder structures become an extremely crucial hardware component.

In any computer arithmetic book, somebody sees that there is a wide variety of distinct circuit architectures having various performance attributes and commonly utilized in practice. Despite numerous studies related to the adder structures, the investigations on the basis of their comparative performance analysis are limited.

Digital Adders form the central block of DSP processors. The final carry propagation adder. (CPA) architecture of most adders entails high carry propagation delay and decreasing the said delay lowers the entire performance of the DSP processor. In the course of this project, qualitative appraisals of the CSLA adder and without BEC architectures are provided. Between the enormous member of the adders we crafted VERILOG (Hardware Description Language) programming of Carry skip and carry select adders in order to stress common per performance traits belong to classes. As far as delay time and power consumption are concerned we can say that the use of CSLA with BEC is effective. The primary benefit of this BEC logic is due to the smaller number of logic gates compared to then-bit Full Adder (FA) structure.

Today Carry Select Adder (CSLA) employed in most data-processing processors toper implement quick arithmetic operations. That is why we have proposed a configurable adder with low delay overhead, and power efficient. CSLA RCA can be substituted by CSLA BEC Where speed and power are the primary constraints. The proposed CSLA BEC only consumes 17mw which is very low when compared to the existing CSLA RCA which consumes 37mw[1].

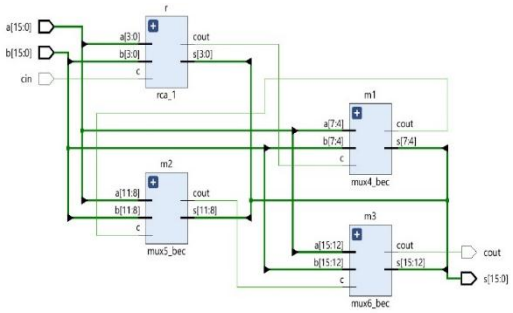

Fig:8. Schematic diagram of CSLA using BEC

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