Comparative Analysis of 7T,10T And 12T SRAM Scheme For Upcoming VLSI Design

Pratik Kumar Dubey[1], Unnati Gaur[2], Pari Sharma[3]
[1](Assitant Professor) Electronics And Communication Engineering, R.D. EngineeringCollege(AKTU University) Ghaziabad , India
[2,3] Department of Electronics And Communication Engineering R.D. EngineeringCollege (AKTU Univesity) Ghaziabad,India

***Abstract*—This study explores and analyzes CMOS SRAM cells utilizing advanced technology nodes, with a focus on three distinct architectures: the 7-transistor (7T), 10-transistor (10T), and 12-transistor (12T) SRAM cells. The primary objective is to assess their performance through simulations conducted in Cadence Virtuoso, evaluating critical metrics such as power consumption, Static Noise Margin (SNM), read delay, and write delay. The design methodology involves schematic design and simulation of each SRAM cell type under various operating conditions to investigate their functionality and performance characteristics. Simulation results reveal trade-offs among the architectures, with the 7T cell offering a balance of simplicity and efficiency, the 10T cell providing enhanced stability, and the 12T cell excelling in low-power and high-reliability applications. These findings underscore the potential for selecting an appropriate SRAM architecture based on specific application requirements, optimizing for performance, area efficiency, and robustness in emerging technologies.**

Keywords—Write Delay, Read Delay, Static Noise Margin (SNM), Power Consumption, SRAM, CMOS Technology.

I. INTRODUCTION

Static Random Access Memory (SRAM) has become essential to all SOC layouts. SRAM has excellent flexibility with logical circuit designs and is utilized extensively in current high-performance solutions [1]. Technology scaling enables several enhancements in devices, including enhanced performance, decreased power usage, and decreased area, which was made possible by making the device smaller. Despite this, as technology nodes diminish, making circuits more susceptible to distortion and unreliability [2].In contemporary times, there has been a significant focus on studying memory circuits that make minimal use of power, driven mainly by the energy limitations of battery-powered gadgets. These memories should meet stringent reliability and power efficiency criteria since they handle large volumes of data to prolong battery life.

In addition, the utilisation of complementary metal oxide technology for semiconductors (CMOS) permits an increase in chip density and enhanced response speed. Nevertheless, this enhancement is accompanied by the disadvantage of undesirable leakage effects and durability concerns. Lowering the supply voltage is an efficient method for dealing with leakage problems, leading to a proportional decrease in power usage and a significant reduction in leakage currents[3].

SRAM is a type of high-performance, low-power memory with random access that stores data without constant refreshment Commonly used in cache memory for computers, its compact size and cost make it less suitable for primary memory SRAM is utilized in a variety of devices, including graphics cards, disk drives, printers, LCD displays, routers, cell phones, wearables, medical products, industrial equipment, and various IoT devices. [4].

II. RELATED WORK

Recent studies have explored SRAM cell designs for low-power and high-stability applications. A 7T SRAM cell proposed in [1] enhances write stability for high-speed applications using 45nm technology, achieving reduced read delay compared to simpler designs. The 10T SRAM cell, as discussed in [2], focuses on leakage characterization and stability improvements, particularly in 65nm CMOS, with applications in sub-threshold operation. For low-power applications, a 12T SRAM cell design in 45nm technology [3] employs power-gating techniques to significantly reduce leakage power, addressing half- select issues observed in earlier

designs. Additionally, FinFET-based 12T SRAM cells [4] demonstrate improved power efficiency and soft-error immunity in 18nm technology, making them suitable for high-reliability applications. These works provide a foundation for comparing advanced SRAM architectures in emerging technology nodes.

III. PERFORMANCE PARAMETER

The performance of SRAM cells is evaluated based on four key parameters:

3.1 Write Delay

Write delay is the time required to complete a write operation, measured from when the word line reaches 50% of its maximum value to the stabilization of the storage node. It is influenced by the write driver, bit-line configuration, and access transistor sizing.

3.2 Read Delay

Read delay quantifies the time taken to retrieve data, measured from the word line transitioning to 50% of its maximum value to the output response. Lower read delay is critical for read-intensive applications, depending on bit-line pre-charge and sense amplifier performance.

3.3 Static Noise Margin (SNM)

SNM measures the cell's stability against noise-induced state changes, particularly during read operations (R-SNM). It is derived from the butterfly curve, representing the maximum DC noise voltage the cell can tolerate without

3.4 Power Consumption

Power consumption includes static (leakage) and dynamic components. Static power arises from transistor leakage currents, while dynamic power results from node charging/discharging during read/write operations. Advanced designs aim to minimize both for energy efficiency. 2limit use of hard returns to only one return at the end of a paragraph. Do not add any kind of pagination anywhere in the paper. Do not number text heads-the template will do that for you.

IV. DESINGING AND SIMULATION OF 7T,10T AND 12T SRAM CELL

1. 7T SRAM CELL

The 7T SRAM cell extends the conventional 6T design by adding a seventh transistor (M7) to optimize write operations. This transistor enables differential bit-line writing, setting one bit-line to '1' and the other to '0', reducing power consumption compared to single-ended writes. The schematic includes cross-coupled inverters for data storage and access transistors connecting storage nodes (Q, QB) to bit-lines (BL, BLB). The additional transistor enhances write stability and reduces read disturbance, making the 7T cell suitable for low-power, high-speed applications [1].

Fig1.1 of Schematic of 7T S-RAM Cell

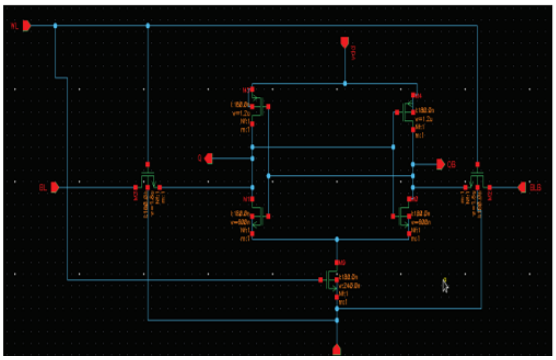


Fig1.2 of Transient Response of 7T SRAM Cell

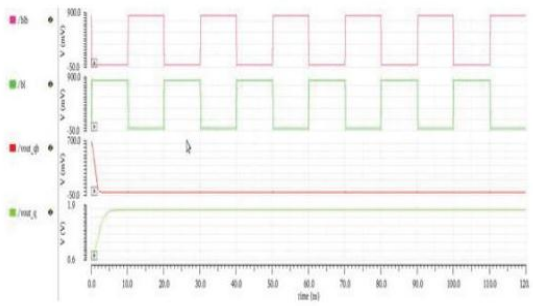
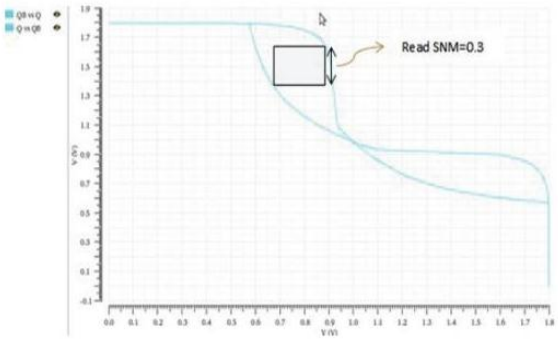


Fig1.3 of Butterfly Curve for 7T SRAM cell



2. 10T SRAM CELL

The 10T SRAM cell incorporates four additional transistors over the 6T design, featuring separate read and write paths to enhance stability. It uses dedicated read bit-lines (RBL) and word lines (RWL) to isolate storage nodes during read operations, significantly improving R-SNM. The write path employs series access transistors to ensure robust data transfer. Techniques such as Schmitt-trigger inverters and power-gating are often applied to reduce power consumption and enhance low-voltage operation, as noted in [2]. The 10T cell is ideal for sub-threshold applications requiring high stability.

Fig2.1 of Schematic of 10T S-RAM Cell

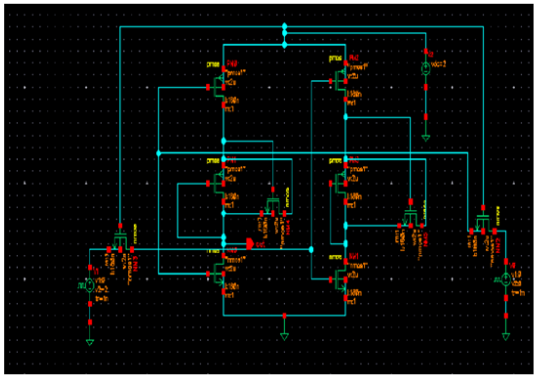


Fig2.2 of Transient Response of 10T SRAM Cell

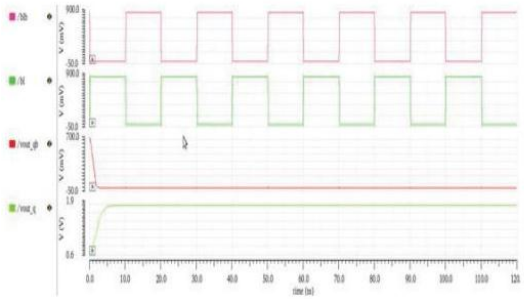
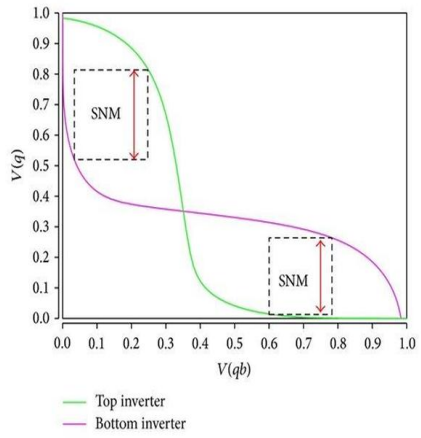


Fig2.3 of Butterfly Curve for 10T SRAM cell



3. 12T SRAM Cell

The 12T SRAM cell is designed for ultra-low-power and high-reliability applications, particularly in sub-threshold regimes. It includes additional transistors to implement power-gating and sleepy-stack techniques, reducing leakage power. The cell features redundant nodes and polar designs to mitigate soft errors caused by radiation, as described in [3]. Separate read and write word lines enhance stability, while dual-threshold voltage transistors minimize leakage. The 12T cell excels in applications demanding robustness, such as aerospace and IOT devices, but requires more area.

Fig 3.1 of Schematic of 12T S-RAM Cell

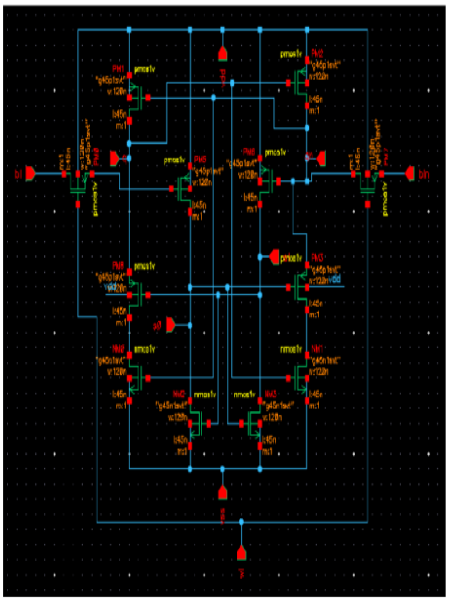


Fig3.2 of Transient Resopnse of 12T SRAM Cell

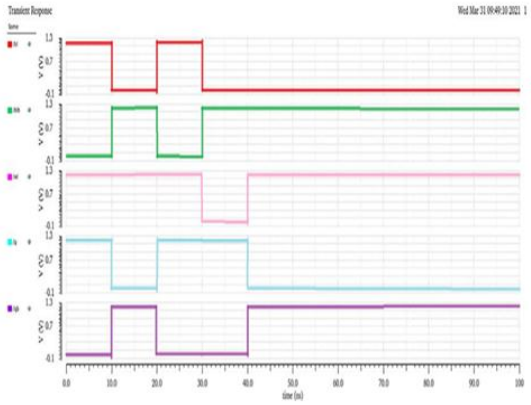
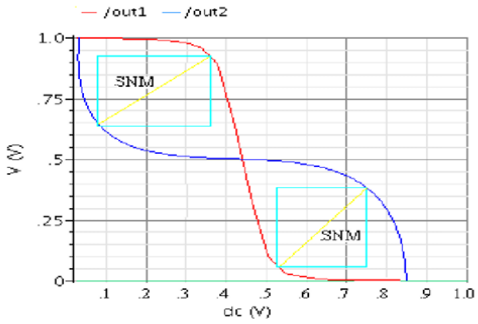


Fig3.3 of Butterfly Curve for 12T SRAM cell



V. PERFORMACE EVOLUTION

The 7T, 10T, and 12T SRAM cells were designed and simulated using Cadence Virtuoso in a 45nm CMOS technology node. The performance metrics are summarized in Table 1.

Table 1: Comparative Analysis of 7T, 10T, and 12T SRAM Cells

Parameters	7T SRAM	10T SRAM	12T SRAM	% Improvement (12T vs. 7T)
Write Delay (ns)	0.752	0.242	0.226	69.95
Read Delay (ns)	0.456	0.167	0.152	66.67
Read SNM (V)	0.375	0.600	0.650	73.33
Power Consumption (µW)	1.09	2.01	0.226	79.27

VI. ANALYSIS

1. 7TSRAM:Offersabalanceofperformancewithare addelayof0.456nsand power consumption of 1.09 µW.However, its R-SNM (0.375 V) is lower, indicating moderate stability [1].
2. 10TSRAM:Achievesfasterread/writedelays(0. 167nsand0.242ns)andhigherR- SNM (0.600 V), but consumes more power (2.01 µW) due to additional transistors [2].
3. 12T SRAM: Demonstrates the lowest power consumption (0.226 µW) and fastest delays (0.152 ns read, 0.226 ns write), with the highest R-SNM (0.650 V), making it ideal for low-power, high-reliability applications [3].

VII. CONCLUSION

This study compares 7T, 10T, and 12T SRAM cells in a 45nm CMOS technology node, highlighting their performance trade-offs. The 7T cell provides a cost-effective solution for general-purpose applications, while the 10T cell excels in stability for sub-threshold operations. The 12T cell outperforms both in power efficiency and reliability, making it suitable for emerging technologies like IoT and aerospace, despite its larger area. These results guide designers in selecting optimal SRAM architectures based on application- specific requirements.

VII. FUTURE SCOPE

The future scope of VLSI design comparative analysis of 7T, 10T, and 12T SRAM schemes will focus on improving stability, performance, and power consumption. These SRAM designs will be suitable for applications of the next generation thanks to advancements in technologies like FinFET and CNTFET.

The future scope of using 7T, 10T, and 12T SRAM in circuit design focuses on enhancing performance, reducing power consumption, and improving stability. As technology advances, these SRAM configurations can be optimized for applications in low-power devices, high-speed computing, and advanced memory systems, addressing the growing demand for efficient and reliable memory solutions. ### Future Scope of Using 7T, 10T, and 12T SRAM

REFERENCES

[1] P. Upadhyay, S. K. Chhotray, R. Kar, D. Mandal, S. P. Ghoshal, “Write stability analysis of 8-T novel SRAM cell for high speed application,” in 2019 3rd IEEE International Advance Computing Conference (IACC), 2019.

[2] A. Islam, M. Hasan, “Leakage characterization of 10T SRAM cell,” IEEE Trans. Electron Devices, vol. 59, no. 3, pp. 631–638, 2012.

[3] T. Santosh Kumar, “Robust 12T SRAM cell using 45nm technology,” ScienceGate, 2021.

[4] A. Rastogi, V. K. Tomar, “Comparative analysis of 6T, 9T and 10T SRAM cells using 18 nm FinFET technology,” in Internet of Things and Connected Technologies, ICIoTCT 2020, Springer, Cham, 2021.