Design & Analysis of 32-Bit Vedic Multiplier using Parallel Prefix adder for Low Power Applications

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***Abstract*—Multiplication plays a vital role in digital signal processing, image processing, and various computational tasks, where the efficiency of the multiplier directly influences overall system performance, particularly in low-power environments. This paper introduces a 32-bit Vedic multiplier architecture that incorporates a parallel prefix adder to enhance speed and minimize power consumption. Leveraging the principles of ancient Indian Vedic mathematics, the design enables efficient partial product generation and reduced computational complexity. The integration of a parallel prefix adder in the accumulation phase further accelerates computation and improves energy efficiency. Comprehensive analysis in terms of power, area, and delay confirms the proposed design's suitability for high-performance, low-power applications.**

***Index Terms*—Vedic Multiplier, Parallel prefix Adder**

I. INTRODUCTION

Multiplication is a fundamental arithmetic operation widely used in digital signal processors (DSPs) for applications such as convolution, FFTs, filters, and within the Arithmetic Logic Unit (ALU) of microprocessors. Due to its frequent use, it is essential to design multipliers that are both fast and power-efficient. Arithmetic operations range from simple tasks like counting to complex scientific and business computations, highlighting the need for a high-speed, effective arithmetic unit in computers. Among various methods, array multiplication offers lower delay compared to partial product parallel techniques. Booth multipliers, known for high-speed performance, use large booth arrays and require registers for partial sums and carries; for two n-bit operands using radix-4 booth encoding, approximately n/(2k) clock cycles are needed, where k is the number of recording stages. Alternatively, the UrdhvaTiryakbhyam Sutra, an ancient Indian "vertical and crosswise" algorithm, provides a scalable and structured method for digital multiplication by breaking down N×N bit operations into smaller parts recursively until reaching a 2×2 base case, forming a tree-like structure for streamlined computation.

II. LITERATURE SURVEY

1. Parameshwara, M.C. presents six innovative approximate 1-bit full adders (AFAs)—AFA1 through AFA6—tailored for energy-efficient image processing applications in the *Journal of Circuits, Systems and Computers*. These AFAs are derived from standard exact full adder (EFA) architectures and evaluated against existing approximate full adders (RAAs) using critical design metrics such as power, delay, PDP, EDP, area, and PSNR. Developed in Verilog and synthesized using Cadence's RC tool with a 180 nm standard cell library, the study finds AFA1 and AFA2 to be the most energy-efficient, each offering high PSNR values (26.4292 dB) and low EDPs, making them highly suitable for power-sensitive image processing tasks.

2. In the 2021 ICCCIS proceedings, Choppala et al. propose a novel 8-bit hybrid Wallace tree multiplier aimed at optimizing area, power, and speed. Recognizing the hardware complexity and power limitations of traditional multiplier designs, the authors introduce a GDI-based 1-bit hybrid full adder within the Wallace tree and array multiplier structures. Implemented using Tanner EDA with 250 nm technology, the proposed design demonstrates significant enhancements in speed, power efficiency, and full voltage swing performance compared to conventional CMOS and GDI designs, making it an effective solution for advanced digital processing systems.

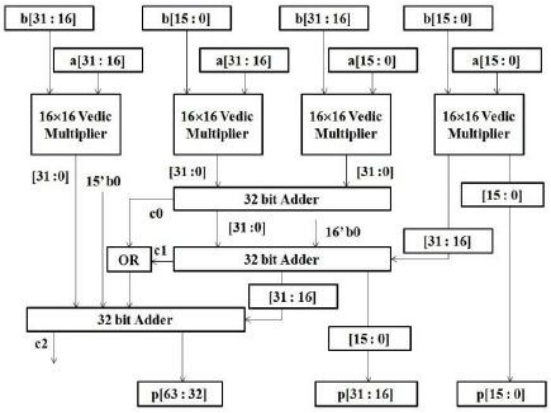
III. EXISTING METHOD

Conventional multipliers like the array and Booth architectures are commonly used for their simplicity

and reliable performance but tend to suffer from high power consumption, increased delay, and larger area, especially when scaled to 32-bit operations. The array multiplier is slowed down by extensive carry propagation, while the Booth multiplier, although efficient for signed operations, adds logic complexity. In contrast, Vedic multiplication, particularly the UrdhvaTiryagbhyam method, offers faster computation and lower hardware complexity by enabling parallel processing of partial products. However, the efficiency is often limited by the final addition stages, which traditionally uses ripple carry or carry look-ahead adders. To address this, parallel prefix adders like Kogge-Stone, Brent-Kung, and Han-Carlson are increasingly adopted for their high-speed, low-power performance and scalability in modern Vedic multiplier designs.

IV. PROPOSED METHOD

The proposed method presents a 32-bit Vedic multiplier integrated with a Parallel Prefix Adder (PPA) to achieve low power and high-speed performance. Utilizing the UrdhvaTiryagbhyam sutra, the Vedic approach enables parallel generation of partial products, while the use of a PPA—such as Kogge-Stone or Brent-Kung—ensures fast and efficient summation through high-speed carry propagation and reduced delay. By segmenting the inputs and recursively combining the results, the design minimizes switching activity and dynamic power consumption. Implemented in Verilog and synthesized using a standard technology library, the architecture is evaluated on metrics like power, delay, area, and PDP, showing enhanced efficiency over traditional multiplier designs for low-power digital processing applications.



V. RESULTS

VI. CONCLUSION

This paper proposes a high-performance 32-bit Vedic multiplier integrated with a parallel prefix adder to enhance the efficiency of arithmetic operations. By leveraging the fast partial product generation of the Vedic multiplication technique and the rapid carry computation of the parallel prefix adder, the design achieves notable improvements in both speed and power consumption over conventional multiplier architectures. Simulation results confirm the effectiveness of the proposed design, highlighting its reduced delay and lower power dissipation. This makes it an ideal solution for modern applications requiring high-speed and energy-efficient arithmetic processing.

VII. FUTURE SCOPE

The proposed design offers significant potential for further optimization through hardware implementation using FPGA or ASIC technologies. Future enhancements may include the development of adaptive architectures capable of dynamically allocating computational resources based on workload demands, thereby improving efficiency. Incorporating approximate computing techniques can also help reduce power consumption, particularly in error-tolerant applications where slight inaccuracies are acceptable. Moreover, extending the principles of Vedic multiplication to emerging domains such as quantum computing and neuromorphic processing presents exciting opportunities for advanced, energy-efficient computing architectures.

REFERENCES

[1]. Parameshwara, M.C., “Approximate full adders for energy efficient image processing applications" Journal of Circuits, Systems and Computers, vol. 30, issue 13, pp.1-17, Oct. 2021.

[2]. P. Choppala, V. Gullipalli, M. Gudivada and B. Kandregula, "Design of Area Efficient, Low Power, High Speed and Full Swing Hybrid Multipliers," 2021 International Conference on Computing, Communication, and Intelligent Systems (ICCCIS), 2021, pp. 929-934.

[3]. A. Jain, S. Bansal, S. Khan, S. Akhter and S. Chaturvedi, "Implementation of an Efficient N×N Multiplier Based on Vedic Mathematics and Booth-Wallace Tree Multiplier" 2019 International Conference on Power Electronics, Control and Automation (ICPECA), 2019, pp. 1-5.

[4]. M. Munawar et al., "Low Power and High Speed Dadda Multiplier using Carry Select Adder with Binary to Excess-1 Converter," 2020 International Conference on Emerging Trends in Smart Technologies (ICETST), pp. 1-4, 2020.

[5]. Parameshwara, M.C., Nagabushanam, M. " Novel low quantum cost reversible logic based full adders for DSP applications. " International Journal of Information Technology.2021, vol. 13, pp.1755–1761.

[6]. C.W.Tung and S.H. Huang, "A High-Performance Multiply- Accumulate Unit by Integrating Additions and Accumulations into Partial Product Reduction Process," in IEEE Access, vol. 8, pp. 87367-87377, 2020.