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Implementation of High-Speed: High Speed 16bit Carry Look a Head Adder Using 4bit Cla Adders

RNS. Kalpana[1], K. Arun kumar[2], D. Hemavathi[3], D. Ashwitha[4]
[1]*Assistant Professor, Dept of ECE, TKR College of Engineering and Technology*
[2,3,4]*Student, Dept of ECE, TKR College of Engineering and Technology*

Abstract: In the realm of digital systems, the speed of arithmetic operations plays a crucial role in determining overall system performance. Among these operations, binary addition is the most fundamental and widely used. This paper presents the design and implementation of a high-speed 16-bit Carry Look ahead Adder (CLA) using modular 4-bit CLA blocks, optimized with CMOS technology. By segmenting the 16-bit adder into smaller 4-bit units, the design effectively reduces the carry propagation delay, which traditionally limits the speed of ripple carry adders. The CLA architecture exploits generate and propagate signals to predict carry values in advance, significantly enhancing computation speed. Implementing this architecture with CMOS ensures reduced power consumption, improved noise immunity, and enhanced performance. Simulation results demonstrate that the proposed 16-bit CLA design achieves notable improvements in speed and efficiency compared to conventional adder architectures, making it suitable for high-performance digital systems.

I. INTRODUCTION

In modern digital systems, arithmetic operations form the backbone of computing tasks, from simple calculations to complex signal processing. Among these operations, binary addition is the most fundamental and frequently executed function in processors, digital signal processors (DSPs), and application-specific integrated circuits (ASICs). As such, the performance of an adder directly impacts the overall computational efficiency and speed of a digital system. The simplest form of adder is the Ripple Carry Adder (RCA), which connects a series of full adders such that the carry output from each bit is passed as an input to the next. Although easy to design and implement, RCAs suffer from long propagation delays because each bit must wait for the carry from the previous stage. This delay increases linearly with the number of bits, making RCAs unsuitable for high-speed operations in systems with wide data paths. To address this limitation, faster adder architectures such as the Carry Lookahead Adder (CLA) have been developed. The CLA reduces the critical path delay by using generate and propagate logic to determine carry signals in parallel rather than sequentially. By calculating the carries in advance, the CLA architecture significantly shortens the computation time compared to traditional RCAs. In a CLA, generate (G) and propagate (P) signals are derived from input bits to predict the carry without waiting for the actual sum computation. This method enables faster addition and forms the basis for scalable high-speed adder designs. However, as the number of bits increases, the complexity of the CLA logic also increases, making direct implementation of large-bit CLAs inefficient in terms of area and power.

II. PROPOSED SYSTEM

The Carry Look ahead Adder (CLA) is a fast and efficient digital adder used to improve performance in arithmetic operations. The major limitation of conventional adders such as the Ripple Carry Adder (RCA) is the delay caused by the propagation of carry from one bit to the next. The CLA addresses this issue by calculating the carry signals in advance using parallel logic, thus reducing overall propagation delay.

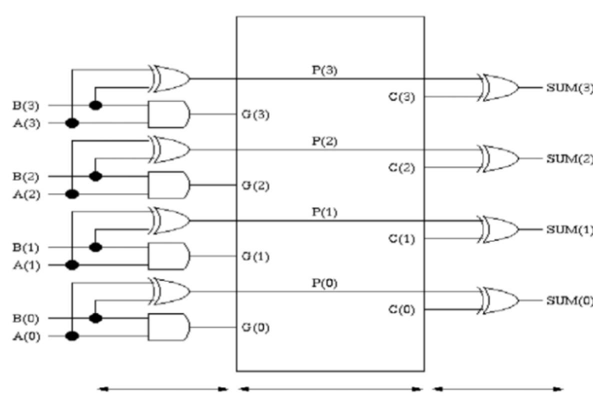


Fig: 4-bit carry look ahead adder

4 bit carry look ahead adder

1. Generate and Propagate Logic

For each bit position iii, given two input bits A(i)A(i)A(i) and B(i)B(i)B(i), the CLA uses two intermediate signals:

Generate (G): $G(i) = A(i) \cdot B(i)$

Propagate (P): $P(i) = A(i) \oplus B(i)$

Generate indicates that a carry will be produced at bit iii regardless of the input carry.

Propagate indicates that a carry will pass through bit iii if there is an input carry.

2.Carry Generation

The CLA uses the G and P signals to compute the carry for each bit without waiting for the actual carry to propagate through previous stages. For a 4-bit CLA, the carry outputs are computed as:

$$C_1 = G_0 + P_0 \cdot C_0$$
$$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot (G_0 + P_0 \cdot C_0)$$
$$C_3 = G_2 + P_2 \cdot C_2$$
$$C_4 = G_3 + P_3 \cdot C_3$$

3. Sum Generation

Once the carry signals are determined, the sum bits are calculated using:

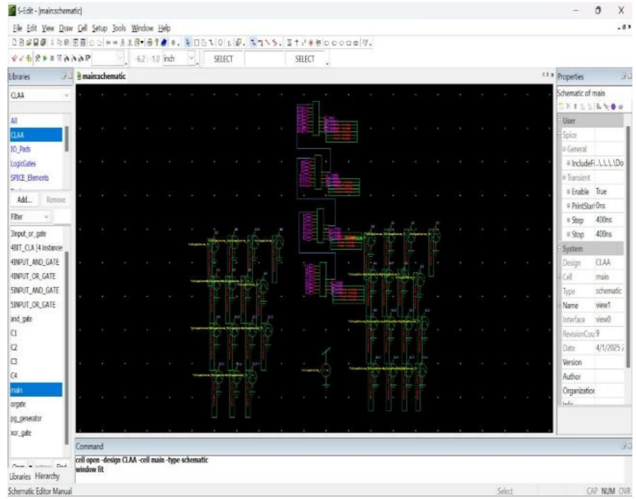
$$\mathrm{SUM}(i) = P(i) \oplus C(i)$$

A	B	C	C Out	Sum
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Fig: Truth table

III. IMPLEMENTATION DESIGN

In binary addition, carry propagation leads to delays. A carry lookahead adder addresses this by forecasting carry values ahead of time through logical expressions, instead of waiting for them to ripple through each individual bit. The 16-bit CLA adder is designed to quickly add two 16-bit binary numbers by partitioning the addition into manageable segments and calculating the carries in parallel.



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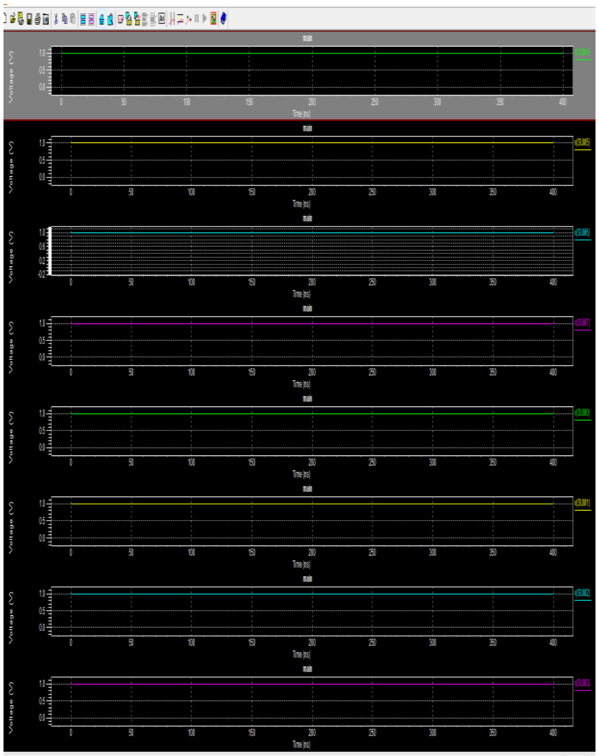
IV. RESULTS AND DISCUSSION

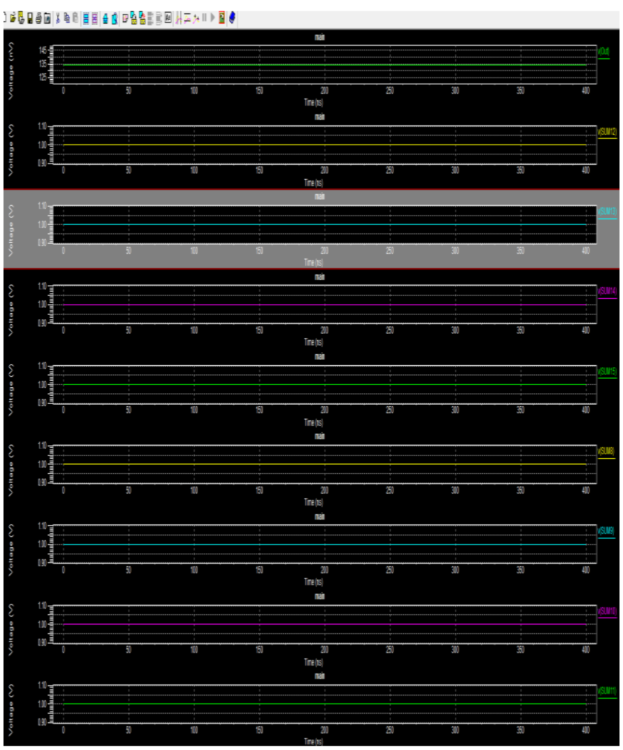
A 16-bit carry look ahead adder (CLA)made of 4-bit blocks, carry-out for each bit depends on generation(G) and propagation(P)The simulation results of a 16-bit Carry Look-Ahead Adder (CLA) in Tanner EDA typically demonstrate the functional correctness and performance advantages of the design. Using Tanner S-Edit for schematic capture and T-Spice for simulation, the adder is tested by applying various combinations of 16-bit binary inputs (A and B) along with a carry-in signal. The outputs observed in the waveform viewer (W-Edit) include the 16-bit sum and the final carry-out, which reflect the correct addition of the input values.

OUTPUTS :

A = 1111 1111 1111 1111

B = 0000 0000 0000 0000
C0 = 0





These waveforms validate that the CLA accurately computes the sum based on the logic of generate and propagate signals, even for edge cases such as carry-over and maximum input values. Additionally, the simulation provides important timing parameters like propagation delay, rise and fall times, and can estimate the maximum operating frequency, all of which highlight the CLA's high-speed performance compared to ripple carry adders. If technology libraries are included, power consumption metrics such as average and peak power can also be extracted. Overall, the simulation results confirm the functional reliability, speed advantage, and potential power efficiency of the 16-bit carry look-ahead adder when implemented and tested using Tanner EDA tools.

Power Results
vdd gnd from time 0 to 1e-006
Average power consumed -> 1.903315e-005 watts

Measurement Results
TRAN_Measure_Delay_1 = 1.8992e-009

V. FUTURE SCOPE

The 16-bit Carry Look Ahead Adder(CLA) holds significant promise for the future of high-speed digital circuit design, particularly in applications where fast arithmetic operations are critical. As computational demands continue to rise in areas like signal processing, artificial intelligence, and high-performance computing, the need for efficient and scalable arithmetic units becomes more pronounced. The CLA adder's ability to reduce propagation delay by predicting carry outputs in advance offers a substantial speed advantage over traditional ripple carry adders, making it an attractive choice for next-generation processors and digital systems. Additionally, with ongoing advancements in VLSI (Very Large Scale Integration) technology, designers can implement increasingly complex CLA circuits with optimized area, power, and performance trade-offs. Future research may focus on hybrid adder designs that combine the CLA with other architectures to further enhance speed and efficiency while minimizing hardware complexity. Therefore, the 16-bit CLA continues to be a vital building block in the evolution of faster, more efficient digital arithmetic units.

VI. CONCLUSION

This theoretical model of the 4-bit Carry Lookahead Adder provides the foundation for building higher-bit adders (such as 16-bit) by combining multiple 4-bit CLA blocks. The CLA architecture significantly improves speed compared to traditional adders, making it ideal for high-performance arithmetic circuits in modern processors and digital systems.

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