Design and Implementation of Schmitt Trigger using FINFET Technology

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***Abstract*—This paper presents the the design and implementation of a Schmitt Trigger circuit utilizing Fin Field-Effect Transistor (FinFET) technology, aimed at enhancing noise immunity and switching performance in modern digital systems. As traditional CMOS technology faces limitations in scaling and leakage control, FinFET has emerged as a promising alternative due to its superior electrostatic control and reduced short-channel effects. The proposed Schmitt Trigger is designed and simulated using advanced FinFET employing Tanner EDA tools (S-Edit and T-Spice) for schematic design, symbol creation, and transient analysis. Performance parameters such as hysteresis width, propagation delay, power consumption, are evaluated and compared with conventional planar CMOS-based designs. The results demonstrate significant improvements in speed and energy efficiency, making FinFET-based Schmitt Triggers suitable for integration in low-power and high-performance digital circuits filtering applications.**

***Index Terms*—Hysteresis, Propagation delay, Average power, CMOS, FINFET**

I. INTRODUCTION

In the ever-evolving landscape of VLSI design, delivering high performance at low power consumption has become a primary objective. The continuous downscaling of transistors has pushed traditional CMOS technology to its physical and electrical limits, especially in the deep submicron or nanometer regimes. As device dimensions shrink, issues such as short-channel effects, increased leakage currents, and degraded control over the channel pose significant challenges. To overcome these limitations, Fin Field- Effect Transistor (FinFET) technology has emerged as a compelling alternative to conventional planar transistors. FinFET devices offer superior gate control, reduced leakage, and enhanced scalability, makin them highly suitable for next- generation integrated circuits. One critical component frequently used in digital and mixed-signal circuits is the Schmitt Trigger.

Schmitt Trigger is a comparator circuit with hysteresis; it has two distinct threshold voltages for rising and falling input signals. This property makes it highly effective in eliminating noise and providing clean transitions in digital signals.

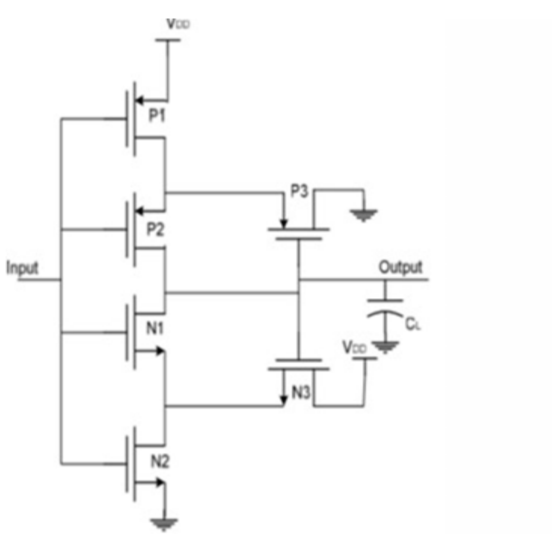
These are found to be used extensively in applications like signal conditioning, waveform shaping, switch debouncing, and clock generation circuits. They can also convert noisy or analog inputs to clean digital transitions is important for accurate system operation. However, implementing Schmitt Triggers using conventional CMOS at nanoscale dimensions introduces performance trade-offs in terms of power, delay and noise margins. As such, designing these circuits using FinFETs can lead to substantial improvements. The inherent properties of FinFETs—such as lower sub threshold leakage, higher ON/OFF current ratios, and better threshold voltage control—contribute to more robust and energy- efficient designs.This study focuses on performance evaluation of a Schmitt Trigger implemented using FinFET technology. The design process is carried by Tanner EDA tools—S-Edit for schematic capture and T-Spice for simulation. The objective is to explore how FinFETs can enhance the overall performance of the Schmitt Trigger circuit in terms of hysteresis characteristics, power efficiency, propagation delay, and noise resilience.

II. METHODLOGY

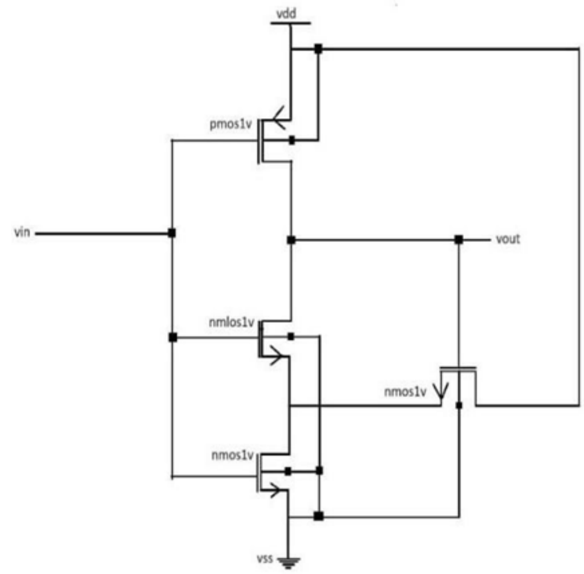
In CMOS technology,N-type and P-type transistors are employed to implement logic junctions. The same signal that activates a transistor of one kind is utilized to deactivate a transistor of the other kind. This Design and Implementation of Schmitt Trigger using FINFET Technology trait facilitates the creation of logic devices through only simple switches, eliminating the need for a pull-up resistor. In CMOS logic gates, a group of n-type MOSFETs are implemented in a pull-down network that connects the output to the low voltage

power supply rail (Vss or simply ground). Rather than a load resistor as with NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network that connects the output to the higher-voltage rail (usually referred to as Vdd).

The major features of CMOS are low static power consumption and high immunity to noise. When any one transistor out of the paired MOSFETs is switched OFF, the series configuration draws a lot of power when switching between the ON and OFF states. Hence, these devices do not produce excess heat, unlike other logic circuits, like TTL or NMOS logic, which tend to have some standby current even when not undergoing state changes. These CMOS characteristics enable the compact integration of logic functions on an integrated circuit. As a result, CMOS has emerged as the technology most commonly used for implementation in VLSI chips.



6T CMOS



4T CMOS

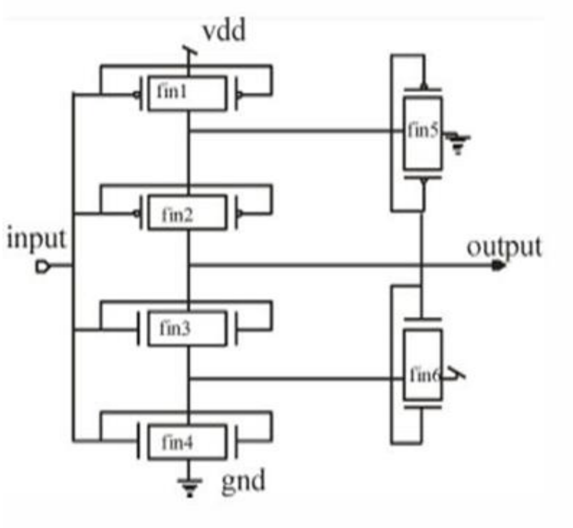
A FinFET, or Fin Field Effect Transistor, is a specialized type of field-effect transistor (FET) characterized by its tall, narrow fin structure, as opposed to a flat design. The gate envelops the channel on three sides, which are situated between the source and drain. This increased surface area between the gate and channel enhances the control over the electric state and minimizes leakage compared to traditional planar FETs. The use of FinFET technology significantly improves the electrostatic control of the channel, resulting in superior electrical characteristics when compared to planar FETs. FinFET is a member of the FET family

structure of FinFET features a three- dimensional fin, along with the gate, drain, source, and substrate.

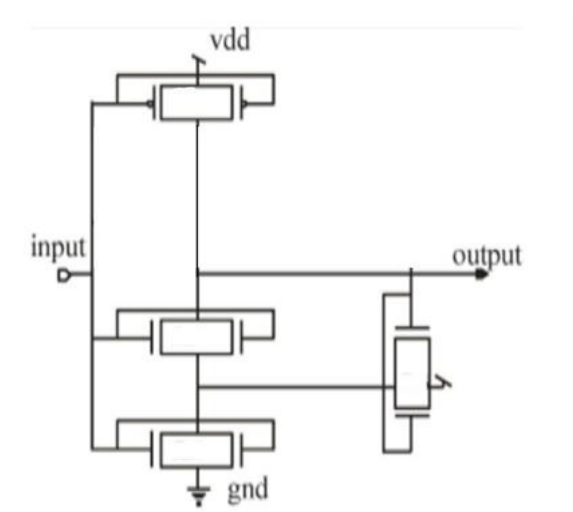
- *Fin*: The term FinFET is derived from this three-dimensional vertical fin-like form that acts as the channel in FinFET. The fin is made from semiconductor material or silicon.
- *Gate*: The role of the gate in FinFET is similar to that in a typical MOSFET. The fin of the FinFET surrounds the gate of the FinFET, and the gate creates a three- dimensional structure; multiple gates can exist in a FinFET. The gate is made from metal. The gate is employed to control the flow of electric current in the channel.
- *Drain and Source*: The drain and source of FinFET function similarly to those in MOSFET. Current

enters through the source and exits via the drain, with the gate serving to regulate the current. Carriers within the channel come in through the source and exit through the drain. Just like in the MOSFET, in FinFET too, the drain is at a high potential while the source is at a low potential.

The term FINFET is inspired by the shape of a fish fin, as the top view of the FINFET's drain and source resembles this fin. The fin can also be viewed as the connection between the drain and the source. Similar to MOSFET, FINFET is constructed on silicon on insulator (SOI) technology and is a three-terminal device that includes the gate, drain, and source, with its fabrication process being similar to that of MOSFET. Both FINFET and MOSFET operate based on the same underlying principles. The fundamental



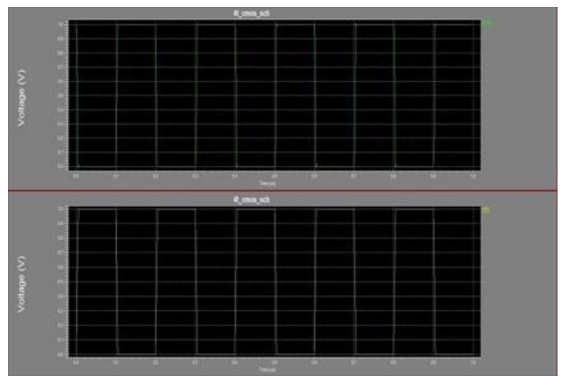
6T FINFET



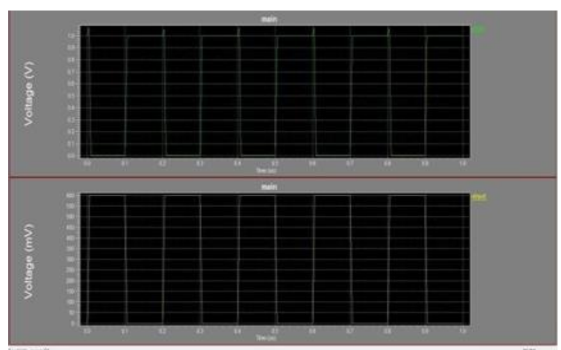
4T FINFET

III. RESULT

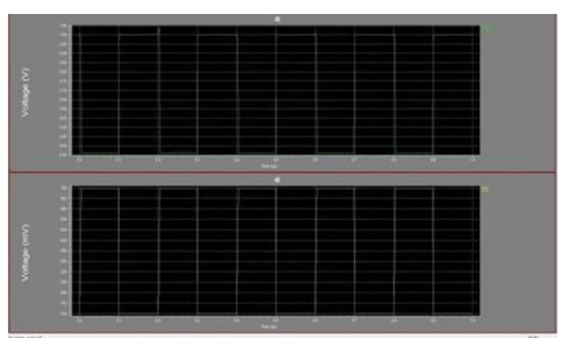
6T CMOS



4T CMOS

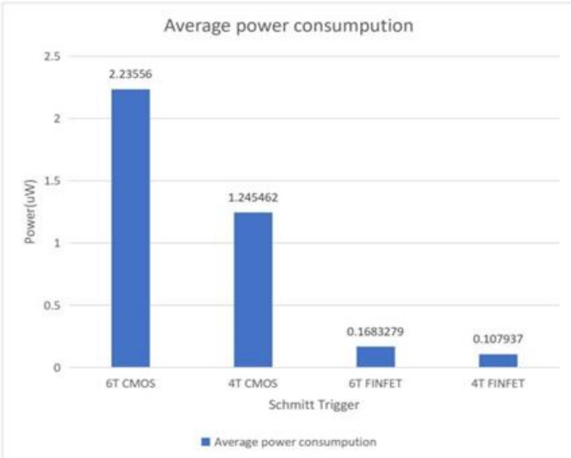


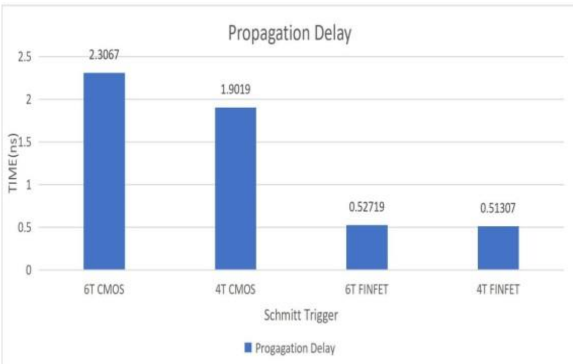
6T FINFET

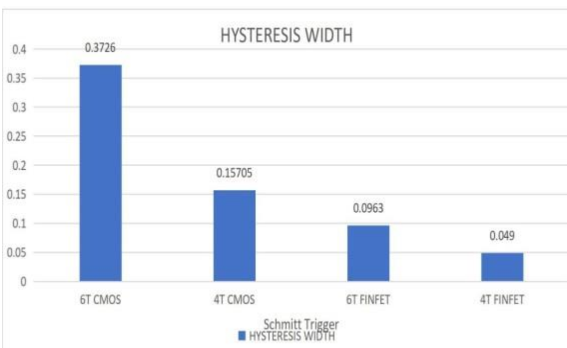


4T FINFET

IV. OBSERVATIONS







V. OBSERVATION TABLES

S.NO	Mode of Schmitt trigger	Power consumption
1	6T CMOS	2.23556
2	4T CMOS	1.245462
3	6T FINFET	0.1683279
4	4T FINFET	0.107937

Table-1 : Schmitt Trigger parameter analysis in power consumption

S.NO	Mode of Schmitt trigger	Propagation Delay
1	6T CMOS	2.3067
2	4T CMOS	1.9019
3	6T FINFET	0.52719
4	4T FINFET	0.51307

Table-2 : Schmitt Trigger parameter analysis in Propagation delay

S.NO	Mode of Schmitt trigger	Hysteresis width
1	6T CMOS	0.3726
2	4T CMOS	0.15705
3	6T FINFET	0.0963
4	4T FINFET	0.049

Table-3 : Schmitt Trigger parameter analysis in Hysteresis width

VI. ADVANTAGES

The device offers reduced power consumption, improved noise immunity, a compact design, high-speed operation, and scalability.

VII. APPLICATIONS

Signal conditioning, square wave generation, oscillators, switching power supplies, data communication, level translators, and waveform generators are essential components in electronic systems.

VIII. FUTURE SCOPE

FinFETs will continue to be scaled down to smaller node sizes (e.g., 3nm and beyond), offering improved performance and energy efficiency.FinFETs are well-suited for low-power logic systems, high-performance computing, and artificial intelligence. GAAFETs are being developed as a potential replacement for FinFETs in future chip architectures, especially for extreme scaling. While FinFETs offer advantages like improved performance and lower power consumption, they face challenges with scaling down to very small dimensions. GAAFETs, with their gate-all-around structure, promise better control over current flow, potentially leading to faster switching speeds and even more efficient energy consumption.

IX. CONCLUSION

This study presents the design and implementation of a Schmitt Trigger using FinFET technology, with a comparative analysis against traditional CMOS-based designs. The results clearly indicate that FinFETs, owing to their superior gate control, reduced leakage current, and better scalability, offer a significant performance advantage in nanoscale circuit design.

Through simulation and analysis, the FinFET-based Schmitt Trigger demonstrated improved hysteresis characteristics, reduced propagation delay, and lower power consumption when compared to its CMOS counterpart. These improvements make FinFET's an ideal choice for modern low-power and high-performance applications, especially in noise-sensitive and compact VLSI systems.

Performance: FinFET-based Schmitt triggers typically exhibit improved performance characteristics compared to CMOS-based counterparts. The three-dimensional structure of FinFET's allows for better electrostatic control, reduced leakage current, and enhanced switching speeds, leading to superior overall performance.

Energy Efficiency: FinFET technology offers better energy efficiency due to reduced leakage currents and improved gate control, making it well- suited for low-power applications where energy efficiency is critical.

Noise Immunity: Both CMOS and FinFET-based Schmitt triggers provide noise immunity through hysteresis, but FinFET's may offer additional advantages due to their improved electrostatic control and reduced susceptibility to process variations.

Scalability: FinFET technology enables continued scaling to smaller feature sizes, allowing for higher transistor density and improved integration levels on semiconductor chips. This scalability is essential for meeting the demands of advanced semiconductor applications.

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